

54-MHz 32-bit RX MCUs, built-in FPU, 88.56 DMIPS, up to 512-KB flash memory, various communication functions including USB 2.0 full-speed host/function/OTG, CAN, SD host interface, serial sound interface, capacitive touch sensing unit, 12-bit A/D, 12-bit D/A, RTC, AES, MPU security functions

Features

■ 32-bit RXv2 CPU core

- Max. operating frequency: 54 MHz
- Capable of 88.56 DMIPS in operation at 54 MHz
- Enhanced DSP: 32-bit multiply-accumulate and 16-bit multiply-subtract instructions supported
- Built-in FPU: 32-bit single-precision floating point (compliant to IEEE754)
- Divider (fastest instruction execution takes two CPU clock cycles)
- Fast interrupt
- CISC Harvard architecture with 5-stage pipeline
- Variable-length instructions, ultra-compact code
- On-chip debugging circuit
- Memory protection unit (MPU) supported

■ Low power design and architecture

- Operation from a single 1.8-V to 5.5-V supply
- RTC capable of operating on the battery backup power supply
- Three low power consumption modes
- Low power timer (LPT) that operates during the software standby state

■ On-chip flash memory for code

- 128- to 512-Kbyte capacities
- On-board or off-board user programming
- Programmable at 1.8 V
- For instructions and operands

■ On-chip data flash memory

- 8 Kbytes (1,000,000 program/erase cycles (typ.))
- BGO (Background Operation)

■ On-chip SRAM, no wait states

- 32- to 64-Kbyte size capacities

■ Data transfer functions

- DMAC: Incorporates four channels
- DTC: Four transfer modes

■ ELC

- Module operation can be initiated by event signals without using interrupts.
- Linked operation between modules is possible while the CPU is sleeping.

■ Reset and supply management

- Eight types of reset, including the power-on reset (POR)
- Low voltage detection (LVD) with voltage settings

■ Clock functions

- Main clock oscillator frequency: 1 to 20 MHz
- External clock input frequency: Up to 20 MHz
- Sub-clock oscillator frequency: 32.768 kHz
- PLL circuit input: 4 MHz to 12.5 MHz
- On-chip low- and high-speed oscillators, dedicated on-chip low-speed oscillator for the IWDTC
- USB-dedicated PLL circuit: 4, 6, 8, or 12 MHz
- 54 MHz can be set for the system clock and 48 MHz for the USB clock
- Generation of a dedicated 32.768-kHz clock for the RTC
- Clock frequency accuracy measurement circuit (CAC)

■ Realtime clock

- Adjustment functions (30 seconds, leap year, and error)
- Calendar count mode or binary count mode selectable
- Time capture function
- Time capture on event-signal input through external pins

■ Independent watchdog timer

- 15-kHz on-chip oscillator produces a dedicated clock signal to drive IWDTC operation.

■ Useful functions for IEC60730 compliance

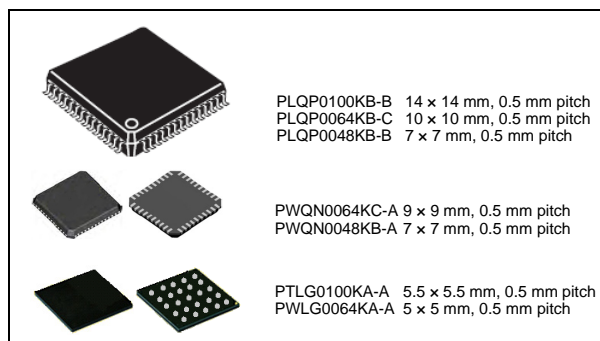
- Self-diagnostic and disconnection-detection assistance functions for the A/D converter, clock frequency accuracy measurement circuit, independent watchdog timer, RAM test assistance functions using the DOC, etc.

■ External address space

- Four CS areas (4 × 16 Mbytes)
- 8- or 16-bit bus space is selectable per area

■ MPC

- Input/output functions selectable from multiple pins



PLQP0100KB-B 14 × 14 mm, 0.5 mm pitch
 PLQP0064KB-C 10 × 10 mm, 0.5 mm pitch
 PLQP0048KB-B 7 × 7 mm, 0.5 mm pitch

PWQN0064KC-A 9 × 9 mm, 0.5 mm pitch
 PWQN0048KB-A 7 × 7 mm, 0.5 mm pitch

PTLG0100KA-A 5.5 × 5.5 mm, 0.5 mm pitch
 PWLG0064KA-A 5 × 5 mm, 0.5 mm pitch

■ Up to 14 communication functions

- USB 2.0 host/function/On-The-Go (OTG) (one channel), full-speed = 12 Mbps, low-speed = 1.5 Mbps, isochronous transfer, and BC (Battery Charger) supported
- CAN (one channel) compliant to ISO11898-1: Transfer at up to 1 Mbps
- SCI with many useful functions (up to 7 channels) Asynchronous mode, clock synchronous mode, smart card interface Reduction of errors in communications using the bit modulation function
- IrDA interface (one channel, in cooperation with the SCI5)
- I²C bus interface: Transfer at up to 400 kbps, capable of SMBus operation (one channel)
- RSPI (one channel): Transfer at up to 16 Mbps
- Serial sound interface (one channel)
- SD host interface (optional: one channel) SD memory/ SDIO 1-bit or 4-bit SD bus supported
 Note: 48-pin packages support 1-bit mode only

■ Up to 20 extended-function timers

- 16-bit MTU: input capture, output compare, complementary PWM output, phase counting mode (six channels)
- 16-bit TPU: input capture, output compare, phase counting mode (six channels)
- 8-bit TMR (four channels)
- 16-bit compare-match timers (four channels)

■ 12-bit A/D converter

- Capable of conversion within 0.83 μs
- 24 channels
- Sampling time can be set for each channel
- Self-diagnostic function and analog input disconnection detection assistance function

■ 12-bit D/A converter

- Two channels

■ Capacitive touch sensing unit

- Self-capacitance method: A single pin configures a single key, supporting up to 24 keys
- Mutual capacitance method: Matrix configuration with 24 pins, supporting up to 144 keys

■ Analog comparator

- Two channels × two units

■ General I/O ports

- 5-V tolerant, open drain, input pull-up, switching of driving capacity

■ Security Functions (TSIP-Lite)

- Unauthorized access to the encryption engine is disabled and imposture and falsification of information are prevented
- Safe management of keys
- 128- or 256-bit key length of AES for ECB, CBC, GCM, others
- True random number generator

■ Temperature sensor

■ Operating temperature range

- -40 to +85°C
- -40 to +105°C

■ Applications

- General industrial and consumer equipment

1. Overview

1.1 Outline of Specifications

Table 1.1 lists the specifications, and Table 1.2 gives a comparison of the functions of the products in different packages.

Table 1.1 is for products with the greatest number of functions, so the number of peripheral modules and channels will differ in accordance with the package type. For details, see Table 1.2, Comparison of Functions for Different Packages.

Table 1.1 Outline of Specifications (1/4)

Classification	Module/Function	Description
CPU	CPU	<ul style="list-style-type: none"> Maximum operating frequency: 54 MHz 32-bit RX CPU (RX v2) Minimum instruction execution time: One instruction per clock cycle Address space: 4-Gbyte linear Register set <ul style="list-style-type: none"> General purpose: Sixteen 32-bit registers Control: Ten 32-bit registers Accumulator: Two 72-bit registers Basic instructions: 75 (variable-length instruction format) Floating-point instructions: 11 DSP instructions: 23 Addressing modes: 10 Data arrangement <ul style="list-style-type: none"> Instructions: Little endian Data: Selectable as little endian or big endian On-chip 32-bit multiplier: 32-bit × 32-bit → 64-bit On-chip divider: 32-bit ÷ 32-bit → 32 bits Barrel shifter: 32 bits Memory protection unit (MPU)
	FPU	<ul style="list-style-type: none"> Single precision (32-bit) floating point Data types and floating-point exceptions in conformance with the IEEE754 standard
Memory	ROM	<ul style="list-style-type: none"> Capacity: 128/256/384/512 Kbytes Up to 32 MHz: No-wait memory access 32 to 54 MHz: Wait state required. No wait state if the instruction is served by a ROM accelerator hit. Programming/erasing method: <ul style="list-style-type: none"> Serial programming (asynchronous serial communication/USB communication), self-programming
	RAM	<ul style="list-style-type: none"> Capacity: 32/64 Kbytes 54 MHz, no-wait memory access
	E2 DataFlash	<ul style="list-style-type: none"> Capacity: 8 Kbytes Number of erase/write cycles: 1,000,000 (typ)
MCU operating mode		Single-chip mode, on-chip ROM enabled expansion mode, and on-chip ROM disabled expansion mode (software switching)
Clock	Clock generation circuit	<ul style="list-style-type: none"> Main clock oscillator, sub-clock oscillator, low-speed on-chip oscillator, high-speed on-chip oscillator, PLL frequency synthesizer, USB-dedicated PLL frequency synthesizer, and IWDG-dedicated on-chip oscillator Oscillation stop detection: Available Clock frequency accuracy measurement circuit (CAC) Independent settings for the system clock (ICLK), peripheral module clock (PCLK), external bus clock (BCLK), and FlashIF clock (FCLK) The CPU and system sections such as other bus masters run in synchronization with the system clock (ICLK): 54 MHz (at max.) MTU2a runs in synchronization with the PCLKA: 54 MHz (at max.) The ADCLK for the S12AD runs in synchronization with the PCLKD: 54 MHz (at max.) Peripheral modules other than MTU2a and S12ADE run in synchronization with the PCLKB: 32 MHz (at max.) Devices connected to external buses run in synchronization with the BCLK: 32 MHz (at max.) The flash peripheral circuit runs in synchronization with the FCLK: 32 MHz (at max.)
Resets		RES# pin reset, power-on reset, voltage monitoring reset, watchdog timer reset, independent watchdog timer reset, and software reset
Voltage detection	Voltage detection circuit (LVDAb)	<ul style="list-style-type: none"> When the voltage on VCC falls below the voltage detection level, an internal reset or internal interrupt is generated. Voltage detection circuit 0 is capable of selecting the detection voltage from 4 levels Voltage detection circuit 1 is capable of selecting the detection voltage from 14 levels Voltage detection circuit 2 is capable of selecting the detection voltage from 4 levels

Table 1.1 Outline of Specifications (2/4)

Classification	Module/Function	Description
Low power consumption	Low power consumption functions	<ul style="list-style-type: none"> Module stop function Three low power consumption modes Sleep mode, deep sleep mode, and software standby mode Low power timer that operates during the software standby state
	Function for lower operating power consumption	<ul style="list-style-type: none"> Operating power control modes High-speed operating mode, middle-speed operating mode, and low-speed operating mode
Interrupt	Interrupt controller (ICUb)	<ul style="list-style-type: none"> Interrupt vectors: 167 External interrupts: 9 (NMI, IRQ0 to IRQ7 pins) Non-maskable interrupts: 7 (NMI pin, oscillation stop detection interrupt, voltage monitoring 1 interrupt, voltage monitoring 2 interrupt, WDT interrupt, IWDI interrupt, and VBATT power monitoring interrupt) 16 levels specifiable for the order of priority
External bus extension		<ul style="list-style-type: none"> The external address space can be divided into four areas (CS0 to CS3), each with independent control of access settings. Capacity of each area: 16 Mbytes (CS0 to CS3) A chip-select signal (CS0# to CS3#) can be output for each area. Each area is specifiable as an 8-bit or 16-bit bus space The data arrangement in each area is selectable as little or big endian (only for data). Bus format: Separate bus, multiplex bus Wait control Write buffer facility
DMA	DMA controller (DMACA)	<ul style="list-style-type: none"> 4 channels Three transfer modes: Normal transfer, repeat transfer, and block transfer Activation sources: Software trigger, external interrupts, and interrupt requests from peripheral functions
	Data transfer controller (DTCa)	<ul style="list-style-type: none"> Transfer modes: Normal transfer, repeat transfer, and block transfer Activation sources: Interrupts Chain transfer function
I/O ports	General I/O ports	<p>100-pin /64-pin /48-pin I/O: 79/43/30 (RX231 Group), 83/47/34 (RX230 Group)</p> <ul style="list-style-type: none"> Input: 1/1/1 Pull-up resistors: 79/43/30(RX231 Group), 83/47/34 (RX230 Group) Open-drain outputs: 58/34/26 5-V tolerance: 5/3/3
Event link controller (ELC)		<ul style="list-style-type: none"> Event signals of 61 types can be directly connected to the module Operations of timer modules are selectable at event input Capable of event link operation for port B and port E
Multi-function pin controller (MPC)		Capable of selecting the input/output function from multiple pins
Timers	16-bit timer pulse unit (TPUa)	<ul style="list-style-type: none"> (16 bits × 6 channels) × 1 unit Maximum of 16 pulse-input/output possible Select from among seven or eight counter-input clock signals for each channel Supports the input capture/output compare function Output of PWM waveforms in up to 15 phases in PWM mode Support for buffered operation, phase-counting mode (two-phase encoder input) and cascade connected operation (32 bits × 2 channels) depending on the channel. Capable of generating conversion start triggers for the A/D converters Signals from the input capture pins are input via a digital filter Clock frequency measuring method
	Multi-function timer pulse unit 2 (MTU2a)	<ul style="list-style-type: none"> (16 bits × 6 channels) × 1 unit Up to 16 pulse-input/output lines and three pulse-input lines are available based on the six 16-bit timer channels Select from among eight or seven counter-input clock signals for each channel (PCLK/1, PCLK/4, PCLK/16, PCLK/64, PCLK/256, PCLK/1024, MTCLKA, MTCLKB, MTCLKC, MTCLKD) other than channel 5, for which only four signals are available. Input capture function 21 output compare/input capture registers Pulse output mode Complementary PWM output mode Reset synchronous PWM mode Phase-counting mode Capable of generating conversion start triggers for the A/D converter
	Port output enable 2 (POE2a)	Controls the high-impedance state of the MTU's waveform output pins
	Compare match timer (CMT)	<ul style="list-style-type: none"> (16 bits × 2 channels) × 2 units Select from among four clock signals (PCLK/8, PCLK/32, PCLK/128, PCLK/512)
	Watchdog timer (WDTA)	<ul style="list-style-type: none"> 14 bits × 1 channel Select from among six counter-input clock signals (PCLK/4, PCLK/64, PCLK/128, PCLK/512, PCLK/2048, PCLK/8192)

Table 1.1 Outline of Specifications (3/4)

Classification	Module/Function	Description
Timers	Independent watchdog timer (IWDTa)	<ul style="list-style-type: none"> • 14 bits × 1 channel • Count clock: Dedicated low-speed on-chip oscillator for the IWDT Frequency divided by 1, 16, 32, 64, 128, or 256
	Realtime clock (RTCe)	<ul style="list-style-type: none"> • Clock source: Sub-clock • Time/calendar • Interrupts: Alarm interrupt, periodic interrupt, and carry interrupt • Time-capture facility for three values
	Low power timer (LPT)	<ul style="list-style-type: none"> • 16 bits × 1 channel • Clock source: Sub-clock, Dedicated low-speed on-chip oscillator for the IWDT Frequency divided by 2, 4, 8, 16, or 32
	8-bit timer (TMR)	<ul style="list-style-type: none"> • (8 bits × 2 channels) × 2 units • Seven internal clocks (PCLK/1, PCLK/2, PCLK/8, PCLK/32, PCLK/64, PCLK/1024, and PCLK/8192) and an external clock can be selected • Pulse output and PWM output with any duty cycle are available • Two channels can be cascaded and used as a 16-bit timer
Communication functions	Serial communications interfaces (SCIg, SCIH)	<ul style="list-style-type: none"> • 7 channels (channel 0, 1, 5, 6, 8, 9: SCIg, channel 12: SCIH) • SCIg <ul style="list-style-type: none"> Serial communications modes: Asynchronous, clock synchronous, and smart-card interface Multi-processor function On-chip baud rate generator allows selection of the desired bit rate Choice of LSB-first or MSB-first transfer Average transfer rate clock can be input from TMR timers for SCI5, SCI6, and SCI12 Start-bit detection: Level or edge detection is selectable. Simple I²C Simple SPI 9-bit transfer mode Bit rate modulation Event linking by the ELC (only on channel 5) • SCIH (The following functions are added to SCIg) <ul style="list-style-type: none"> Supports the serial communications protocol, which contains the start frame and information frame Supports the LIN format
	IrDA interface (IRDA)	<ul style="list-style-type: none"> • 1 channel (SCI5 used) • Supports encoding/decoding of waveforms conforming to IrDA standard 1.0
	I ² C bus interface (RIICa)	<ul style="list-style-type: none"> • 1 channel • Communications formats: I²C bus format/SMBus format • Master mode or slave mode selectable • Supports fast mode
	Serial peripheral interface (RSP1a)	<ul style="list-style-type: none"> • 1 channel • Transfer facility <ul style="list-style-type: none"> Using the MOSI (master out, slave in), MISO (master in, slave out), SSL (slave select), and RSPCK (RSP1 clock) enables serial transfer through SPI operation (four lines) or clock-synchronous operation (three lines) • Capable of handling serial transfer as a master or slave • Data formats • Choice of LSB-first or MSB-first transfer <ul style="list-style-type: none"> The number of bits in each transfer can be changed to 8, 9, 10, 11, 12, 13, 14, 15, 16, 20, 24, or 32 bits. 128-bit buffers for transmission and reception Up to four frames can be transmitted or received in a single transfer operation (with each frame having up to 32 bits) • Double buffers for both transmission and reception
	USB 2.0 host/function module (USBd)	<ul style="list-style-type: none"> • USB Device Controller (UDC) and transceiver for USB 2.0 are incorporated. • Host/function module: 1 port • Compliant with USB version 2.0 • Transfer speed: Full-speed (12 Mbps), low-speed (1.5 Mbps) • OTG (ON-The-Go) is supported. • Isochronous transfer is supported. • BC1.2 (Battery Charging Specification Revision 1.2) is supported. • Internal power supply for USB (allows operation without external power input to the VCC_USB pin when VCC = 4.0 to 5.5V)
	CAN module (RSCAN)	<ul style="list-style-type: none"> • 1 channel • Compliance with the ISO11898-1 specification (standard frame and extended frame) • 16 Message boxes

Table 1.1 Outline of Specifications (4/4)

Classification	Module/Function	Description
Communication functions	Serial Sound Interface (SSI)	<ul style="list-style-type: none"> • 1 channel • Capable of duplex communications • Various serial audio formats supported • Master/slave function supported • Programmable word clock or bit clock generation function • 8/16/18/20/22/24/32-bit data formats supported • On-chip 8-stage FIFO for transmission/reception • Supports WS continue mode in which the SSIWS signal is not stopped.
	SD Host Interface (SDHla)	<ul style="list-style-type: none"> • 1 channel • Transfer speed : Default speed mode (8MB/s) • SD memory card interface (1 bit / 4bits SD bus) • MMC, eMMC Backward-compatible are supported. • SD Specifications <ul style="list-style-type: none"> Part 1: Compliant with Physical Layer Specification Ver.3.01 (Not support DDR) Part E1: SDIO Specification Ver. 3.00 • Compliant with USB version 2.0 • Error check function: CRC7 (command), CRC16 (data) • Interrupt Source: Card access interrupt, SDIO access interrupt, Card detection interrupt, SD buffer access interrupt • DMA transfer sources: SD_BUFwrite, SD_BUF read • Card detection, Write protection
Security functions		<ul style="list-style-type: none"> • Access management circuit • Encryption engine <ul style="list-style-type: none"> 128- or 256-bit key sizes of AES Block cipher mode of operation: GCM, ECB, CBC, CMAC, XTS, CTR, GCTR • Hash function • True random number generator • Unique ID
12-bit A/D converter (S12ADE)		<ul style="list-style-type: none"> • 12 bits (24 channels × 1 unit) • 12-bit resolution • Minimum conversion time: 0.83 μs per channel when the ADCLK is operating at 54 MHz • Operating modes <ul style="list-style-type: none"> Scan mode (single scan mode, continuous scan mode, and group scan mode) Group A priority control (only for group scan mode) • Sampling variable <ul style="list-style-type: none"> Sampling time can be set up for each channel. • Self-diagnostic function • Double trigger mode (A/D conversion data duplicated) • Detection of analog input disconnection • A/D conversion start conditions <ul style="list-style-type: none"> A software trigger, a trigger from a timer (MTU, TPU), an external trigger signal, or ELC • Event linking by the ELC
Temperature sensor (TEMPSA)		<ul style="list-style-type: none"> • 1 channel • The voltage output from the temperature sensor is converted into a digital value by the 12-bit A/D converter.
12-bit D/A converter (R12DAA)		<ul style="list-style-type: none"> • 2 channels • 12-bit resolution • Output voltage: 0.4 to AVCC0-0.5V
CRC calculator (CRC)		<ul style="list-style-type: none"> • CRC code generation for arbitrary amounts of data in 8-bit units • Select any of three generating polynomials: <ul style="list-style-type: none"> $X^8 + X^2 + X + 1$, $X^{16} + X^{15} + X^2 + 1$, or $X^{16} + X^{12} + X^5 + 1$ • Generation of CRC codes for use with LSB-first or MSB-first communications is selectable.
Comparator B (CMPBa)		<ul style="list-style-type: none"> • 2 channels × 2 units • Function to compare the reference voltage and the analog input voltage • Window comparator operation or standard comparator operation is selectable
Capacitive touch sensing unit (CTSU)		Detection pin: 24 channels
Data operation circuit (DOC)		Comparison, addition, and subtraction of 16-bit data
Power supply voltages/Operating frequencies		VCC = 1.8 to 2.4 V: 8 MHz, VCC = 2.4 to 2.7 V: 16 MHz, VCC = 2.7 to 5.5 V: 54 MHz
Operating temperature range		D version: -40 to +85°C, G version: -40 to +105°C
Packages		100-pin TFLGA (PTLG0100KA-A) 5.5 × 5.5 mm, 0.5 mm pitch 100-pin LQFP (PLQP0100KB-B) 14 × 14 mm, 0.5 mm pitch 64-pin WFLGA (PWLG0064KA-A) 5 × 5 mm, 0.5 mm pitch 64-pin HWQFN (PWQN0064KC-A) 9 × 9 mm, 0.5 mm pitch 64-pin LQFP (PLQP0064KB-C) 10 × 10 mm, 0.5 mm pitch 48-pin HWQFN (PWQN0048KB-A) 7 × 7 mm, 0.5 mm pitch 48-pin LQFP (PLQP0048KB-B) 7 × 7 mm, 0.5 mm pitch
On-chip debugging system		E1 emulator (FINE interface)

Table 1.2 Comparison of Functions for Different Packages

Module/Functions		RX230 Group			RX231 Group		
		100 Pins	64 Pins	48 Pins	100 Pins	64 Pins	48 Pins
External bus	External bus	16 bit	Not supported		16 bit	Not supported	
Interrupts	External interrupts	NMI, IRQ0 to IRQ7	NMI, IRQ0 to IRQ2, IRQ4 to IRQ7	NMI, IRQ0, IRQ1, IRQ4 to IRQ7	NMI, IRQ0 to IRQ7	NMI, IRQ0 to IRQ2, IRQ4 to IRQ7	NMI, IRQ0, IRQ1, IRQ4 to IRQ7
DMA	DMA controller	4 channels (DMAC0 to DMAC3)			4 channels (DMAC0 to DMAC3)		
	Data transfer controller	Available			Available		
Timers	16-bit timer pulse unit	6 channels (TPU0 to TPU5)			6 channels (TPU0 to TPU5)		
	Multi-function timer pulse unit 2	6 channels (MTU0 to MTU5)			6 channels (MTU0 to MTU5)		
	Port output enable 2	POE0# to POE3#, POE8#			POE0# to POE3#, POE8#		
	8-bit timer	2 channelsx 2 units			2 channelsx 2 units		
	Compare match timer	2 channelsx 2 units			2 channelsx 2 units		
	Low power timer	1 channel			1 channel		
	Realtime clock	Available		Not supported	Available		Not supported
	Watchdog timer	Available			Available		
	Independent watchdog timer	Available			Available		
Communication functions	Serial communications interfaces (SCIg)	6 channels (SCI0, 1, 5, 6, 8, 9)	5 channels (SCI1, 5, 6, 8, 9)	4 channels (SCI1, 5, 6, 8)	6 channels (SCI0, 1, 5, 6, 8, 9)	5 channels (SCI1, 5, 6, 8, 9)	4 channels (SCI1, 5, 6, 8)
	IrDA interface	1 channel (SCI5)			1 channel (SCI5)		
	Serial communications interfaces (SCIh)	1 channel (SCI12)			1 channel (SCI12)		
	I ² C bus interface	1 channel			1 channel		
	CAN module	Not supported			1 channel		
	Serial peripheral interface	1 channel			1 channel		
	USB 2.0 host/function module	Not supported			1 channel		
	Serial sound interface	1 channel			1 channel		
SD Host Interface	Not supported			1 channel			
Capacitive touch sensing unit	24 channels	10 channels	6 channels	24 channels	10 channels	6 channels	
12-bit A/D converter (including high-precision channels)	24 channels (8 channels)	12 channels (6 channels)	8 channels (4 channels)	24 channels (8 channels)	12 channels (6 channels)	8 channels (4 channels)	
Temperature sensor	Available			Available			
D/A converter	2 channels		Not supported	2 channels		Not supported	
CRC calculator	Available			Available			
Event link controller	Available			Available			
Comparator B	4 channels			4 channels			
Packages	100-pin TFLGA 100-pin LFQFP	64-pin WFLGA 64-pin HWQFN 64-pin LFQFP	48-pin HWQFN 48-pin LFQFP	100-pin TFLGA 100-pin LFQFP	64-pin WFLGA 64-pin HWQFN 64-pin LFQFP	48-pin HWQFN 48-pin LFQFP	

1.2 List of Products

Table 1.3 and Table 1.4 are a list of products, and Figure 1.1 shows how to read the product part no., memory capacity, and package type.

Table 1.3 List of Products: D Version (T_a = -40 to +85°C) (1/2)

Group	Part No.	Order Part No.	Package	ROM Capacity	RAM Capacity	E2 DataFlash	Operating Frequency	Security Function	SDHI	CAN	Operating Temperature
RX231	R5F52318ADLA	R5F52318ADLA#20	PTLG0100KA-A	512 Kbytes	64 Kbytes	8 Kbytes	54 MHz	Not available	Not available	Available	-40 to +85°C
	R5F52318BDLA	R5F52318BDLA#20						Available	Available	Available	
	R5F52318ADFP	R5F52318ADFP#30	PLQP0100KB-B					Not available	Not available	Available	
	R5F52318BDFP	R5F52318BDFP#30						Available	Available	Available	
	R5F52318ADND	R5F52318ADND#U0	PWQN0064KC-A					Not available	Not available	Available	
	R5F52318BDND	R5F52318BDND#U0						Available	Available	Available	
	R5F52318ADFM	R5F52318ADFM#30	PLQP0064KB-C					Not available	Not available	Available	
	R5F52318BDFM	R5F52318BDFM#30						Available	Available	Available	
	R5F52318ADNE	R5F52318ADNE#U0	PWQN0048KB-A					Not available	Not available	Available	
	R5F52318BDNE	R5F52318BDNE#U0						Available	Available	Available	
	R5F52318ADFL	R5F52318ADFL#30	PLQP0048KB-B					Not available	Not available	Available	
	R5F52318BDFL	R5F52318BDFL#30						Available	Available	Available	
	R5F52317ADLA	R5F52317ADLA#20	PTLG0100KA-A	384 Kbytes	32 Kbytes	8 Kbytes	54 MHz	Not available	Not available	Available	
	R5F52317BDLA	R5F52317BDLA#20						Available	Available	Available	
	R5F52317ADFP	R5F52317ADFP#30	PLQP0100KB-B					Not available	Not available	Available	
	R5F52317BDFP	R5F52317BDFP#30						Available	Available	Available	
	R5F52317ADND	R5F52317ADND#U0	PWQN0064KC-A					Not available	Not available	Available	
	R5F52317BDND	R5F52317BDND#U0						Available	Available	Available	
	R5F52317ADFM	R5F52317ADFM#30	PLQP0064KB-C					Not available	Not available	Available	
	R5F52317BDFM	R5F52317BDFM#30						Available	Available	Available	
	R5F52317ADNE	R5F52317ADNE#U0	PWQN0048KB-A					Not available	Not available	Available	
	R5F52317BDNE	R5F52317BDNE#U0						Available	Available	Available	
	R5F52317ADFL	R5F52317ADFL#30	PLQP0048KB-B					Not available	Not available	Available	
	R5F52317BDFL	R5F52317BDFL#30						Available	Available	Available	
	R5F52316ADLA	R5F52316ADLA#20	PTLG0100KA-A	256 Kbytes	32 Kbytes	8 Kbytes	54 MHz	Not available	Not available	Available	
	R5F52316CDLA	R5F52316CDLA#20						Not available	Not available	Not available	
	R5F52316ADFP	R5F52316ADFP#30	PLQP0100KB-B					Not available	Not available	Available	
	R5F52316CDFP	R5F52316CDFP#30						Not available	Not available	Not available	
	R5F52316CDLF	R5F52316CDLF#U0	PWLG0064KA-A					Not available	Not available	Not available	
	R5F52316ADND	R5F52316ADND#U0						Not available	Not available	Available	
	R5F52316CDND	R5F52316CDND#U0	PWQN0064KC-A					Not available	Not available	Not available	
	R5F52316ADFM	R5F52316ADFM#30						Not available	Not available	Available	
R5F52316CDFM	R5F52316CDFM#30	PWQN0048KB-A	Not available					Not available	Not available		
R5F52316ADNE	R5F52316ADNE#U0		Not available					Not available	Available		
R5F52316CDNE	R5F52316CDNE#U0	PLQP0048KB-B	Not available					Not available	Not available		
R5F52316ADFL	R5F52316ADFL#30		Not available					Not available	Available		
R5F52316CDFL	R5F52316CDFL#30	PLQP0048KB-B	Not available	Not available	Not available						
R5F52316CDFL	R5F52316CDFL#30		Not available	Not available	Not available						

Table 1.3 List of Products: D Version (T_a = -40 to +85°C) (2/2)

Group	Part No.	Order Part No.	Package	ROM Capacity	RAM Capacity	E2 DataFlash	Operating Frequency	Security Function	SDHI	CAN	Operating Temperature
RX231	R5F52315ADLA	R5F52315ADLA#20	PTLG0100KA-A	128 Kbytes	32 Kbytes	8 Kbytes	54 MHz	Not available	Not available	Available	-40 to +85°C
	R5F52315CDLA	R5F52315CDLA#20						Not available	Not available	Not available	
	R5F52315ADFP	R5F52315ADFP#30	PLQP0100KB-B					Not available	Not available	Available	
	R5F52315CDFP	R5F52315CDFP#30						Not available	Not available	Not available	
	R5F52315CDLF	R5F52315CDLF#20	PWLG0064KA-A					Not available	Not available	Not available	
	R5F52315ADND	R5F52315ADND#U0	PWQN0064KC-A					Not available	Not available	Available	
	R5F52315CDND	R5F52315CDND#U0						Not available	Not available	Not available	
	R5F52315ADFM	R5F52315ADFM#30	PLQP0064KB-C					Not available	Not available	Available	
	R5F52315CDFM	R5F52315CDFM#30						Not available	Not available	Not available	
	R5F52315ADNE	R5F52315ADNE#U0	PWQN0048KB-A					Not available	Not available	Available	
	R5F52315CDNE	R5F52315CDNE#U0						Not available	Not available	Not available	
	R5F52315ADFL	R5F52315ADFL#30	PLQP0048KB-B					Not available	Not available	Available	
	R5F52315CDFL	R5F52315CDFL#30						Not available	Not available	Not available	
	RX230	R5F52306ADLA	R5F52306ADLA#20					PTLG0100KA-A	256 Kbytes	32 Kbytes	
R5F52306ADFP		R5F52306ADFP#30	PLQP0100KB-B	Not available	Not available	Not available					
R5F52306ADLF		R5F52306ADLF#20	PWLG0064KA-A	Not available	Not available	Not available					
R5F52306ADND		R5F52306ADND#U0	PWQN0064KC-A	Not available	Not available	Not available					
R5F52306ADFM		R5F52306ADFM#30	PLQP0064KB-C	Not available	Not available	Not available					
R5F52306ADNE		R5F52306ADNE#U0	PWQN0048KB-A	Not available	Not available	Not available					
R5F52306ADFL		R5F52306ADFL#30	PLQP0048KB-B	Not available	Not available	Not available					
R5F52305ADLA		R5F52305ADLA#20	PTLG0100KA-A	128 Kbytes	Not available	Not available	Not available				
R5F52305ADFP		R5F52305ADFP#30	PLQP0100KB-B		Not available	Not available	Not available				
R5F52305ADLF		R5F52305ADLF#20	PWLG0064KA-A		Not available	Not available	Not available				
R5F52305ADND		R5F52305ADND#U0	PWQN0064KC-A		Not available	Not available	Not available				
R5F52305ADFM		R5F52305ADFM#30	PLQP0064KB-C		Not available	Not available	Not available				
R5F52305ADNE		R5F52305ADNE#U0	PWQN0048KB-A		Not available	Not available	Not available				
R5F52305ADFL		R5F52305ADFL#30	PLQP0048KB-B		Not available	Not available	Not available				

Table 1.4 List of Products: G Version (T_a = -40 to +105°C) (1/2)

Group	Part No.	Order Part No.	Package	ROM Capacity	RAM Capacity	E2 DataFlash	Operating Frequency	Security Function	SDHI	CAN	Operating Temperature
RX231	R5F52318AGFP	R5F52318AGFP#30	PLQP0100KB-B	512 Kbytes	64 Kbytes	8 Kbytes	54 MHz	Not available	Not available	Available	-40 to +105°C
	R5F52318BGFP	R5F52318BGFP#30						Available	Available	Available	
	R5F52318AGND	R5F52318AGND#U0	PWQN0064KC-A					Not available	Not available	Available	
	R5F52318BGND	R5F52318BGND#U0						Available	Available	Available	
	R5F52318AGFM	R5F52318AGFM#30	PLQP0064KB-C					Not available	Not available	Available	
	R5F52318BGFM	R5F52318BGFM#30						Available	Available	Available	
	R5F52318AGNE	R5F52318AGNE#U0	PWQN0048KB-A	Not available	Not available	Available					
	R5F52318BGNE	R5F52318BGNE#U0		Available	Available	Available					
	R5F52318AGFL	R5F52318AGFL#30	PLQP0048KB-B	Not available	Not available	Available					
	R5F52318BGFL	R5F52318BGFL#30		Available	Available	Available					
	R5F52317AGFP	R5F52317AGFP#30	PLQP0100KB-B	384 Kbytes	32 Kbytes			Not available	Not available	Available	
	R5F52317BGFP	R5F52317BGFP#30						Available	Available	Available	
	R5F52317AGND	R5F52317AGND#U0	PWQN0064KC-A					Not available	Not available	Available	
	R5F52317BGND	R5F52317BGND#U0						Available	Available	Available	
	R5F52317AGFM	R5F52317AGFM#30	PLQP0064KB-C					Not available	Not available	Available	
	R5F52317BGFM	R5F52317BGFM#30						Available	Available	Available	
	R5F52317AGNE	R5F52317AGNE#U0	PWQN0048KB-A	Not available	Not available	Available					
	R5F52317BGNE	R5F52317BGNE#U0		Available	Available	Available					
	R5F52317AGFL	R5F52317AGFL#30	PLQP0048KB-B	Not available	Not available	Available					
	R5F52317BGFL	R5F52317BGFL#30		Available	Available	Available					
	R5F52316AGFP	R5F52316AGFP#30	PLQP0100KB-B	256 Kbytes	32 Kbytes			Not available	Not available	Available	
	R5F52316CGFP	R5F52316CGFP#30						Not available	Not available	Not available	
	R5F52316AGND	R5F52316AGND#U0	PWQN0064KC-A					Not available	Not available	Available	
	R5F52316CGND	R5F52316CGND#U0						Not available	Not available	Not available	
	R5F52316AGFM	R5F52316AGFM#30	PLQP0064KB-C					Not available	Not available	Available	
	R5F52316CGFM	R5F52316CGFM#30						Not available	Not available	Not available	
	R5F52316AGNE	R5F52316AGNE#U0	PWQN0048KB-A	Not available	Not available	Available					
	R5F52316CGNE	R5F52316CGNE#U0		Not available	Not available	Not available					
	R5F52316AGFL	R5F52316AGFL#30	PLQP0048KB-B	Not available	Not available	Available					
	R5F52316CGFL	R5F52316CGFL#30		Not available	Not available	Not available					
	R5F52315AGFP	R5F52315AGFP#30	PLQP0100KB-B	128 Kbytes				Not available	Not available	Available	
	R5F52315CGFP	R5F52315CGFP#30						Not available	Not available	Not available	
	R5F52315AGND	R5F52315AGND#U0	PWQN0064KC-A					Not available	Not available	Available	
	R5F52315CGND	R5F52315CGND#U0						Not available	Not available	Not available	
	R5F52315AGFM	R5F52315AGFM#30	PLQP0064KB-C					Not available	Not available	Available	
	R5F52315CGFM	R5F52315CGFM#30						Not available	Not available	Not available	
	R5F52315AGNE	R5F52315AGNE#U0	PWQN0048KB-A	Not available	Not available	Available					
	R5F52315CGNE	R5F52315CGNE#U0		Not available	Not available	Not available					
	R5F52315AGFL	R5F52315AGFL#30	PLQP0048KB-B	Not available	Not available	Available					
	R5F52315CGFL	R5F52315CGFL#30		Not available	Not available	Not available					

Table 1.4 List of Products: G Version (T_a = -40 to +105°C) (2/2)

Group	Part No.	Order Part No.	Package	ROM Capacity	RAM Capacity	E2 DataFlash	Operating Frequency	Security Function	SDHI	CAN	Operating Temperature
RX230	R5F52306AGFP	R5F52306AGFP#30	PLQP0100KB-B	256 Kbytes	32 Kbytes	8 Kbytes	54 MHz	Not available	Not available	Not available	-40 to +105°C
	R5F52306AGND	R5F52306AGND#U0	PWQN0064KC-A					Not available	Not available	Not available	
	R5F52306AGFM	R5F52306AGFM#30	PLQP0064KB-C					Not available	Not available	Not available	
	R5F52306AGNE	R5F52306AGNE#U0	PWQN0048KB-A					Not available	Not available	Not available	
	R5F52306AGFL	R5F52306AGFL#30	PLQP0048KB-B					Not available	Not available	Not available	
	R5F52305AGFP	R5F52305AGFP#30	PLQP0100KB-B					128 Kbytes	Not available	Not available	
	R5F52305AGND	R5F52305AGND#U0	PWQN0064KC-A	Not available	Not available	Not available					
	R5F52305AGFM	R5F52305AGFM#30	PLQP0064KB-C	Not available	Not available	Not available					
	R5F52305AGNE	R5F52305AGNE#U0	PWQN0048KB-A	Not available	Not available	Not available					
	R5F52305AGFL	R5F52305AGFL#30	PLQP0048KB-B	Not available	Not available	Not available					

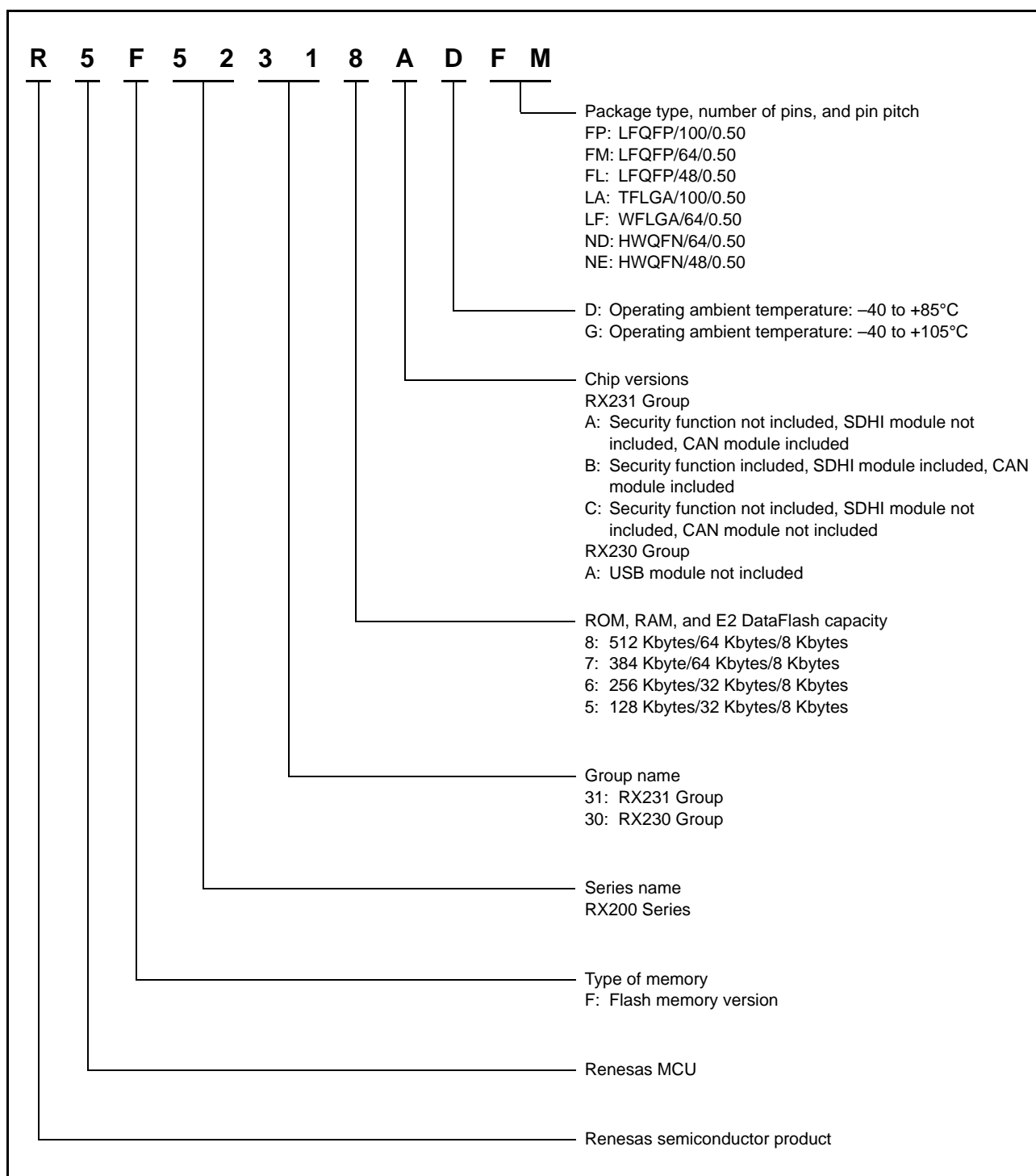


Figure 1.1 How to Read the Product Part Number

1.3 Block Diagram

Figure 1.2 shows a block diagram.

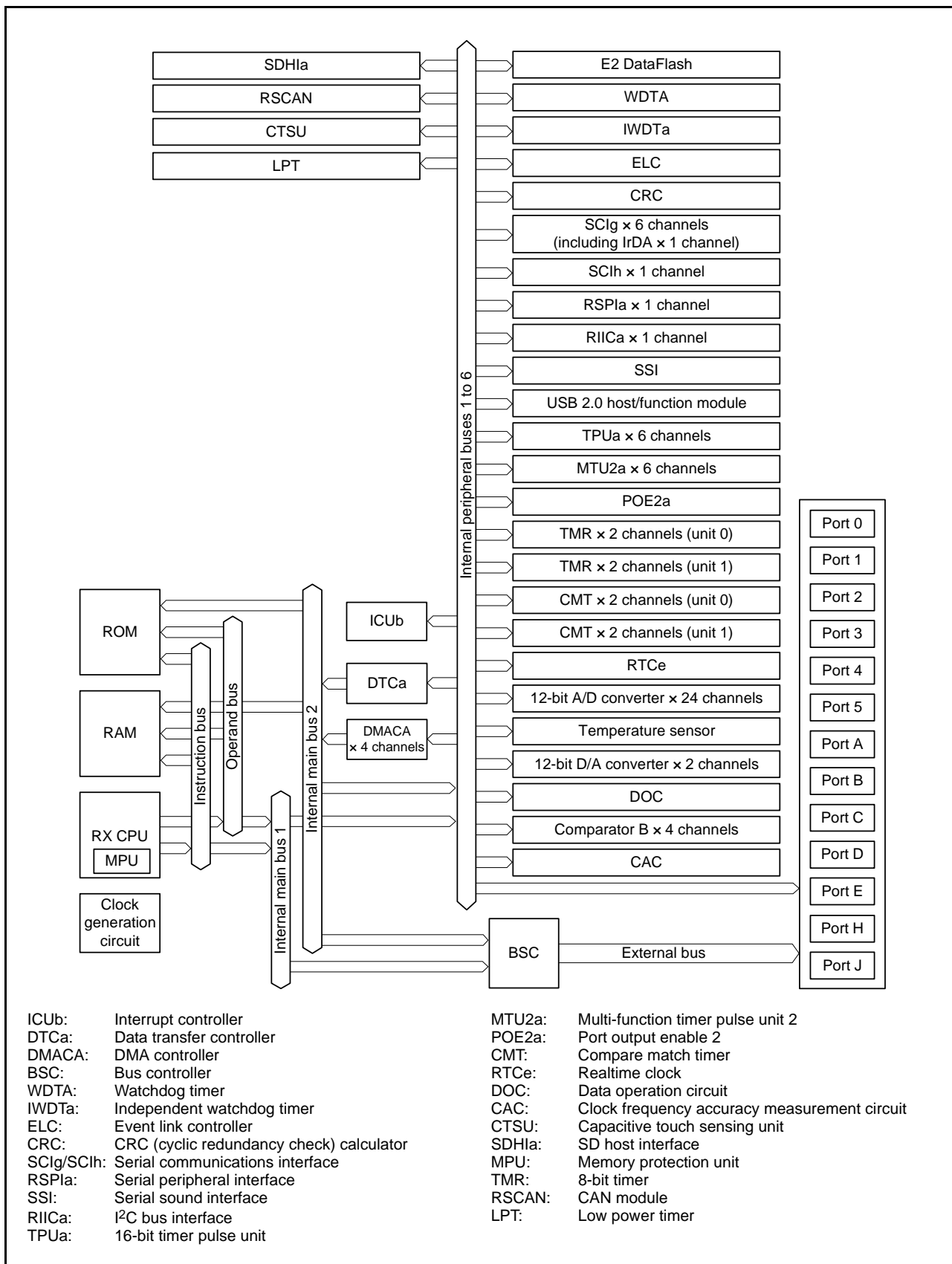


Figure 1.2 Block Diagram

1.4 Pin Functions

Table 1.5 lists the pin functions.

Table 1.5 Pin Functions (1/4)

Classifications	Pin Name	I/O	Description
Power supply	VCC	Input	Power supply pin. Connect it to the system power supply.
	VCL	—	Connect this pin to the VSS pin via the 4.7 μ F smoothing capacitor used to stabilize the internal power supply. Place the capacitor close to the pin.
	VSS	Input	Ground pin. Connect it to the system power supply (0 V).
	VBATT	Input	Backup power pin
Clock	XTAL	Output	Pins for connecting a crystal. An external clock can be input through the EXTAL pin.
	EXTAL	Input	
	BCLK	Output	Outputs the external bus clock for external devices.
	XCIN	Input	Input/output pins for the sub-clock oscillator. Connect a crystal between XCIN and XCOUT.
	XCOUT	Output	
	CLKOUT	Output	Clock output pin.
Operating mode control	MD	Input	Pin for setting the operating mode. The signal levels on this pin must not be changed during operation.
	UB	Input	Pin used for boot mode (USB interface).
	UPSEL	Input	Pin used for boot mode (USB interface).
System control	RES#	Input	Reset pin. This MCU enters the reset state when this signal goes low.
CAC	CACREF	Input	Input pin for the clock frequency accuracy measurement circuit.
On-chip emulator	FINED	I/O	FINE interface pin.
Address bus	A0 to A23	Output	Output pins for the address.
Data bus	D0 to D15	I/O	Input and output pins for the bidirectional data bus.
Multiplexed bus	A0/D0 to A15/D15	I/O	Address/data multiplexed bus
Bus control	RD#	Output	Strobe signal which indicates that reading from the external bus interface space is in progress.
	WR#	Output	Strobe signal which indicates that writing to the external bus interface space is in progress, in single-write strobe mode.
	WR0#, WR1#	Output	Strobe signals which indicate that either group of data bus pins (D7 to D0, and D15 to D8) is valid in writing to the external bus interface space, in byte strobe mode.
	BC0#, BC1#	Output	Strobe signals which indicate that either group of data bus pins (D7 to D0 and D15 to D8) is valid in access to the external bus interface space, in single-write strobe mode.
	CS0# to CS3#	Output	Select signals for areas 0 to 3.
	WAIT#	Input	Input pin for wait request signals in access to the external space.
	ALE	Output	Address latch signal when address/data multiplexed bus is selected.
LVD	CMPA2	Input	Detection target voltage pin for voltage detection 2.
Interrupts	NMI	Input	Non-maskable interrupt request pin.
	IRQ0 to IRQ7	Input	Interrupt request pins.

Table 1.5 Pin Functions (2/4)

Classifications	Pin Name	I/O	Description
16-bit timer pulse unit	TIOCA0, TIOCB0 TIOCC0, TIOCD0	I/O	The TGRA0 to TGRD0 input capture input/output compare output/PWM output pins.
	TIOCA1, TIOCB1	I/O	The TGRA1 and TGRB1 input capture input/output compare output/PWM output pins.
	TIOCA2, TIOCB2	I/O	The TGRA2 and TGRB2 input capture input/output compare output/PWM output pins.
	TIOCA3, TIOCB3 TIOCC3, TIOCD3	I/O	The TGRA3 to TGRD3 input capture input/output compare output/PWM output pins.
	TIOCA4, TIOCB4	I/O	The TGRA4 and TGRB4 input capture input/output compare output/PWM output pins.
	TIOCA5, TIOCB5	I/O	The TGRA5 and TGRB5 input capture input/output compare output/PWM output pins.
	TCLKA, TCLKB TCLKC, TCLKD	Input	Input pins for external clock signals.
Multi-function timer pulse unit 2	MTIOC0A, MTIOC0B MTIOC0C, MTIOC0D	I/O	The TGRA0 to TGRD0 input capture input/output compare output/PWM output pins.
	MTIOC1A, MTIOC1B	I/O	The TGRA1 and TGRB1 input capture input/output compare output/PWM output pins.
	MTIOC2A, MTIOC2B	I/O	The TGRA2 and TGRB2 input capture input/output compare output/PWM output pins.
	MTIOC3A, MTIOC3B MTIOC3C, MTIOC3D	I/O	The TGRA3 to TGRD3 input capture input/output compare output/PWM output pins.
	MTIOC4A, MTIOC4B MTIOC4C, MTIOC4D	I/O	The TGRA4 to TGRD4 input capture input/output compare output/PWM output pins.
	MTIC5U, MTIC5V, MTIC5W	Input	The TGRU5, TGRV5, and TGRW5 input capture input/external pulse input pins.
	MTCLKA, MTCLKB, MTCLKC, MTCLKD	Input	Input pins for the external clock.
Port output enable 2	POE0# to POE3#, POE8#	Input	Input pins for request signals to place the MTU pins in the high impedance state.
Realtime clock	RTCOUT	Output	Output pin for the 1-Hz/64-Hz clock.
	RTCIC0 to RTCIC2	Input	Time capture event input pins.
8-bit timer	TMO0 to TMO3	Output	Compare match output pins.
	TMCI0 to TMCI3	Input	Input pins for the external clock to be input to the counter.
	TMRI0 to TMRI3	Input	Counter reset input pins.
Serial communications interface (SCIg)	<ul style="list-style-type: none"> Asynchronous mode/clock synchronous mode 		
	SCK0, SCK1, SCK5, SCK6, SCK8, SCK9	I/O	Input/output pins for the clock.
	RXD0, RXD1, RXD5, RXD6, RXD8, RXD9	Input	Input pins for received data.
	TXD0, TXD1, TXD5, TXD6, TXD8, TXD9	Output	Output pins for transmitted data.
	CTS0#, CTS1#, CTS5#, CTS6#, CTS8#, CTS9#	Input	Input pins for controlling the start of transmission and reception.
	RTS0#, RTS1#, RTS5#, RTS6#, RTS8#, RTS9#	Output	Output pins for controlling the start of transmission and reception.
	<ul style="list-style-type: none"> Simple I²C mode 		
	SSCL0, SSCL1, SSCL5, SSCL6, SSCL8, SSCL9	I/O	Input/output pins for the I ² C clock.
	SSDA0, SSDA1, SSDA5, SSDA6, SSDA8, SSDA9	I/O	Input/output pins for the I ² C data.

Table 1.5 Pin Functions (3/4)

Classifications	Pin Name	I/O	Description
Serial communications interface (SClg)	• Simple SPI mode		
	SCK0, SCK1, SCK5, SCK6, SCK8, SCK9	I/O	Input/output pins for the clock.
	SMISO0, SMISO1, SMISO5, SMISO6, SMISO8, SMISO9	I/O	Input/output pins for slave transmit data.
	SMOSI0, SMOSI1, SMOSI5, SMOSI6, SMOSI8, SMOSI9	I/O	Input/output pins for master transmit data.
	SS0#, SS1#, SS5#, SS6#, SS8#, SS9#	Input	Slave-select input pins.
IrDA interface	IRTXD5	Output	Data output pin in the IrDA format.
	IRRXD5	Input	Data input pin in the IrDA format.
Serial communications interface (SClh)	• Asynchronous mode/clock synchronous mode		
	SCK12	I/O	Input/output pin for the clock.
	RXD12	Input	Input pin for receiving data.
	TXD12	Output	Output pin for transmitting data.
	CTS12#	Input	Input pin for controlling the start of transmission and reception.
	RTS12#	Output	Output pin for controlling the start of transmission and reception.
	• Simple I ² C mode		
	SSCL12	I/O	Input/output pin for the I ² C clock.
	SSDA12	I/O	Input/output pin for the I ² C data.
	• Simple SPI mode		
	SCK12	I/O	Input/output pin for the clock.
	SMISO12	I/O	Input/output pin for slave transmit data.
	SMOSI12	I/O	Input/output pin for master transmit data.
	SS12#	Input	Slave-select input pin.
	• Extended serial mode		
	RDX12	Input	Input pin for data reception by SCIf.
	TXDX12	Output	Output pin for data transmission by SCIf.
	SIOX12	I/O	Input/output pin for data reception or transmission by SCIf.
	I ² C bus interface	SCL	I/O
SDA		I/O	Input/output pin for I ² C bus interface data. Bus can be directly driven by the N-channel open drain output.
Serial peripheral interface	RSPCKA	I/O	Input/output pin for the RSPI clock.
	MOSIA	I/O	Input/output pin for transmitting data from the RSPI master.
	MISOA	I/O	Input/output pin for transmitting data from the RSPI slave.
	SSLA0	I/O	Input/output pin to select the slave for the RSPI.
	SSLA1 to SSLA3	Output	Output pins to select the slave for the RSPI.
Serial sound interface	SSISCK0	I/O	SSI serial bit clock pin.
	SSIWS0	I/O	Word selection pin.
	SSITXD0	Output	Serial data output pin.
	SSIRXD0	Input	Serial data input pin.
	AUDIO_MCLK	Input	Master clock pin for audio.
CAN module	CRXD0	Input	Input pin
	CTXD0	Output	Output pin
SD host interface	SDHI_CLK	Output	SD clock output pin
	SDHI_CMD	I/O	SD command output, response input signal pin

Table 1.5 Pin Functions (4/4)

Classifications	Pin Name	I/O	Description
SD host interface	SDHI_D3 to SD_D0	I/O	SD data bus pins
	SDHI_CD	Input	SD card detection pin
	SDHI_WP	Input	SD write-protect signal
USB 2.0 host/ function module	VCC_USB	Input	Power supply pin for USB. Connect this pin to VCC.
	VSS_USB	Input	Ground pin for USB. Connect this pin to VSS.
	USB0_DP	I/O	D+ I/O pin of the USB on-chip transceiver.
	USB0_DM	I/O	D- I/O pin of the USB on-chip transceiver.
	USB0_VBUS	Input	USB cable connection monitor pin.
	USB0_EXICEN	Output	Low-power control signal for the OTG chip.
	USB0_VBUSEN	Output	VBUS (5 V) supply enable signal for the OTG chip.
	USB0_OVRCURA, USB0_OVRCURB	Input	External overcurrent detection pins.
12-bit A/D converter	AN000 to AN007, AN016 to AN031	Input	Input pins for the analog signals to be processed by the A/D converter.
	ADTRG0#	Input	Input pin for the external trigger signal that start the A/D conversion.
12-bit D/A converter	DA0, DA1	Output	Analog output pins of the D/A converter.
Comparator B	CMPB0 to CMPB3	Input	Input pin for the analog signal to be processed by comparator B.
	CVREFB0 to CVREFB3	Input	Analog reference voltage supply pin for comparator B.
	CMPOB0 to CMPOB3	Output	Output pin for comparator B.
CTSU	TS0 to TS9, TS12, TS13, TS15 to TS20, TS22, TS23, TS27, TS30, TS33, TS35	Output	Electrostatic capacitance measurement pins (touch pins).
	TSCAP	Output	LPF connection pin.
Analog power supply	AVCC0	Input	Analog voltage supply pin for the 12-bit A/D converter and D/A converter. Connect this pin to VCC when not using the 12-bit A/D converter and D/A converter.
	AVSS0	Input	Analog ground pin for the 12-bit A/D converter and D/A converter. Connect this pin to VSS when not using the 12-bit A/D converter and D/A converter.
	VREFH0	Input	Analog reference voltage supply pin for the 12-bit A/D converter.
	VREFL0	Input	Analog reference ground pin for the 12-bit A/D converter.
	VREFH	Input	Analog reference voltage supply pin for the 12-bit D/A converter.
	VREFL	Input	Analog reference ground pin for the 12-bit D/A converter.
I/O ports	P03, P05, P07	I/O	3-bit input/output pins.
	P12 to P17	I/O	6-bit input/output pins.
	P20 to P27	I/O	8-bit input/output pins.
	P30 to P37	I/O	8-bit input/output pins (P35 input pin).
	P40 to P47	I/O	8-bit input/output pins.
	P50 to P55	I/O	6-bit input/output pins.
	PA0 to PA7	I/O	8-bit input/output pins.
	PB0 to PB7	I/O	8-bit input/output pins.
	PC0 to PC7	I/O	8-bit input/output pins.
	PD0 to PD7	I/O	8-bit input/output pins.
	PE0 to PE7	I/O	8-bit input/output pins.
	PH0 to PH3	I/O	4-bit input/output pins.
	PJ3	I/O	1-bit input/output pin.

1.5 Pin Assignments

Figure 1.3 to Figure 1.9 show the pin assignments. Table 1.6 to Table 1.10 show the lists of pins and pin functions.

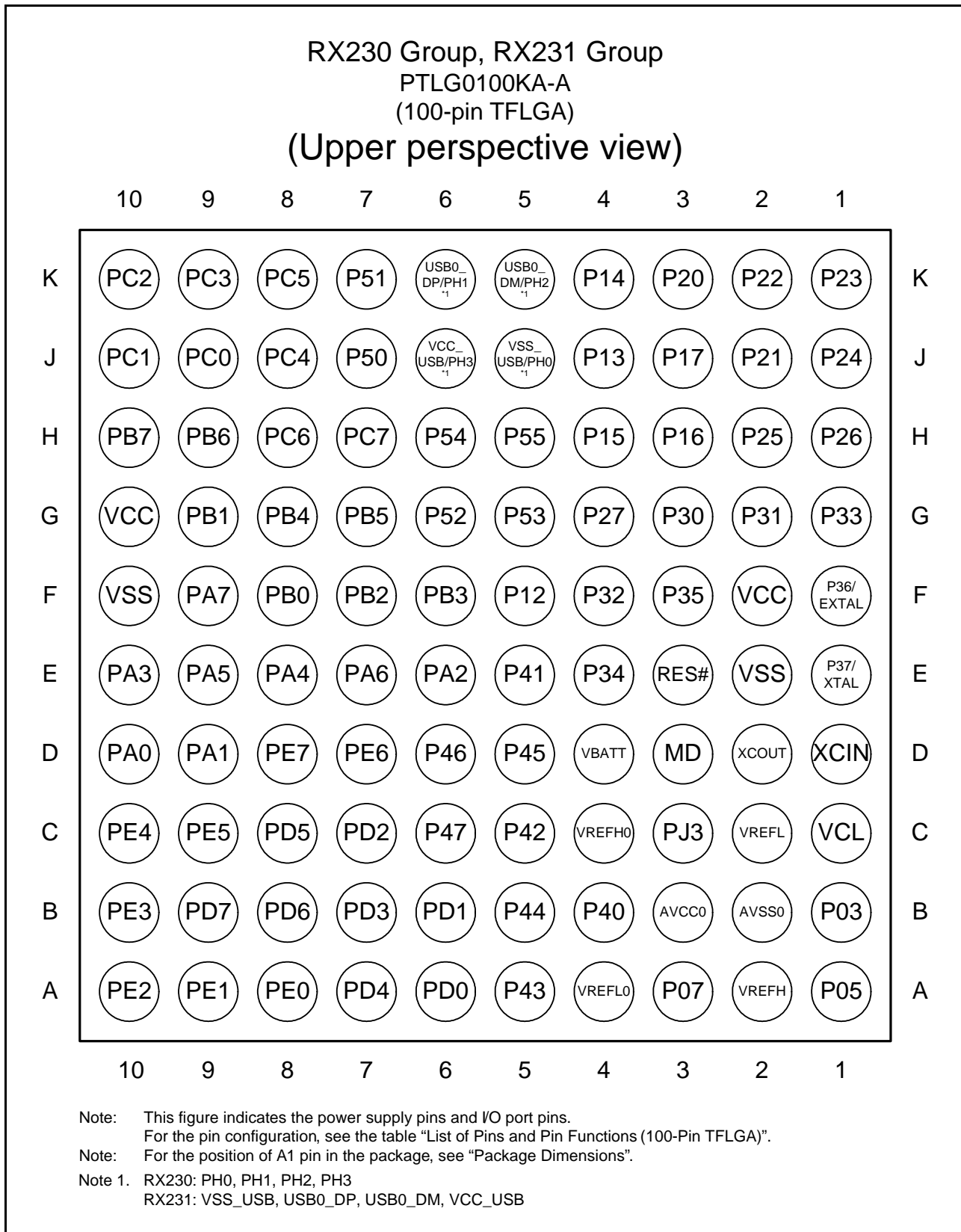


Figure 1.3 Pin Assignments of the 100-Pin TFLGA (Upper Perspective View)

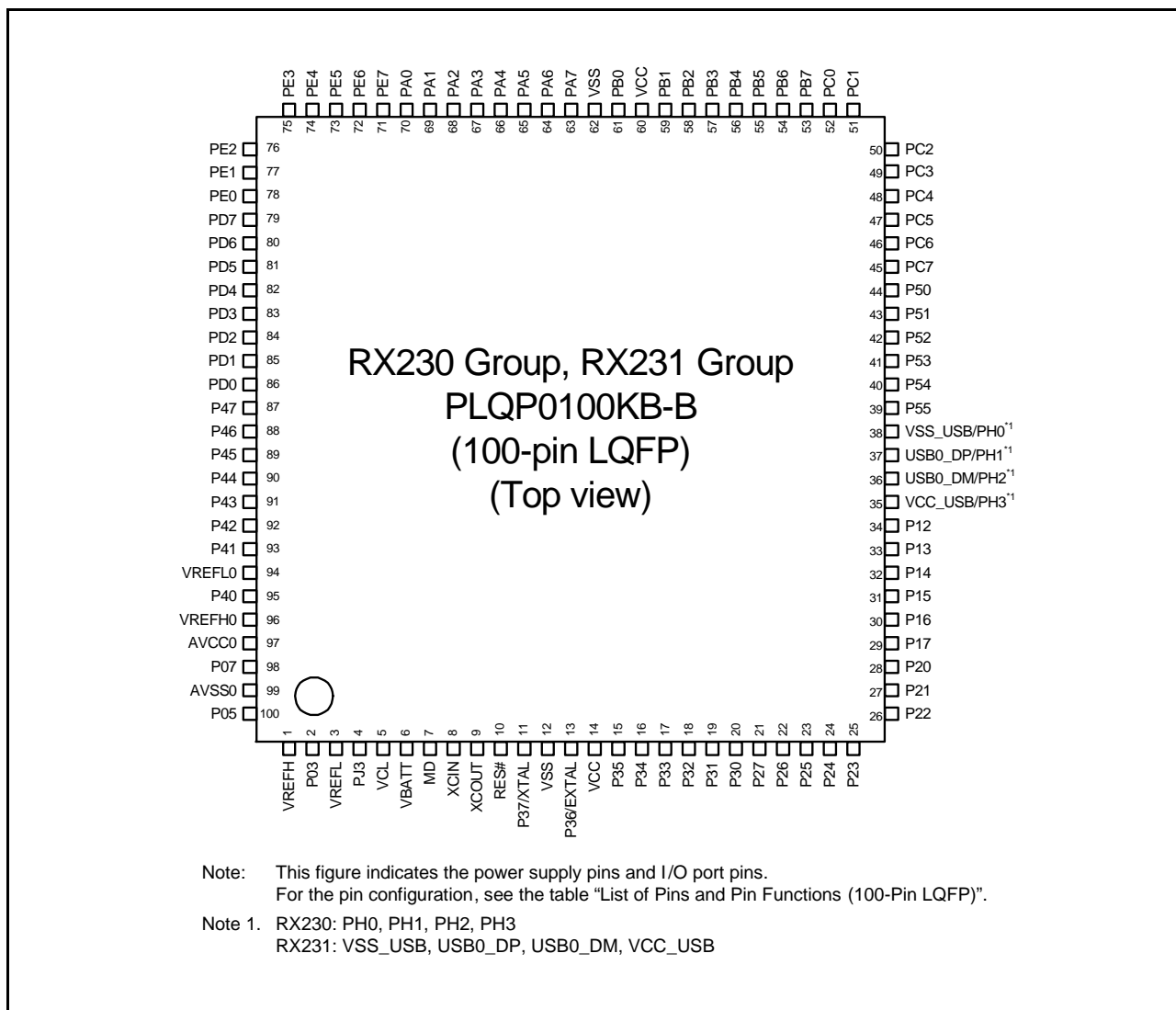


Figure 1.4 Pin Assignments of the 100-Pin LQFP

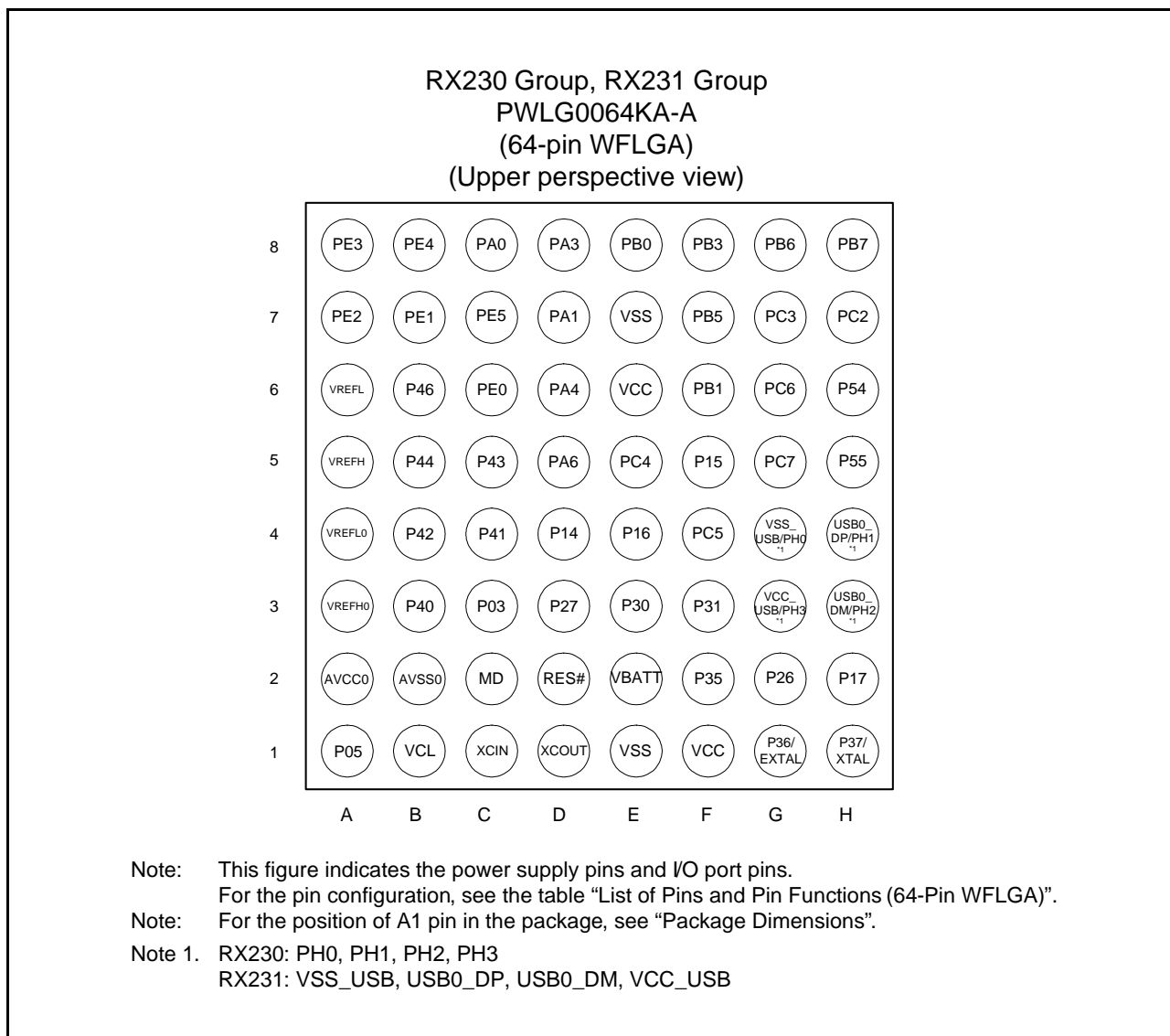


Figure 1.5 Pin Assignments of the 64-Pin WFLGA

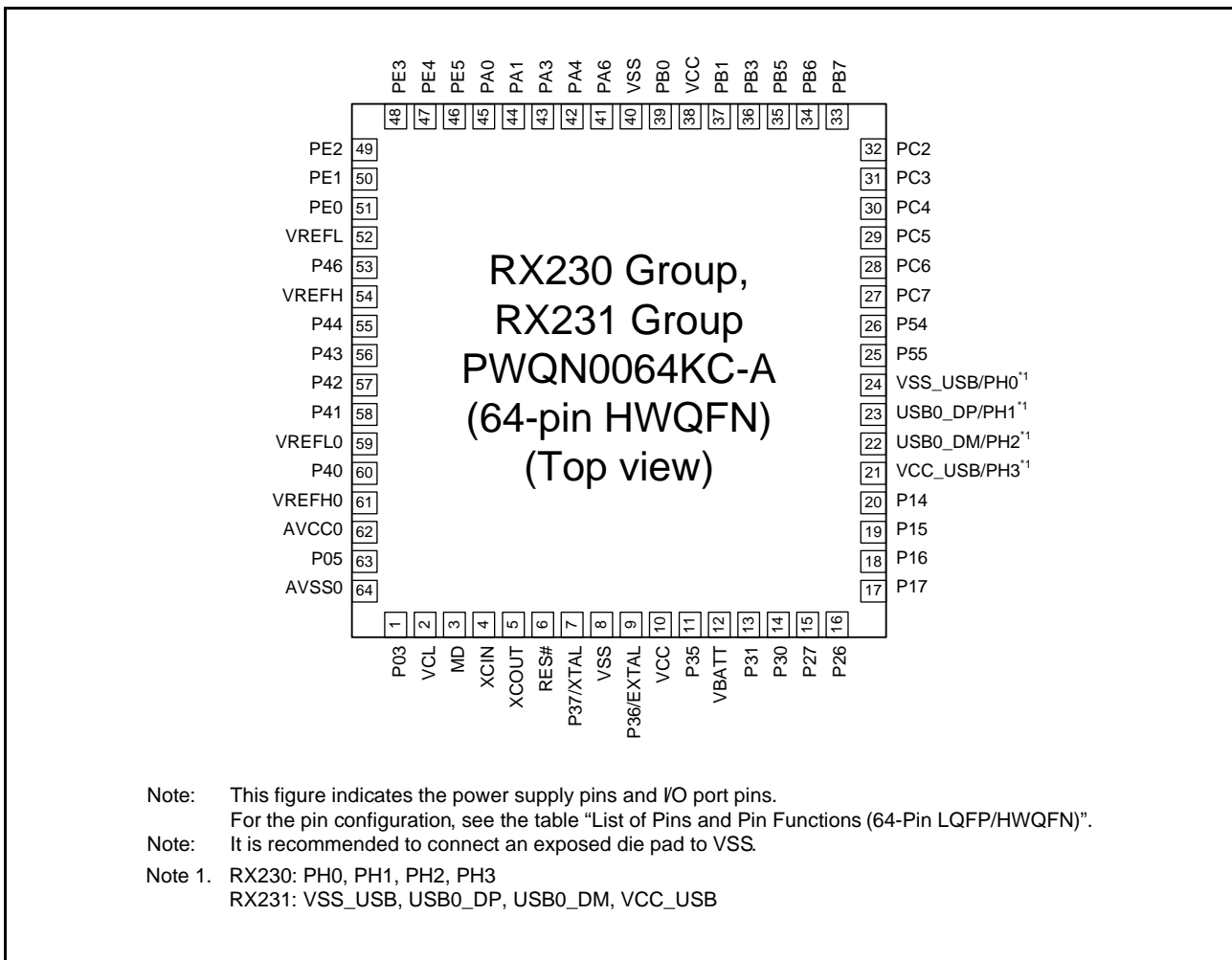


Figure 1.6 Pin Assignments of the 64-Pin HWQFN

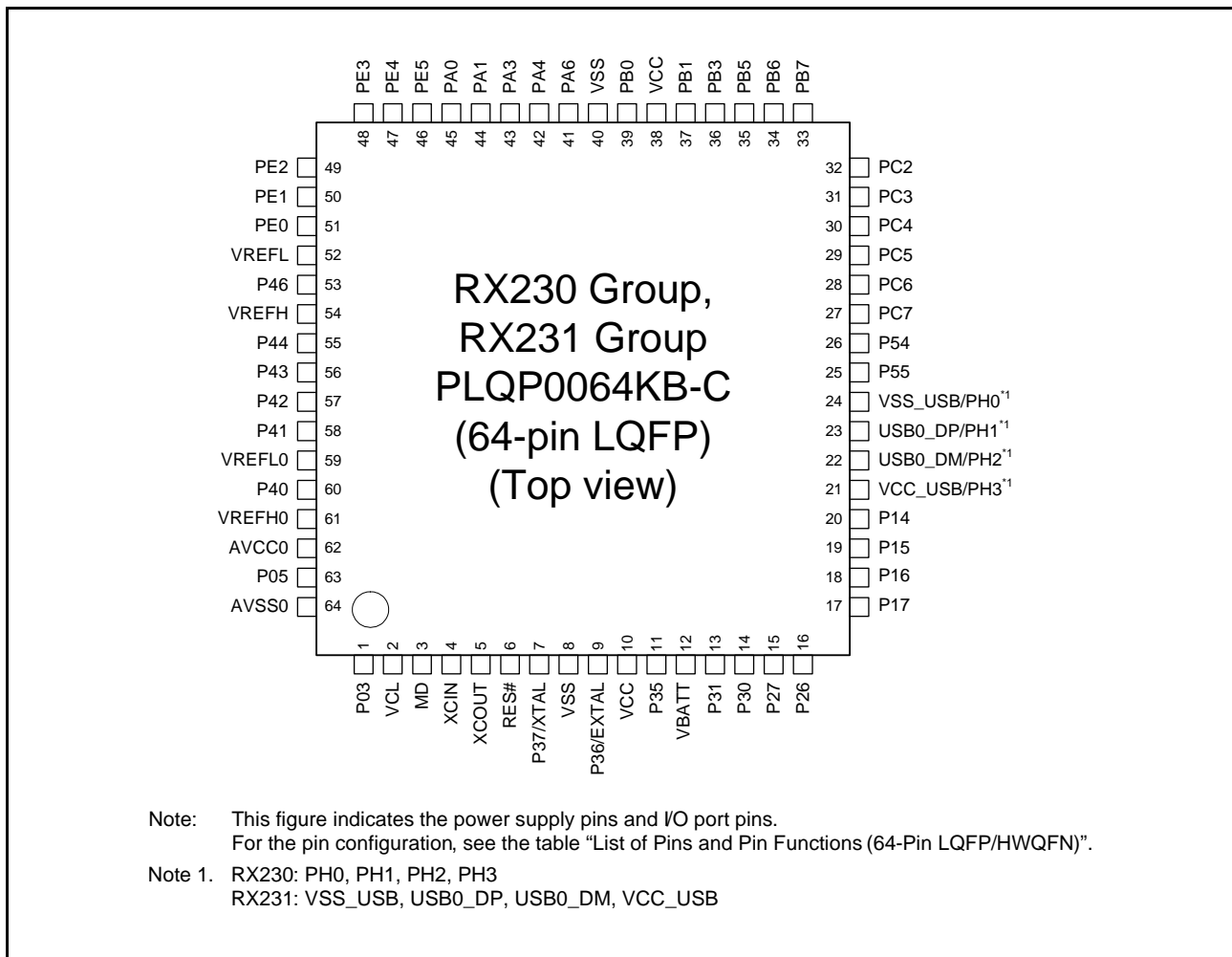


Figure 1.7 Pin Assignments of the 64-Pin LQFP

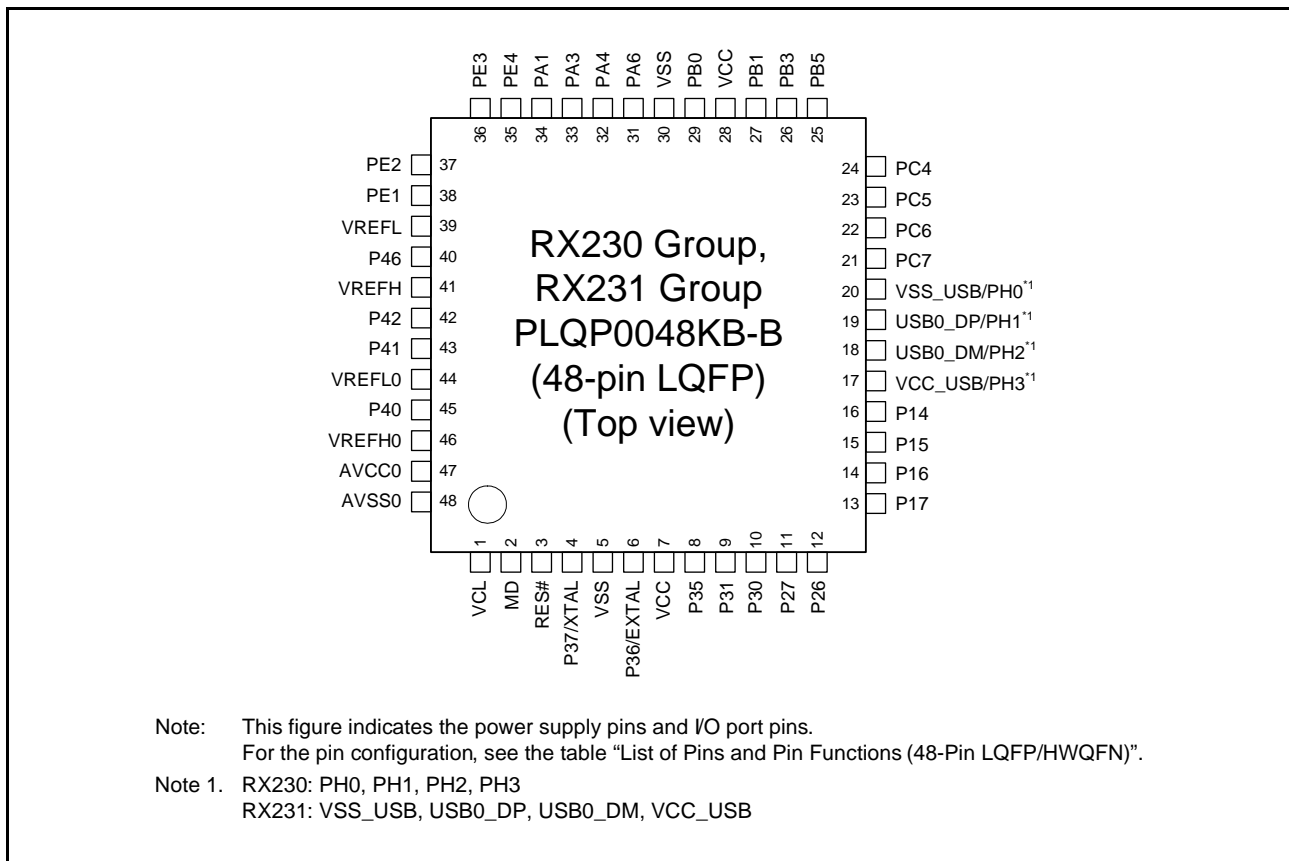


Figure 1.8 Pin Assignments of the 48-Pin LQFP

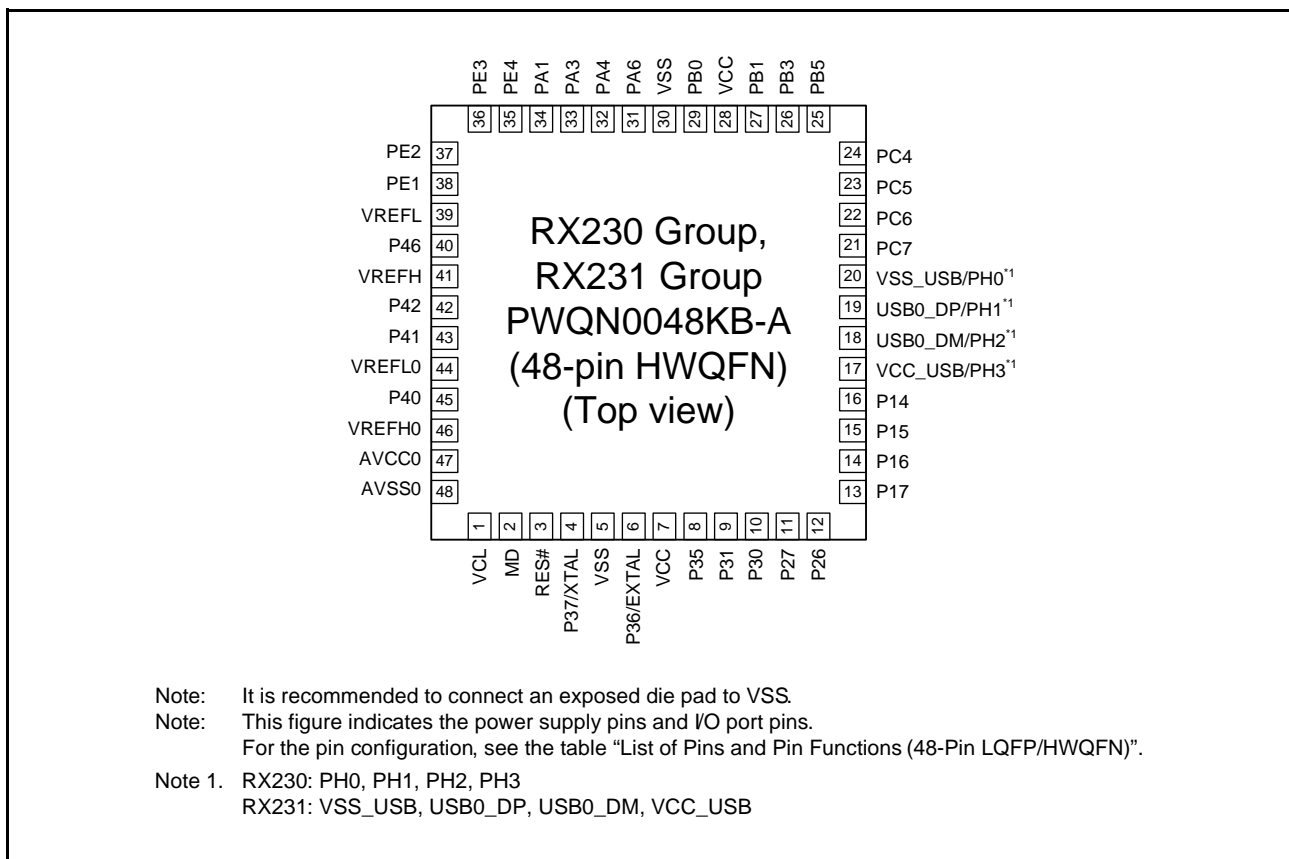


Figure 1.9 Pin Assignments of the 48-Pin HWQFN

Table 1.6 List of Pins and Pin Functions (100-Pin TFLGA) (1/3)

Pin No.	Power Supply, Clock, System Control	I/O Port	External Bus	Timers (MTU, TPU, TMR, RTC, CMT, POE, CAC)	Communications (SCIg, SC1h, RSPI, RIIC, CAN, USB, SSI)	Memory Interface (SDHI)	Touch sensing	Others
A1		P05						DA1
A2	VREFH							
A3		P07						ADTRG0#
A4	VREFL0							
A5		P43						AN003
A6		PD0	D0[A0/D0]					IRQ0/AN024
A7		PD4	D4[A4/D4]	POE3#				IRQ4/AN028
A8		PE0	D8[A8/D8]		SCK12			AN016
A9		PE1	D9[A9/D9]	MTIOC4C	TXD12/TXD12/SIOX12/ SMOS12/SSDA12			AN017/ CMPB0
A10		PE2	D10[A10/D10]	MTIOC4A	RXD12/RXD12/ SMISO12/SSCL12			IRQ7/AN018/ CVREFB0
B1		P03						DA0
B2	AVSS0							
B3	AVCC0							
B4		P40						AN000
B5		P44						AN004
B6		PD1	D1[A1/D1]	MTIOC4B				IRQ1/AN025
B7		PD3	D3[A3/D3]	POE8#				IRQ3/AN027
B8		PD6	D6[A6/D6]	MTIC5V/POE1#				IRQ6/AN030
B9		PD7	D7[A7/D7]	MTIC5U/POE0#				IRQ7/AN031
B10		PE3	D11[A11/D11]	MTIOC4B/POE8#	CTS12#/RTS12#/SS12#/ AUDIO_MCLK			AN019/ CLKOUT
C1	VCL							
C2	VREFL							
C3		PJ3		MTIOC3C	CTS6#/RTS6#/SS6#			
C4	VREFH0							
C5		P42						AN002
C6		P47						AN007
C7		PD2	D2[A2/D2]	MTIOC4D				IRQ2/AN026
C8		PD5	D5[A5/D5]	MTIC5W/POE2#				IRQ5/AN029
C9		PE5	D13[A13/D13]	MTIOC4C/MTIOC2B				IRQ5/AN021/ CMPOB0
C10		PE4	D12[A12/D12]	MTIOC4D/MTIOC1A				AN020/ CMPA2/ CLKOUT
D1	XCIN							
D2	XCOUT							
D3	MD							FINED
D4	VBATT							
D5		P45						AN005
D6		P46						AN006
D7		PE6	D14[A14/D14]					IRQ6/AN022
D8		PE7	D15[A15/D15]					IRQ7/AN023
D9		PA1	A1	MTIOC0B/MTCLKC/ TIOCB0	SCK5/SSLA2/SSISCK0			
D10		PA0	A0/BC0#	MTIOC4A/TIOCA0	SSLA1			CACREF
E1	XTAL	P37						
E2	VSS							
E3	RES#							
E4		P34		MTIOC0A/TMC13/POE2#	SCK6		TS0	IRQ4
E5		P41						AN001
E6		PA2	A2		RXD5/SMISO5/SSCL5/ SSLA3/IRRXD5			
E7		PA6	A6	MTIC5V/MTCLKB/TMC13/ POE2#/TIOCA2	CTS5#/RTS5#/SS5#/ MOSIA/SSIWS0			

Table 1.6 List of Pins and Pin Functions (100-Pin TFLGA) (2/3)

Pin No.	Power Supply, Clock, System Control	I/O Port	External Bus	Timers (MTU, TPU, TMR, RTC, CMT, POE, CAC)	Communications (SCIg, SC1h, RSPI, RIIC, CAN, USB, SSI)	Memory Interface (SDHI)	Touch sensing	Others
E8		PA4	A4	MTIC5U/MTCLKA/TMRI0/TIOCA1	TXD5/SMOSI5/SSDA5/SSLA0/SSITXD0/IRTXD5			IRQ5 / CVREFB1
E9		PA5	A5	TIOCB1	RSPCKA			
E10		PA3	A3	MTIOC0D/MTCLKD/TIOC0D/TCLKB	RXD5/SMISO5/SSCL5/SSIRXD0/IRRXD5			IRQ6 /CMPB1
F1	EXTAL	P36						
F2	VCC							
F3		P35						NMI
F4		P32		MTIOC0C/TMO3/TIOCC0/RTCOUT/RTCIC2	TXD6/SMOSI6/SSDA6/USB0_VBUSEN			IRQ2
F5		P12		TMCI1	SCL			IRQ2
F6		PB3	A11	MTIOC0A/MTIOC4A/TMO0/POE3#/TIOC0D3/TCLKD	SCK6	SDHI_W P		
F7		PB2	A10	TIOCC3/TCLKC	CTS6#/RTS6#/SS6#			
F8		PB0	A8	MTIC5W/TIOCA3	RXD6/SMISO6/SSCL6/RSPCKA	SDHI_C MD		
F9		PA7	A7	TIOCB2	MISOA			
F10	VSS							
G1		P33		MTIOC0D/TMRI3/POE3#/TIOC0D	RXD6/SMISO6/SSCL6		TS1	IRQ3
G2		P31		MTIOC4D/TMCI2/RTCIC1	CTS1#/RTS1#/SS1#/SSISCK0			IRQ1
G3		P30		MTIOC4B/TMRI3/POE8#/RTCIC0	RXD1/SMISO1/SSCL1/AUDIO_MCLK			IRQ0/CMPOB3
G4		P27	CS3#	MTIOC2B/TMCI3	SCK1/ SSIWS0		TS2	CVREFB3
G5	BCLK	P53					TS17	
G6		P52	RD#				TS18	
G7		PB5	A13	MTIOC2A/MTIOC1B/TMRI1#/POE1#/TIOCB4	SCK9	SDHI_CD		
G8		PB4	A12	TIOCA4	CTS9#/RTS9#/SS9#			
G9		PB1	A9	MTIOC0C/MTIOC4C/TMCI0/TIOCB3	TXD6/SMOSI6/SSDA6	SDHI_CL K		IRQ4/CMPOB1
G10	VCC							
H1		P26	CS2#	MTIOC2A/TMO1	TXD1/SMOSI1/SSDA1/SSIRXD0		TS3	CMPB3
H2		P25	CS1#	MTIOC4C/MTCLKB/TIOCA4			TS4	ADTRG0#
H3		P16		MTIOC3C/MTIOC3D/TMO2/TIOCB1/TCLKC/RTCOUT	TXD1/SMOSI1/SSDA1/MOSIA/SCL USB0_VBUS/ USB0_VBUSEN/ USB0_OVRCURB			IRQ6/ADTRG0#
H4		P15		MTIOC0B/MTCLKB/TMCI2/TIOCB2/TCLKB	RXD1/SMISO1/SSCL1/CRXD0		TS12	IRQ5/CMPB2
H5		P55	WAIT#	MTIOC4D/TMO3	CRXD0		TS15	
H6		P54	ALE	MTIOC4B/TMCI1	CTXD0		TS16	
H7	UB	PC7	A23/CS0#	MTIOC3A/MTCLKB/TMO2	TXD8/SMOSI8/SSDA8/MISOA			CACREF
H8		PC6	A22/CS1#	MTIOC3C/MTCLKA/TMCI2	RXD8/SMISO8/SSCL8/MOSIA		TS22	
H9		PB6	A14	MTIOC3D/TIOCA5	RXD9/SMISO9/SSCL9	SDHI_D1		
H10		PB7	A15	MTIOC3B/TIOCB5	TXD9/SMOSI9/SSDA9	SDHI_D2		
J1		P24	CS0#	MTIOC4A/MTCLKA/TMRI1/TIOCB4	USB0_VBUSEN		TS5	
J2		P21		MTIOC1B/TMCI0/TIOCA3	RXD0/SMISO0/SSCL0/USB0_EXICEN/SSIWS0		TS8	
J3		P17		MTIOC3A/MTIOC3B/TMO1/POE8#/TIOCB0/TCLKD	SCK1/MISOA/SDA/SSITXD0			IRQ7/CMPOB2
J4		P13		MTIOC0B/TMO3/TIOCA5	SDA			IRQ3
J5	VSS_USB*1	PH0*1						CACREF*1

Table 1.6 List of Pins and Pin Functions (100-Pin TFLGA) (3/3)

Pin No.	Power Supply, Clock, System Control	I/O Port	External Bus	Timers (MTU, TPU, TMR, RTC, CMT, POE, CAC)	Communications (SCIg, SC1h, RSPI, RIIC, CAN, USB, SSI)	Memory Interface (SDHI)	Touch sensing	Others
J6	VCC_USB*1	PH3*1		TMCI0*1				
J7		P50	WR0#/WR#				TS20	
J8		PC4	A20/CS3#	MTIOC3D/MTCLKC/TMCI1/POE0#	SCK5/CTS8#/RTS8#/SS8#/SSLA0	SDHI_D1	TSCAP	
J9		PC0	A16	MTIOC3C/TCLKC	CTS5#/RTS5#/SS5#/SSLA1		TS35	
J10		PC1	A17	MTIOC3A/TCLKD	SCK5/SSLA2		TS33	
K1		P23		MTIOC3D/MTCLKD/TIOCD3	CTS0#/RTS0#/SS0#/SSISCK0		TS6	
K2		P22		MTIOC3B/MTCLKC/TMO0/TIOCC3	SCK0/USB0_OVRCURB/AUDIO_MCLK		TS7	
K3		P20		MTIOC1A/TMRI0/TIOCB3	TXD0/SMOSI0/SSDA0/USB0_ID/SSIRXD0		TS9	
K4		P14		MTIOC3A/MTCLKA/TMRI2/TIOCB5/TCLKA	CTS1#/RTS1#/SS1#/CTXD0/USB0_OVRCURA		TS13	IRQ4/ CVREFB2
K5		PH2*1		TMRI0*1	USB0_DM*1			IRQ1*1
K6		PH1*1		TMO0*1	USB0_DP*1			IRQ0*1
K7		P51	WR1#/BC1#/ WAIT#				TS19	
K8		PC5	A21/CS2#/ WAIT#	MTIOC3B/MTCLKD/TMRI2	SCK8/RSPCKA		TS23	
K9		PC3	A19	MTIOC4D/TCLKB	TXD5/SMOSI5/SSDA5/IRTXD5	SDHI_D0	TS27	
K10		PC2	A18	MTIOC4B/TCLKA	RXD5/SMISO5/SSCL5/SSLA3/IRRXD5	SDHI_D3	TS30	

Note 1. RX230: PH0/CACREF, PH1/IRQ0/TMO0, PH2/IRQ1/TMRI0, PH3/TMCI0
RX231: VSS_USB, USB0_DP, USB0_DM, VCC_USB

Table 1.7 List of Pins and Pin Functions (100-Pin LQFP) (1/3)

Pin No.	Power Supply, Clock, System Control	I/O Port	External Bus	Timers (MTU, TPU, TMR, RTC, CMT, POE, CAC)	Communications (SCIg, SClh, RSPI, RIIC, CAN, USB, SSI)	Memory Interface (SDHI)	Touch sensing	Others
1	VREFH							
2		P03						DA0
3	VREFL							
4		PJ3		MTIOC3C	CTS6#/RTS6#/SS6#			
5	VCL							
6	VBATT							
7	MD							FINED
8	XCIN							
9	XCOUT							
10	RES#							
11	XTAL	P37						
12	VSS							
13	EXTAL	P36						
14	VCC							
15		P35						NMI
16		P34		MTIOC0A/TMCI3/POE2#	SCK6		TS0	IRQ4
17		P33		MTIOC0D/TMRI3/POE3#/TIOC0D	RXD6/SMISO6/SSCL6		TS1	IRQ3
18		P32		MTIOC0C/TMO3/TIOCC0/RTCOUT/RTCIC2	TXD6/SMOSI6/SSDA6/USB0_VBUSEN			IRQ2
19		P31		MTIOC4D/TMCI2/RTCIC1	CTS1#/RTS1#/SS1#/SSISCK0			IRQ1
20		P30		MTIOC4B/TMRI3/POE8#/RTCIC0	RXD1/SMISO1/SSCL1/AUDIO_MCLK			IRQ0/ CMPOB3
21		P27	CS3#	MTIOC2B/TMCI3	SCK1/ SSIWS0		TS2	CVREFB3
22		P26	CS2#	MTIOC2A/TMO1	TXD1/SMOSI1/SSDA1/SSIRXD0		TS3	CMPB3
23		P25	CS1#	MTIOC4C/MTCLKB/TIOCA4			TS4	ADTRG0#
24		P24	CS0#	MTIOC4A/MTCLKA/TMRI1/TIOCB4	USB0_VBUSEN		TS5	
25		P23		MTIOC3D/MTCLKD/TIOCD3	CTS0#/RTS0#/SS0#/SSISCK0		TS6	
26		P22		MTIOC3B/MTCLKC/TMO0/TIOCC3	SCK0/ USB0_OVRCURB/AUDIO_MCLK		TS7	
27		P21		MTIOC1B/TMCI0/TIOCA3	RXD0/SMISO0/SSCL0/USB0_EXICEN/SSIWS0		TS8	
28		P20		MTIOC1A/TMRI0/TIOCB3	TXD0/SMOSI0/SSDA0/USB0_ID/SSIRXD0		TS9	
29		P17		MTIOC3A/MTIOC3B/TMO1/POE8#/TIOCB0/TCLKD	SCK1/MISOA/SDA/SSITXD0			IRQ7/ CMPOB2
30		P16		MTIOC3C/MTIOC3D/TMO2/TIOCB1/TCLKC/RTCOUT	TXD1/SMOSI1/SSDA1/MOSIA/SCL/USB0_VBUS/USB0_VBUSEN/USB0_OVRCURB			IRQ6/ ADTRG0#
31		P15		MTIOC0B/MTCLKB/TMCI2/TIOCB2/TCLKB	RXD1/SMISO1/SSCL1/CRXD0		TS12	IRQ5/CMPB2
32		P14		MTIOC3A/MTCLKA/TMRI2/TIOCB5/TCLKA	CTS1#/RTS1#/SS1#/CTXD0/USB0_OVRCURA		TS13	IRQ4/ CVREFB2
33		P13		MTIOC0B/TMO3/TIOCA5	SDA			IRQ3
34		P12		TMCI1	SCL			IRQ2
35	VCC_USB*1	PH3*1		TMCI0*1				
36		PH2*1		TMRI0*1	USB0_DM*1			IRQ1*1
37		PH1*1		TMO0*1	USB0_DP*1			IRQ0*1
38	VSS_USB*1	PH0*1						CACREF*1
39		P55	WAIT#	MTIOC4D/TMO3	CRXD0		TS15	
40		P54	ALE	MTIOC4B/TMCI1	CTXD0		TS16	
41	BCLK	P53					TS17	

Table 1.7 List of Pins and Pin Functions (100-Pin LQFP) (2/3)

Pin No.	Power Supply, Clock, System Control	I/O Port	External Bus	Timers (MTU, TPU, TMR, RTC, CMT, POE, CAC)	Communications (SCIg, SC1h, RSPI, RIIC, CAN, USB, SSI)	Memory Interface (SDHI)	Touch sensing	Others
42		P52	RD#				TS18	
43		P51	WR1#/BC1#/ WAIT#				TS19	
44		P50	WR0#/WR#				TS20	
45	UB	PC7	A23/CS0#	MTIOC3A/MTCLKB/TMO2	TXD8/SMOSI8/SSDA8/ MISOA			CACREF
46		PC6	A22/CS1#	MTIOC3C/MTCLKA/TMC12	RXD8/SMISO8/SSCL8/ MOSIA		TS22	
47		PC5	A21/CS2#/ WAIT#	MTIOC3B/MTCLKD/TMRI2	SCK8/RSPCKA		TS23	
48		PC4	A20/CS3#	MTIOC3D/MTCLKC/TMC11/ POE0#	SCK5/CTS8#/RTS8#/ SS8#/SSLA0	SDHI_D1	TSCAP	
49		PC3	A19	MTIOC4D/TCLKB	TXD5/SMOSI5/SSDA5/ IRTXD5	SDHI_D0	TS27	
50		PC2	A18	MTIOC4B/TCLKA	RXD5/SMISO5/SSCL5/ SSLA3/ IRRXD5	SDHI_D3	TS30	
51		PC1	A17	MTIOC3A/TCLKD	SCK5/SSLA2		TS33	
52		PC0	A16	MTIOC3C/TCLKC	CTS5#/RTS5#/SS5#/ SSLA1		TS35	
53		PB7	A15	MTIOC3B/TIOCB5	TXD9/SMOSI9/SSDA9	SDHI_D2		
54		PB6	A14	MTIOC3D/TIOCA5	RXD9/SMISO9/SSCL9	SDHI_D1		
55		PB5	A13	MTIOC2A/MTIOC1B/ TMRI1/POE1#/TIOCB4	SCK9/USB0_VBUS	SDHI_CD		
56		PB4	A12	TIOCA4	CTS9#/RTS9#/SS9#			
57		PB3	A11	MTIOC0A/MTIOC4A/TMO0/ POE3#/TIOC3D/TCLKD	SCK6	SDHI_W P		
58		PB2	A10	TIOCC3/TCLKC	CTS6#/RTS6#/SS6#			
59		PB1	A9	MTIOC0C/MTIOC4C/ TMC10/TIOCB3	TXD6/SMOSI6/SSDA6	SDHI_CL K		IRQ4/ CMPOB1
60	VCC							
61		PB0	A8	MTIC5W/TIOCA3	RXD6/SMISO6/SSCL6/ RSPCKA	SDHI_C MD		
62	VSS							
63		PA7	A7	TIOCB2	MISOA			
64		PA6	A6	MTIC5V/MTCLKB/TMC13/ POE2#/TIOCA2	CTS5#/RTS5#/SS5#/ MOSIA/SSIWS0			
65		PA5	A5	TIOCB1	RSPCKA			
66		PA4	A4	MTIC5U/MTCLKA/TMRI0/ TIOCA1	TXD5/SMOSI5/SSDA5/ SSLA0/SSITXD0/IRTXD5			IRQ5 / CVREFB1
67		PA3	A3	MTIOC0D/MTCLKD/ TIOC0D/TCLKB	RXD5/SMISO5/SSCL5/ SSIRXD0/IRRXD5			IRQ6 /CMPB1
68		PA2	A2		RXD5/SMISO5/SSCL5/ SSLA3/IRRXD5			
69		PA1	A1	MTIOC0B/MTCLKC/ TIOCB0	SCK5/SSLA2/SSISCK0			
70		PA0	A0/BC0#	MTIOC4A/TIOCA0	SSLA1			CACREF
71		PE7	D15[A15/D15]					IRQ7/AN023
72		PE6	D14[A14/D14]					IRQ6/AN022
73		PE5	D13[A13/D13]	MTIOC4C/MTIOC2B				IRQ5/AN021/ CMPOB0
74		PE4	D12[A12/D12]	MTIOC4D/MTIOC1A				AN020/ CMPA2/ CLKOUT
75		PE3	D11[A11/D11]	MTIOC4B/POE8#	CTS12#/RTS12#/SS12#/ AUDIO_MCLK			AN019/ CLKOUT
76		PE2	D10[A10/D10]	MTIOC4A	RXD12/RXDX12/ SMISO12/SSCL12			IRQ7/AN018/ CVREFB0
77		PE1	D9[A9/D9]	MTIOC4C	TXD12/TXDX12/SIOX12/ SMOSI12/SSDA12			AN017/ CMPB0
78		PE0	D8[A8/D8]		SCK12			AN016

Table 1.7 List of Pins and Pin Functions (100-Pin LQFP) (3/3)

Pin No.	Power Supply, Clock, System Control	I/O Port	External Bus	Timers (MTU, TPU, TMR, RTC, CMT, POE, CAC)	Communications (SCIg, SC1h, RSPI, RIIC, CAN, USB, SSI)	Memory Interface (SDHI)	Touch sensing	Others
79		PD7	D7[A7/D7]	MTIC5U/POE0#				IRQ7/AN031
80		PD6	D6[A6/D6]	MTIC5V/POE1#				IRQ6/AN030
81		PD5	D5[A5/D5]	MTIC5W/POE2#				IRQ5/AN029
82		PD4	D4[A4/D4]	POE3#				IRQ4/AN028
83		PD3	D3[A3/D3]	POE8#				IRQ3/AN027
84		PD2	D2[A2/D2]	MTIOC4D				IRQ2/AN026
85		PD1	D1[A1/D1]	MTIOC4B				IRQ1/AN025
86		PD0	D0[A0/D0]					IRQ0/AN024
87		P47						AN007
88		P46						AN006
89		P45						AN005
90		P44						AN004
91		P43						AN003
92		P42						AN002
93		P41						AN001
94	VREFL0							
95		P40						AN000
96	VREFH0							
97	AVCC0							
98		P07						ADTRG0#
99	AVSS0							
100		P05						DA1

Note 1. RX230: PH0/CACREF, PH1/IRQ0/TMO0, PH2/IRQ1/TMRI0, PH3/TMC10
RX231: VSS_USB, USB0_DP, USB0_DM, VCC_USB

Table 1.8 List of Pins and Pin Functions (64-Pin WFLGA) (1/2)

Pin No.	Power Supply, Clock, System Control	I/O Port	Timers (MTU, TPU, TMR, RTC, CMT, POE, CAC)	Communications (SClg, SClh, RSPI, RIIC, CAN, USB, SSI)	Memory Interface (SDHI)	Touch sensing	Others
A1		P05					DA1
A2	AVCC0						
A3	VREFH0						
A4	VREFL0						
A5	VREFH						
A6	VREFL						
A7		PE2	MTIOC4A	RXD12/RXD12/SMISO12/SSCL12			IRQ7/AN018/ CVREFB0
A8		PE3	MTIOC4B/POE8#	CTS12#/RTS12#/SS12#/AUDIO_MCLK			AN019/CLKOUT
B1	VCL						
B2	AVSS0						
B3		P40					AN000
B4		P42					AN002
B5		P44					AN004
B6		P46					AN006
B7		PE1	MTIOC4C	TXD12/TXD12/SIOX12/SMOSI12/SSDA12			AN017/CMPB0
B8		PE4	MTIOC4D/MTIOC1A				AN020/CMPA2/ CLKOUT
C1	XCIN						
C2	MD						FINED
C3		P03					DA0
C4		P41					AN001
C5		P43					AN003
C6		PE0		SCK12			AN016
C7		PE5	MTIOC4C/MTIOC2B				IRQ5/AN021/ CMPOB0
C8		PA0	MTIOC4A/TIOCA0	SSLA1			CACREF
D1	XCOU						
D2	RES#						
D3		P27	MTIOC2B/TMCI3	SCK1/ SSIWS0		TS2	CVREFB3
D4		P14	MTIOC3A/MTCLKA/TMRI2/TIOCB5/TCLKA	CTS1#/RTS1#/SS1#/CTXD0/USB0_OVRCURA		TS13	IRQ4/CVREFB2
D5		PA6	MTIC5V/MTCLKB/TMCI3/POE2#/TIOCA2	CTS5#/RTS5#/SS5#/MOSIA/SSIWS0			
D6		PA4	MTIC5U/MTCLKA/TMRI0/TIOCA1	TXD5/SMOSI5/SSDA5/SSLA0/SSITXD0/IRTXD5			IRQ5 /CVREFB1
D7		PA1	MTIOC0B/MTCLKC/TIOCB0	SCK5/SSLA2/SSISCK0			
D8		PA3	MTIOC0D/MTCLKD/TIOCD0/TCLKB	RXD5/SMISO5/SSCL5/SSIRXD0/IRRXD5			IRQ6 /CMPB1
E1	VSS						
E2	VBATT						
E3		P30	MTIOC4B/TMRI3/POE8#/RTCIC0	RXD1/SMISO1/SSCL1/AUDIO_MCLK			IRQ0/CMPOB3
E4		P16	MTIOC3C/MTIOC3D/TMO2/TIOCB1/TCLKC/RTCOU	TXD1/SMOSI1/SSDA1/MOSIA/SCL/USB0_VBUS/USB0_VBUSEN/USB0_OVRCURB			IRQ6/ADTRG0#
E5		PC4	MTIOC3D/MTCLKC/TMCI1/POE0#	SCK5/CTS8#/RTS8#/SS8#/SSLA0	SDHI_D1	TSCAP	
E6	VCC						
E7	VSS						
E8		PB0	MTIC5W/TIOCA3	RXD6/SMISO6/SSCL6/RSPCKA	SDHI_C MD		
F1	VCC						
F2		P35					NMI
F3		P31	MTIOC4D/TMCI2/RTCIC1	CTS1#/RTS1#/SS1#/SSISCK0			IRQ1

Table 1.8 List of Pins and Pin Functions (64-Pin WFLGA) (2/2)

Pin No.	Power Supply, Clock, System Control	I/O Port	Timers (MTU, TPU, TMR, RTC, CMT, POE, CAC)	Communications (SClg, SClh, RSPI, RIIC, CAN, USB, SSI)	Memory Interface (SDHI)	Touch sensing	Others
F4		PC5	MTIOC3B/MTCLKD/TMRI2	SCK8/RSPCKA/USB0_ID			TS23
F5		P15	MTIOC0B/MTCLKB/TMCI2/TIOC2/TCLKB	RXD1/SMISO1/SSCL1/CRXD0		TS12	IRQ5/CMPB2
F6		PB1	MTIOC0C/MTIOC4C/TMCI0/TIOC3	TXD6/SMOSI6/SSDA6	SDHI_CLK		IRQ4/CMPOB1
F7		PB5	MTIOC2A/MTIOC1B/TMRI1/POE1#/TIOC4	SCK9	SDHI_CD		
F8		PB3	MTIOC0A/MTIOC4A/TMO0/POE3#/TIOC3/TCLKD	SCK6	SDHI_WP		
G1	EXTAL	P36					
G2		P26	MTIOC2A/TMO1	TXD1/SMOSI1/SSDA1/USB0_VBUSEN/SSIRXD0		TS3	CMPB3
G3	VCC_USB*1	PH3*1	TMCI0*1				
G4	VSS_USB*1	PH0*1					CACREF*1
G5	UB	PC7	MTIOC3A/MTCLKB/TMO2	TXD8/SMOSI8/SSDA8/MISOA			CACREF
G6		PC6	MTIOC3C/MTCLKA/TMCI2	RXD8/SMISO8/SSCL8/MOSIA/USB0_EXICEN		TS22	
G7		PC3	MTIOC4D/TCLKB	TXD5/SMOSI5/SSDA5/RTXD5	SDHI_D0	TS27	
G8		PB6/PC0	MTIOC3D/TIOCA5	RXD9/SMISO9/SSCL9	SDHI_D1		
H1	XTAL	P37					
H2		P17	MTIOC3A/MTIOC3B/TMO1/POE8#/TIOC3/TCLKD	SCK1/MISOA/SDA/SSITXD0			IRQ7/CMPOB2
H3		PH2*1	TMRI0*1	USB0_DM*1			IRQ1*1
H4		PH1*1	TMO0*1	USB0_DP*1			IRQ0*1
H5		P55	MTIOC4D/TMO3	CRXD0		TS15	
H6		P54	MTIOC4B/TMCI1	CTXD0		TS16	
H7		PC2	MTIOC4B/TCLKA	RXD5/SMISO5/SSCL5/SSLA3/IRRXD5	SDHI_D3	TS30	
H8		PB7/PC1	MTIOC3B/TIOC3	TXD9/SMOSI9/SSDA9	SDHI_D2		

Note 1. RX230: PH0/CACREF, PH1/IRQ0/TMO0, PH2/IRQ1/TMRI0, PH3/TMCI0
 RX231: VSS_USB, USB0_DP, USB0_DM, VCC_USB

Table 1.9 List of Pins and Pin Functions (64-Pin LQFP/HWQFN) (1/2)

Pin No.	Power Supply, Clock, System Control	I/O Port	Timers (MTU, TPU, TMR, RTC, CMT, POE, CAC)	Communications (SClg, SCih, RSPI, RIIC, CAN, USB, SSI)	Memory Interface (SDHI)	Touch sensing	Others
1		P03					DA0
2	VCL						
3	MD						FINED
4	XCIN						
5	XCOU						
6	RES#						
7	XTAL	P37					
8	VSS						
9	EXTAL	P36					
10	VCC						
11		P35					NMI
12	VBATT						
13		P31	MTIOC4D/TMCI2/RTCIC1	CTS1#/RTS1#/SS1#/SSISCK0			IRQ1
14		P30	MTIOC4B/TMRI3/POE8#/RTCIC0	RXD1/SMISO1/SSCL1/AUDIO_MCLK			IRQ0/CMPOB3
15		P27	MTIOC2B/TMCI3	SCK1/SSIWS0		TS2	CVREFB3
16		P26	MTIOC2A/TMO1	TXD1/SMOSI1/SSDA1/USB0_VBUSEN/SSIRXD0		TS3	CMPB3
17		P17	MTIOC3A/MTIOC3B/TMO1/POE8#/TIOC0/TCLKD	SCK1/MISOA/SDA/SSITXD0			IRQ7/ CMPOB2
18		P16	MTIOC3C/MTIOC3D/TMO2/TIOC0B1/TCLKC/RTCOU	TXD1/SMOSI1/SSDA1/MOSIA/SCL/USB0_VBUS/USB0_VBUSEN/USB0_OVRCURB			IRQ6/ADTRG0#
19		P15	MTIOC0B/MTCLKB/TMCI2/TIOC0B2/TCLKB	RXD1/SMISO1/SSCL1/CRXD0		TS12	IRQ5/CMPB2
20		P14	MTIOC3A/MTCLKA/TMRI2/TIOC0B5/TCLKA	CTS1#/RTS1#/SS1#/CTXD0/USB0_OVRCURA		TS13	IRQ4/CVREFB2
21	VCC_USB*1	PH3*1	TMCI0*1				
22		PH2*1	TMRI0*1	USB0_DM*1			IRQ1*1
23		PH1*1	TMO0*1	USB0_DP*1			IRQ0*1
24	VSS_USB*1	PH0*1					CACREF*1
25		P55	MTIOC4D/TMO3	CRXD0		TS15	
26		P54	MTIOC4B/TMCI1	CTXD0		TS16	
27	UB	PC7	MTIOC3A/MTCLKB/TMO2	TXD8/SMOSI8/SSDA8/MISOA			CACREF
28		PC6	MTIOC3C/MTCLKA/TMCI2	RXD8/SMISO8/SSCL8/MOSIA/USB0_EXICEN		TS22	
29		PC5	MTIOC3B/MTCLKD/TMRI2	SCK8/RSPCKA/USB0_ID		TS23	
30		PC4	MTIOC3D/MTCLKC/TMCI1/POE0#	SCK5/CTS8#/RTS8#/SS8#/SSLA0	SDHI_D1	TSCAP	
31		PC3	MTIOC4D/TCLKB	TXD5/SMOSI5/SSDA5/IRTXD5	SDHI_D0	TS27	
32		PC2	MTIOC4B/TCLKA	RXD5/SMISO5/SSCL5/SSLA3/IRRXD5	SDHI_D3	TS30	
33		PB7/PC1	MTIOC3B/TIOC0B5	TXD9/SMOSI9/SSDA9	SDHI_D2		
34		PB6/PC0	MTIOC3D/TIOCA5	RXD9/SMISO9/SSCL9	SDHI_D1		
35		PB5	MTIOC2A/MTIOC1B/TMRI1/POE1#/TIOC0B4	SCK9	SDHI_CD		
36		PB3	MTIOC0A/MTIOC4A/TMO0/POE3#/TIOC0D3/TCLKD	SCK6	SDHI_W P		
37		PB1	MTIOC0C/MTIOC4C/TMCI0/TIOC0B3	TXD6/SMOSI6/SSDA6	SDHI_CLK		IRQ4/ CMPOB1
38	VCC						
39		PB0	MTIC5W/TIOCA3	RXD6/SMISO6/SSCL6/RSPCKA	SDHI_C MD		
40	VSS						
41		PA6	MTIC5V/MTCLKB/TMCI3/POE2#/TIOCA2	CTS5#/RTS5#/SS5#/MOSIA/SSIWS0			

Table 1.9 List of Pins and Pin Functions (64-Pin LQFP/HWQFN) (2/2)

Pin No.	Power Supply, Clock, System Control	I/O Port	Timers (MTU, TPU, TMR, RTC, CMT, POE, CAC)	Communications (SClg, SClh, RSPI, RIIC, CAN, USB, SSI)	Memory Interface (SDHI)	Touch sensing	Others
42		PA4	MTIC5U/MTCLKA/TMRI0/TIOCA1	TXD5/SMOSI5/SSDA5/SSLA0/SSITXD0/IRTXD5			IRQ5 /CVREFB1
43		PA3	MTIOC0D/MTCLKD/TIOCD0/TCLKB	RXD5/SMISO5/SSCL5/SSIRXD0/IRRXD5			IRQ6 /CMPB1
44		PA1	MTIOC0B/MTCLKC/TIOCB0	SCK5/SSLA2/SSISCK0			
45		PA0	MTIOC4A/TIOCA0	SSLA1			CACREF
46		PE5	MTIOC4C/MTIOC2B				IRQ5/AN021/CMPOB0
47		PE4	MTIOC4D/MTIOC1A				AN020/CMPA2/CLKOUT
48		PE3	MTIOC4B/POE8#	CTS12#/RTS12#/SS12#/AUDIO_MCLK			AN019/CLKOUT
49		PE2	MTIOC4A	RXD12/RDX12/SMISO12/SSCL12			IRQ7/AN018/CVREFB0
50		PE1	MTIOC4C	TXD12/TXDX12/SIOX12/SMOSI12/SSDA12			AN017/CMPB0
51		PE0		SCK12			AN016
52	VREFL						
53		P46					AN006
54	VREFH						
55		P44					AN004
56		P43					AN003
57		P42					AN002
58		P41					AN001
59	VREFL0						
60		P40					AN000
61	VREFH0						
62	AVCC0						
63		P05					DA1
64	AVSS0						

Note 1. RX230: PH0/CACREF, PH1/IRQ0/TMO0, PH2/IRQ1/TMRI0, PH3/TMCI0
RX231: VSS_USB, USB0_DP, USB0_DM, VCC_USB

Table 1.10 List of Pins and Pin Functions (48-Pin LQFP/HWQFN) (1/2)

Pin No.	Power Supply, Clock, System Control	I/O Port	Timers (MTU, TPU, TMR, RTC, CMT, POE, CAC)	Communications (SClg, SCih, RSPI, RIIC, CAN, USB, SSI)	Memory Interface (SDHI)	Touch sensing	Others
1	VCL						
2	MD						FINED
3	RES#						
4	XTAL	P37					
5	VSS						
6	EXTAL	P36					
7	VCC						
8		P35					NMI
9		P31	MTIOC4D/TMCI2	CTS1#/RTS1#/SS1#/SSISCK0			IRQ1
10		P30	MTIOC4B/TMRI3/POE8#	RXD1/SMISO1/SSCL1/ AUDIO_MCLK			IRQ0/CMPOB3
11		P27	MTIOC2B/TMCI3	SCK1/SSIWS0		TS2	CVREFB3
12		P26	MTIOC2A/TMO1	TXD1/SMOS1/SSDA1/ USB0_VBUSEN/SSIRXD0		TS3	CMPB3
13		P17	MTIOC3A/MTIOC3B/TMO1/ POE8#/TIOCB0/TCLKD	SCK1/MISOA/SDA/ SSITXD0			IRQ7/ CMPOB2
14		P16	MTIOC3C/MTIOC3D/TMO2/ TIOCB1/TCLKC	TXD1/SMOS1/SSDA1/MOSIA/ SCL/USB0_VBUS/ USB0_VBUSEN/ USB0_OVRCURB			IRQ6/ADTRG0#
15		P15	MTIOC0B/MTCLKB/TMCI2/ TIOCB2/TCLKB	RXD1/SMISO1/SSCL1/CRXD0		TS12	IRQ5/CMPB2
16		P14	MTIOC3A/MTCLKA/TMRI2/ TIOCB5/TCLKA	CTS1#/RTS1#/SS1#/CTXD0/ USB0_OVRCURA		TS13	IRQ4/CVREFB2
17	VCC_USB*1	PH3*1	TMCI0*1				
18		PH2*1	TMRI0*1	USB0_DM*1			IRQ1*1
19		PH1*1	TMO0*1	USB0_DP*1			IRQ0*1
20	VSS_USB*1	PH0*1					CACREF*1
21	UB	PC7	MTIOC3A/MTCLKB/TMO2	TXD8/SMOS8/SSDA8/MISOA			CACREF
22		PC6	MTIOC3C/MTCLKA/TMCI2	RXD8/SMISO8/SSCL8/MOSIA/ USB0_EXICEN		TS22	
23		PC5	MTIOC3B/MTCLKD/TMRI2	SCK8/RSPCKA/USB0_ID		TS23	
24		PC4	MTIOC3D/MTCLKC/TMCI1/ POE0#	SCK5/CTS8#/RTS8#/SS8#/ SSLA0	SDHI_D1	TSCAP	
25		PB5/PC3	MTIOC2A/MTIOC1B/TMRI1/ POE1#/TIOCB4		SDHI_CD		
26		PB3/PC2	MTIOC0A/MTIOC4A/TMO0/ POE3#/TIOC3/TCLKD	SCK6	SDHI_W P		
27		PB1/PC1	MTIOC0C/MTIOC4C/TMCI0/ TIOCB3	TXD6/SMOS6/SSDA6	SDHI_CL K		IRQ4/ CMPOB1
28	VCC						
29		PB0/PC0	MTIC5W/TIOCA3	RXD6/SMISO6/SSCL6/RSPCKA	SDHI_C MD		
30	VSS						
31		PA6	MTIC5V/MTCLKB/TMCI3/POE2#/ TIOCA2	CTS5#/RTS5#/SS5#/MOSIA/ SSIWS0			
32		PA4	MTIC5U/MTCLKA/TMRI0/TIOCA1	TXD5/SMOS5/SSDA5/SSLA0/ SSITXD0/IRTXD5			IRQ5 /CVREFB1
33		PA3	MTIOC0D/MTCLKD/TIOC0D/ TCLKB	RXD5/SMISO5/SSCL5/SSIRXD0/ IRRXD5			IRQ6 /CMPB1
34		PA1	MTIOC0B/MTCLKC/TIOCB0	SCK5/SSLA2/SSISCK0			
35		PE4	MTIOC4D/MTIOC1A				AN020/CMPA2/ CLKOUT
36		PE3	MTIOC4B/POE8#	CTS12#/RTS12#/AUDIO_MCLK			AN019/CLKOUT
37		PE2	MTIOC4A	RXD12/RXD12/SSCL12			IRQ7/AN018/ CVREFB0
38		PE1	MTIOC4C	TXD12/TXD12/SIOX12/SSDA12			AN017/CMPB0
39	VREFL						
40		P46					AN006

Table 1.10 List of Pins and Pin Functions (48-Pin LQFP/HWQFN) (2/2)

Pin No.	Power Supply, Clock, System Control	I/O Port	Timers (MTU, TPU, TMR, RTC, CMT, POE, CAC)	Communications (SCIg, SCIf, RSPI, RIIC, CAN, USB, SSI)	Memory Interface (SDHI)	Touch sensing	Others
41	VREFH						
42		P42					AN002
43		P41					AN001
44	VREFL0						
45		P40					AN000
46	VREFH0						
47	AVCC0						
48	AVSS0						

Note 1. RX230: PH0/CACREF, PH1/IRQ0/TMO0, PH2/IRQ1/TMRI0, PH3/TMCI0
 RX231: VSS_USB, USB0_DP, USB0_DM, VCC_USB

2. CPU

Figure 2.1 shows register set of the CPU.

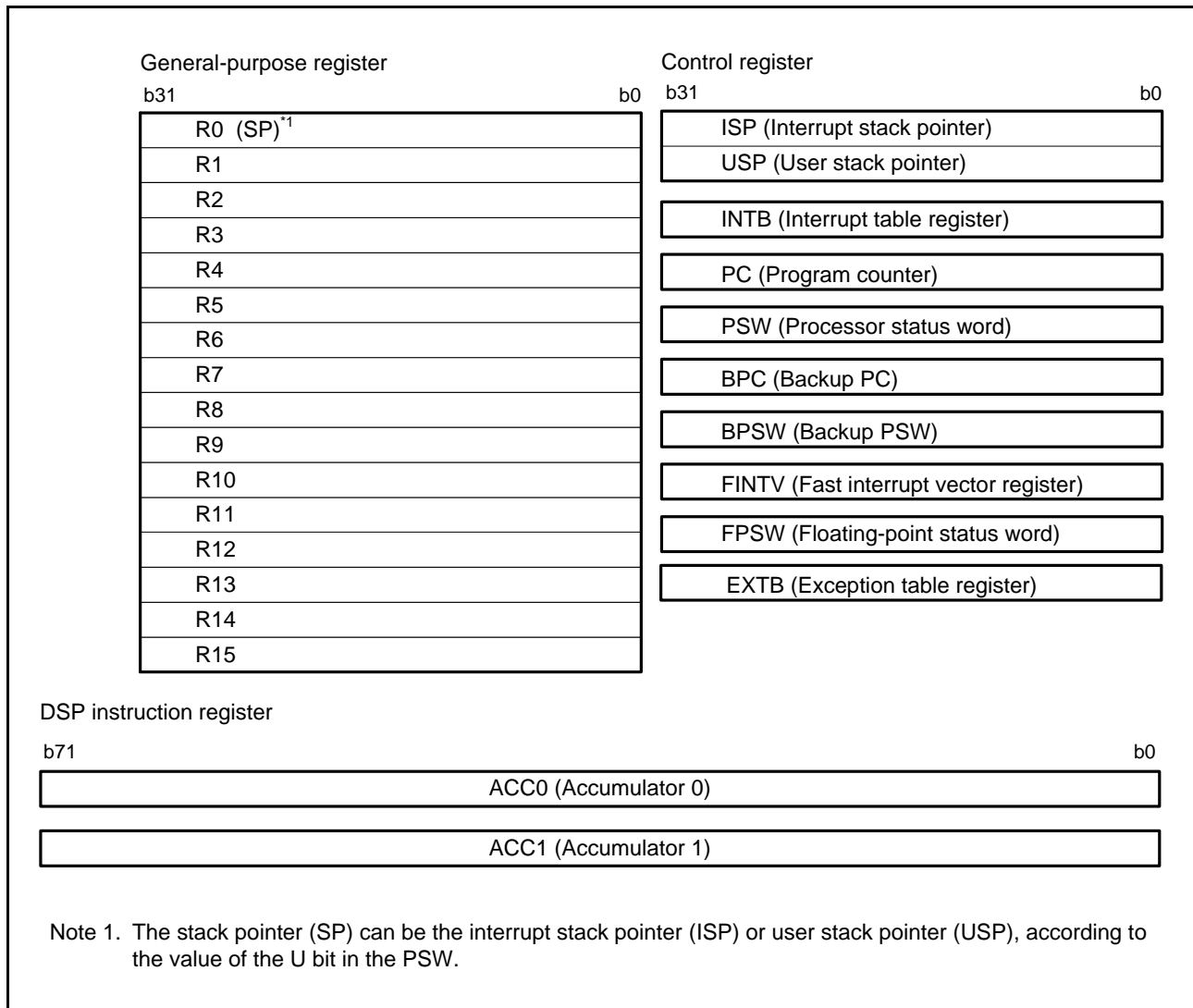


Figure 2.1 Register Set of the CPU

2.1 General-Purpose Registers (R0 to R15)

This CPU has sixteen 32-bit general-purpose registers (R0 to R15). R0 to R15 can be used as data registers or address registers.

R0, a general-purpose register, also functions as the stack pointer (SP).

The stack pointer is switched to operate as the interrupt stack pointer (ISP) or user stack pointer (USP) by the value of the stack pointer select bit (U) in the processor status word (PSW).

2.2 Control Registers

(1) Interrupt stack pointer (ISP) and user stack pointer (USP)

The stack pointer (SP) can be either of two types, the interrupt stack pointer (ISP) or the user stack pointer (USP). Whether the stack pointer operates as the ISP or USP depends on the value of the stack pointer select bit (U) in the processor status word (PSW).

Set the ISP or USP to a multiple of 4 to reduce the number of cycles required to execute interrupt sequences and instructions entailing stack manipulation.

(2) Exception table register (EXTB)

The exception table register (EXTB) specifies the address where the exception vector table starts.

Set the EXTB to a multiple of 4 to reduce the number of cycles required to execute interrupt sequences and instructions entailing stack manipulation.

(3) Interrupt table register (INTB)

The interrupt table register (INTB) specifies the address where the interrupt vector table starts.

Set the INTB to a multiple of 4 to reduce the number of cycles required to execute interrupt sequences and instructions entailing stack manipulation.

(4) Program counter (PC)

The program counter (PC) indicates the address of the instruction being executed.

(5) Processor status word (PSW)

The processor status word (PSW) indicates the results of instruction execution or the state of the CPU.

(6) Backup PC (BPC)

The backup PC (BPC) is provided to speed up response to interrupts.

After a fast interrupt has been generated, the contents of the program counter (PC) are saved in the BPC register.

(7) Backup PSW (BPSW)

The backup PSW (BPSW) is provided to speed up response to interrupts.

After a fast interrupt has been generated, the contents of the processor status word (PSW) are saved in the BPSW. The allocation of bits in the BPSW corresponds to that in the PSW.

(8) Fast interrupt vector register (FINTV)

The fast interrupt vector register (FINTV) is provided to speed up response to interrupts.

The FINTV register specifies a branch destination address when a fast interrupt has been generated.

(9) Floating-point status word (FPSW)

The floating-point status word (FPSW) indicates the results of floating-point operations.

When an exception handling enable bit (E_j) enables the exception handling ($E_j = 1$), the exception cause can be identified by checking the corresponding C_j flag in the exception handling routine. If the exception handling is masked ($E_j = 0$), the occurrence of exception can be checked by reading the F_j flag at the end of a series of processing. Once the F_j flag has been set to 1, this value is retained until it is cleared to 0 by software ($j = X, U, Z, O, \text{ or } V$).

2.3 Accumulator

The accumulator (ACC0 or ACC1) is a 72-bit register used for DSP instructions. The accumulator is handled as a 96-bit register for reading and writing. At this time, when bits 95 to 72 of the accumulator are read, the value where the value of bit 71 is sign extended is read. Writing to bits 95 to 72 of the accumulator is ignored. ACC0 is also used for the multiply and multiply-and-accumulate instructions; EMUL, EMULU, FMUL, MUL, and RMPA, in which case the prior value in ACC0 is modified by execution of the instruction.

Use the MVTACGU, MVTACHI, and MVTACLO instructions for writing to the accumulator. The MVTACGU, MVTACHI, and MVTACLO instructions write data to bits 95 to 64, the higher-order 32 bits (bits 63 to 32), and the lower-order 32 bits (bits 31 to 0), respectively.

Use the MVFACGU, MVFACHI, MVFACMI, and MVFACLO instructions for reading data from the accumulator. The MVFACGU, MVFACHI, MVFACMI, and MVFACLO instructions read data from the guard bits (bits 95 to 64), higher-order 32 bits (bits 63 to 32), the middle 32 bits (bits 47 to 16), and the lower-order 32 bits (bits 31 to 0), respectively.

3. Address Space

3.1 Address Space

This LSI has a 4-Gbyte address space, consisting of the range of addresses from 0000 0000h to FFFF FFFFh. That is, linear access to an address space of up to 4 Gbytes is possible, and this contains both program and data areas.

Figure 3.1 shows the memory maps in the respective operating modes. Accessible areas will differ according to the operating mode and states of control bits.

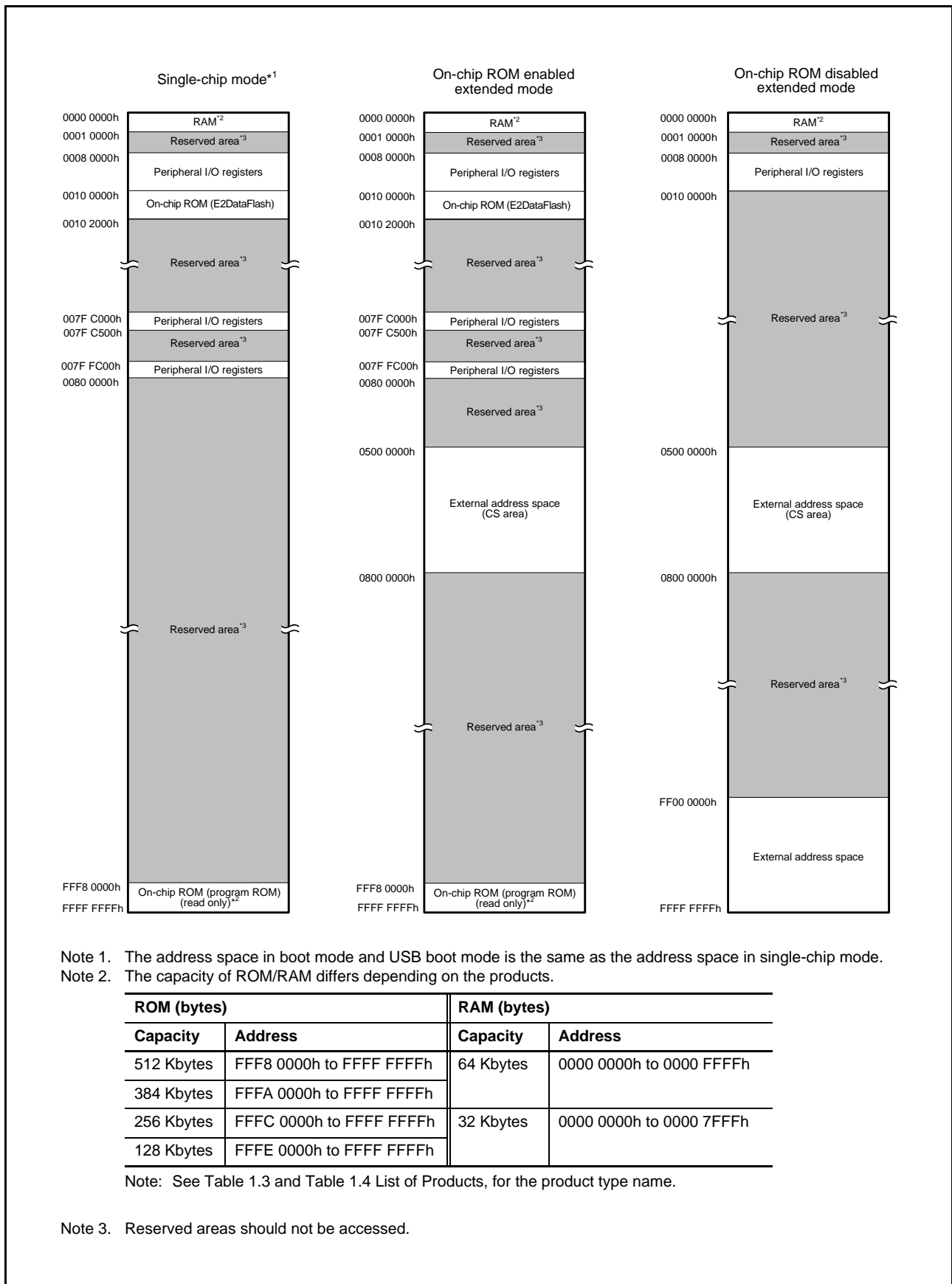


Figure 3.1 Memory Map in Each Operating Mode

3.2 External Address Space

The external address space is divided into up to four CS areas (CS0 to CS3), each corresponding to the CSn# signal output from a CSn# (n = 0 to 3) pin. Figure 3.2 shows the address ranges corresponding to the individual CS areas (CS0 to CS3) in on-chip ROM disabled extended mode.

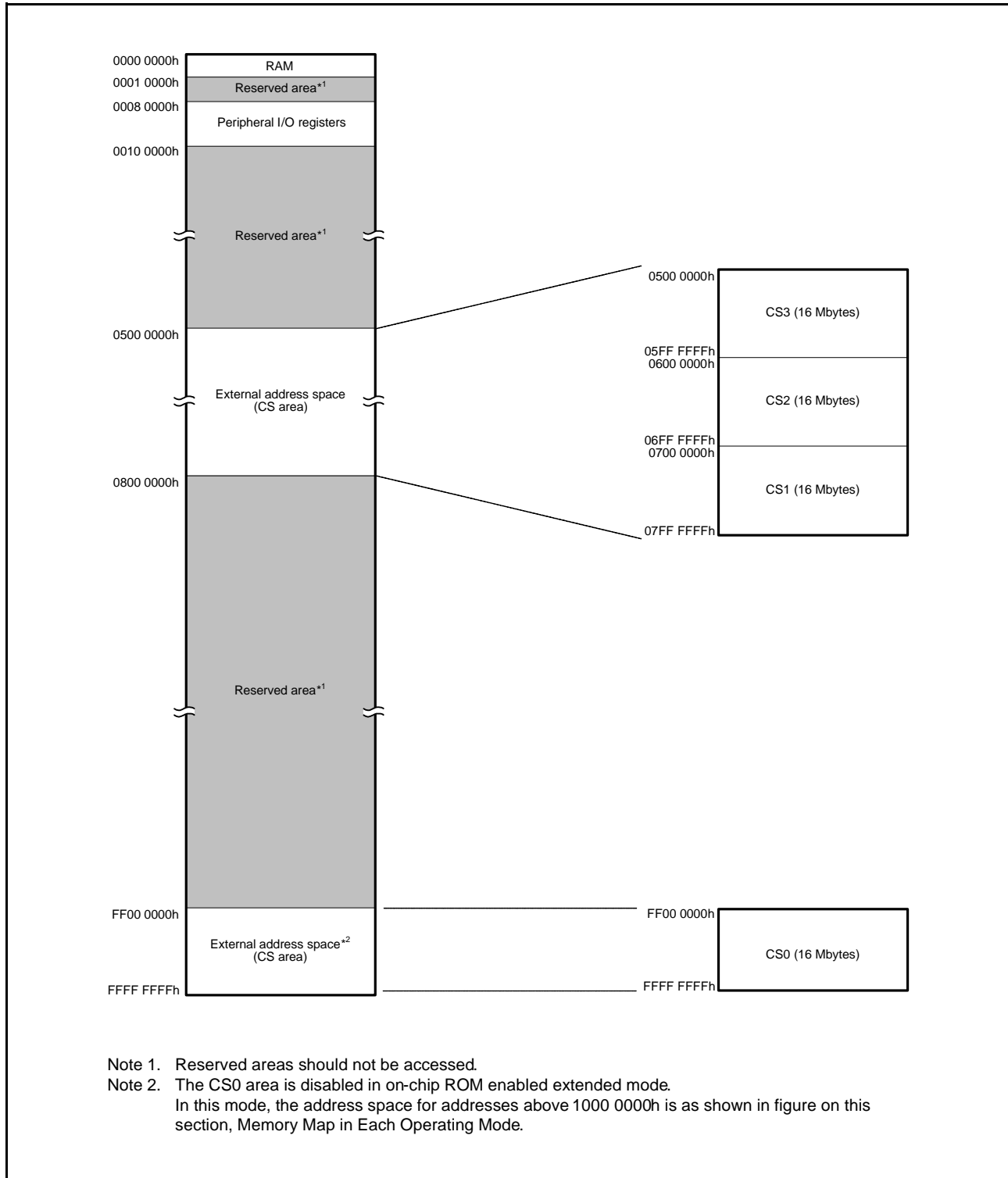


Figure 3.2 Correspondence between External Address Spaces and CS Areas (In On-Chip ROM Disabled Extended Mode)

4. I/O Registers

This section provides information on the on-chip I/O register addresses and bit configuration. The information is given as shown below. Notes on writing to registers are also given below.

(1) I/O register addresses (address order)

- Registers are listed from the lower allocation addresses.
- Registers are classified according to module symbols.
- Numbers of cycles for access indicate numbers of cycles of the given base clock.
- Among the internal I/O register area, addresses not listed in the list of registers are reserved. Reserved addresses must not be accessed. Do not access these addresses; otherwise, the operation when accessing these bits and subsequent operations cannot be guaranteed.

(2) Notes on writing to I/O registers

When writing to an I/O register, the CPU starts executing the subsequent instruction before completing I/O register write. This may cause the subsequent instruction to be executed before the post-update I/O register value is reflected on the operation.

As described in the following examples, special care is required for the cases in which the subsequent instruction must be executed after the post-update I/O register value is actually reflected.

[Examples of cases requiring special care]

- The subsequent instruction must be executed while an interrupt request is disabled with the IENj bit in IERN of the ICU (interrupt request enable bit) cleared to 0.
- A WAIT instruction is executed immediately after the preprocessing for causing a transition to the low power consumption state.

In the above cases, after writing to an I/O register, wait until the write operation is completed using the following procedure and then execute the subsequent instruction.

- Write to an I/O register.
- Read the value from the I/O register to a general register.
- Execute the operation using the value read.
- Execute the subsequent instruction.

[Instruction examples]

- Byte-size I/O registers

```
MOV.L #SFR_ADDR, R1
MOV.B #SFR_DATA, [R1]
CMP [R1].UB, R1
;; Next process
```

- Word-size I/O registers

```
MOV.L #SFR_ADDR, R1
MOV.W #SFR_DATA, [R1]
CMP [R1].W, R1
;; Next process
```

- Longword-size I/O registers

```
MOV.L #SFR_ADDR, R1
MOV.L #SFR_DATA, [R1]
CMP [R1].L, R1
;; Next process
```

If multiple registers are written to and a subsequent instruction should be executed after the write operations are entirely completed, only read the I/O register that was last written to and execute the operation using the value; it is not necessary to read or execute operation for all the registers that were written to.

(3) Number of Access Cycles to I/O Registers

For numbers of clock cycles for access to I/O registers, see Table 4.1, List of I/O Registers (Address Order). The number of access cycles to I/O registers is obtained by following equation.*1

$$\begin{aligned} \text{Number of access cycles to I/O registers} = & \text{Number of bus cycles for internal main bus 1} + \\ & \text{Number of divided clock synchronization cycles} + \\ & \text{Number of bus cycles for internal peripheral bus 1 to 6} \end{aligned}$$

The number of bus cycles of internal peripheral bus 1 to 6 differs according to the register to be accessed. When peripheral functions connected to internal peripheral bus 2 to 6 or registers for the external bus control unit (except for bus error related registers) are accessed, the number of divided clock synchronization cycles is added. The number of divided clock synchronization cycles differs depending on the frequency ratio between ICLK and PCLK (or FCLK, BCLK) or bus access timing.

In the peripheral function unit, when the frequency ratio of ICLK is equal to or greater than that of PCLK (or FCLK), the sum of the number of bus cycles for internal main bus 1 and the number of the divided clock synchronization cycles will be one cycle of PCLK (or FCLK) at a maximum. Therefore, one PCLK (or FCLK) has been added to the number of access cycles shown in Table 4.1.

When the frequency ratio of ICLK is lower than that of PCLK (or FCLK), the subsequent bus access is started from the ICLK cycle following the completion of the access to the peripheral functions. Therefore, the access cycles are described on an ICLK basis.

In the external bus control unit, the sum of the number of bus cycles for internal main bus 1 and the number of divided clock synchronization cycles will be one cycle of BCLK at a maximum. Therefore, one BCLK is added to the number of access cycles shown in Table 4.1.

Note 1. This applies to the number of cycles when the access from the CPU does not conflict with the instruction fetching to the external memory or bus access from the different bus master (DMAC or DTC).

(4) Restrictions in Relation to RMPA and String-Manipulation Instructions

The allocation of data to be handled by RMPA or string-manipulation instructions to I/O registers is prohibited, and operation is not guaranteed if this restriction is not observed.

(5) Notes on Sleep Mode and Mode Transitions

During sleep mode or mode transitions, do not write to the system control related registers (indicated by 'SYSTEM' in the Module Symbol column in Table 4.1, List of I/O Registers (Address Order)).

4.1 I/O Register Addresses (Address Order)

Table 4.1 List of I/O Registers (Address Order) (1 / 42)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles	
						ICLK ≥ PCLK	ICLK < PCLK
0008 0000h	SYSTEM	Mode Monitor Register	MDMONR	16	16	3	ICLK
0008 0006h	SYSTEM	System Control Register 0	SYSCR0	16	16	3	ICLK
0008 0008h	SYSTEM	System Control Register 1	SYSCR1	16	16	3	ICLK
0008 000Ch	SYSTEM	Standby Control Register	SBYCR	16	16	3	ICLK
0008 0010h	SYSTEM	Module Stop Control Register A	MSTPCRA	32	32	3	ICLK
0008 0014h	SYSTEM	Module Stop Control Register B	MSTPCRB	32	32	3	ICLK
0008 0018h	SYSTEM	Module Stop Control Register C	MSTPCRC	32	32	3	ICLK
0008 001Ch	SYSTEM	Module Stop Control Register D	MSTPCRD	32	32	3	ICLK
0008 0020h	SYSTEM	System Clock Control Register	SCKCR	32	32	3	ICLK
0008 0026h	SYSTEM	System Clock Control Register 3	SCKCR3	16	16	3	ICLK
0008 0028h	SYSTEM	PLL Control Register	PLLCR	16	16	3	ICLK
0008 002Ah	SYSTEM	PLL Control Register 2	PLLCR2	8	8	3	ICLK
0008 002Ch	SYSTEM	USB-dedicated PLL Control Register	UPLLCR	16	16	3	ICLK
0008 002Eh	SYSTEM	USB-dedicated PLL Control Register 2	UPLLCR2	8	8	3	ICLK
0008 0030h	SYSTEM	External Bus Clock Control Register	BCKCR	8	8	3	ICLK
0008 0031h	SYSTEM	Memory Wait Cycle Setting Register	MEMWAIT	8	8	3	ICLK
0008 0032h	SYSTEM	Main Clock Oscillator Control Register	MOSCCR	8	8	3	ICLK
0008 0033h	SYSTEM	Sub-Clock Oscillator Control Register	SOSCCR	8	8	3	ICLK
0008 0034h	SYSTEM	Low-Speed On-Chip Oscillator Control Register	LOCOCR	8	8	3	ICLK
0008 0035h	SYSTEM	IWDT-Dedicated On-Chip Oscillator Control Register	ILOCOCR	8	8	3	ICLK
0008 0036h	SYSTEM	High-Speed On-Chip Oscillator Control Register	HOCOCR	8	8	3	ICLK
0008 0037h	SYSTEM	High-Speed On-Chip Oscillator Control Register 2	HOCOCR2	8	8	3	ICLK
0008 003Ch	SYSTEM	Oscillation Stabilization Flag Register	OSCOVFSR	8	8	3	ICLK
0008 003Eh	SYSTEM	CLKOUT Output Control Register	CKOCR	16	16	3	ICLK
0008 0040h	SYSTEM	Oscillation Stop Detection Control Register	OSTDCR	8	8	3	ICLK
0008 0041h	SYSTEM	Oscillation Stop Detection Status Register	OSTDSR	8	8	3	ICLK
0008 0060h	SYSTEM	Low-Speed On-Chip Oscillator Trimming Register	LOCOTRR	8	8	3	ICLK
0008 0064h	SYSTEM	IWDT-Dedicated On-Chip Oscillator Trimming Register	ILOCOTRR	8	8	3	ICLK
0008 0068h	SYSTEM	High-Speed On-Chip Oscillator Trimming Register 0	HOCOTRR0	8	8	3	ICLK
0008 006Bh	SYSTEM	High-Speed On-Chip Oscillator Trimming Register 3	HOCOTRR3	8	8	3	ICLK
0008 00A0h	SYSTEM	Operating Power Control Register	OPCCR	8	8	3	ICLK
0008 00A1h	SYSTEM	Sleep Mode Return Clock Source Switching Register	RSTCKCR	8	8	3	ICLK
0008 00A2h	SYSTEM	Main Clock Oscillator Wait Control Register	MOSCWTCR	8	8	3	ICLK
0008 00AAh	SYSTEM	Sub Operating Power Control Register	SOPCCR	8	8	3	ICLK
0008 00B0h	LPT	Low Power Timer Control Register 1	LPTCR1	8	8	3	ICLK
0008 00B1h	LPT	Low Power Timer Control Register 2	LPTCR2	8	8	3	ICLK
0008 00B2h	LPT	Low Power Timer Control Register 3	LPTCR3	8	8	3	ICLK
0008 00B4h	LPT	Low Power Timer Cycle Setting Register	LPTPRD	16	16	3	ICLK
0008 00B8h	LPT	Low Power Timer Compare Register 0	LPCMR0	16	16	3	ICLK
0008 00BCh	LPT	Low Power Timer Standby Return Enable Register	LPWUCR	16	16	3	ICLK
0008 00C0h	SYSTEM	Reset Status Register 2	RSTSR2	8	8	3	ICLK
0008 00C2h	SYSTEM	Software Reset Register	SWRR	16	16	3	ICLK
0008 00E0h	SYSTEM	Voltage Monitoring 1 Circuit Control Register 1	LVD1CR1	8	8	3	ICLK
0008 00E1h	SYSTEM	Voltage Monitoring 1 Circuit Status Register	LVD1SR	8	8	3	ICLK
0008 00E2h	SYSTEM	Voltage Monitoring 2 Circuit Control Register 1	LVD2CR1	8	8	3	ICLK
0008 00E3h	SYSTEM	Voltage Monitoring 2 Circuit Status Register	LVD2SR	8	8	3	ICLK
0008 03FEh	SYSTEM	Protect Register	PRCR	16	16	3	ICLK
0008 1300h	BSC	Bus Error Status Clear Register	BERCLR	8	8	2	ICLK
0008 1304h	BSC	Bus Error Monitoring Enable Register	BEREN	8	8	2	ICLK

Table 4.1 List of I/O Registers (Address Order) (2 / 42)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles	
						ICLK ≥ PCLK	ICLK < PCLK
0008 1308h	BSC	Bus Error Status Register 1	BERSR1	8	8		2 ICLK
0008 130Ah	BSC	Bus Error Status Register 2	BERSR2	16	16		2 ICLK
0008 1310h	BSC	Bus Priority Control Register	BUSPRI	16	16		2 ICLK
0008 2000h	DMAC0	DMA Source Address Register	DMSAR	32	32		2 ICLK
0008 2004h	DMAC0	DMA Destination Address Register	DMDAR	32	32		2 ICLK
0008 2008h	DMAC0	DMA Transfer Count Register	DMCRA	32	32		2 ICLK
0008 200Ch	DMAC0	DMA Block Transfer Count Register	DMCRB	16	16		2 ICLK
0008 2010h	DMAC0	DMA Transfer Mode Register	DMTMD	16	16		2 ICLK
0008 2013h	DMAC0	DMA Interrupt Setting Register	DMINT	8	8		2 ICLK
0008 2014h	DMAC0	DMA Address Mode Register	DMAMD	16	16		2 ICLK
0008 2018h	DMAC0	DMA Offset Register	DMOFR	32	32		2 ICLK
0008 201Ch	DMAC0	DMA Transfer Enable Register	DMCNT	8	8		2 ICLK
0008 201Dh	DMAC0	DMA Software Start Register	DMREQ	8	8		2 ICLK
0008 201Eh	DMAC0	DMA Status Register	DMSTS	8	8		2 ICLK
0008 201Fh	DMAC0	DMA Activation Source Flag Control Register	DMCSL	8	8		2 ICLK
0008 2040h	DMAC1	DMA Source Address Register	DMSAR	32	32		2 ICLK
0008 2044h	DMAC1	DMA Destination Address Register	DMDAR	32	32		2 ICLK
0008 2048h	DMAC1	DMA Transfer Count Register	DMCRA	32	32		2 ICLK
0008 204Ch	DMAC1	DMA Block Transfer Count Register	DMCRB	16	16		2 ICLK
0008 2050h	DMAC1	DMA Transfer Mode Register	DMTMD	16	16		2 ICLK
0008 2053h	DMAC1	DMA Interrupt Setting Register	DMINT	8	8		2 ICLK
0008 2054h	DMAC1	DMA Address Mode Register	DMAMD	16	16		2 ICLK
0008 205Ch	DMAC1	DMA Transfer Enable Register	DMCNT	8	8		2 ICLK
0008 205Dh	DMAC1	DMA Software Start Register	DMREQ	8	8		2 ICLK
0008 205Eh	DMAC1	DMA Status Register	DMSTS	8	8		2 ICLK
0008 205Fh	DMAC1	DMA Activation Source Flag Control Register	DMCSL	8	8		2 ICLK
0008 2080h	DMAC2	DMA Source Address Register	DMSAR	32	32		2 ICLK
0008 2084h	DMAC2	DMA Destination Address Register	DMDAR	32	32		2 ICLK
0008 2088h	DMAC2	DMA Transfer Count Register	DMCRA	32	32		2 ICLK
0008 208Ch	DMAC2	DMA Block Transfer Count Register	DMCRB	16	16		2 ICLK
0008 2090h	DMAC2	DMA Transfer Mode Register	DMTMD	16	16		2 ICLK
0008 2093h	DMAC2	DMA Interrupt Setting Register	DMINT	8	8		2 ICLK
0008 2094h	DMAC2	DMA Address Mode Register	DMAMD	16	16		2 ICLK
0008 209Ch	DMAC2	DMA Transfer Enable Register	DMCNT	8	8		2 ICLK
0008 209Dh	DMAC2	DMA Software Start Register	DMREQ	8	8		2 ICLK
0008 209Eh	DMAC2	DMA Status Register	DMSTS	8	8		2 ICLK
0008 209Fh	DMAC2	DMA Activation Source Flag Control Register	DMCSL	8	8		2 ICLK
0008 20C0h	DMAC3	DMA Source Address Register	DMSAR	32	32		2 ICLK
0008 20C4h	DMAC3	DMA Destination Address Register	DMDAR	32	32		2 ICLK
0008 20C8h	DMAC3	DMA Transfer Count Register	DMCRA	32	32		2 ICLK
0008 20CCh	DMAC3	DMA Block Transfer Count Register	DMCRB	16	16		2 ICLK
0008 20D0h	DMAC3	DMA Transfer Mode Register	DMTMD	16	16		2 ICLK
0008 20D3h	DMAC3	DMA Interrupt Setting Register	DMINT	8	8		2 ICLK
0008 20D4h	DMAC3	DMA Address Mode Register	DMAMD	16	16		2 ICLK
0008 20DCh	DMAC3	DMA Transfer Enable Register	DMCNT	8	8		2 ICLK
0008 20DDh	DMAC3	DMA Software Start Register	DMREQ	8	8		2 ICLK
0008 20DEh	DMAC3	DMA Status Register	DMSTS	8	8		2 ICLK
0008 20DFh	DMAC3	DMA Activation Source Flag Control Register	DMCSL	8	8		2 ICLK
0008 2200h	DMAC	DMA Module Activation Register	DMAST	8	8		2 ICLK
0008 2400h	DTC	DTC Control Register	DTCCR	8	8		2 ICLK
0008 2404h	DTC	DTC Vector Base Register	DTCVBR	32	32		2 ICLK
0008 2408h	DTC	DTC Address Mode Register	DTCADMOD	8	8		2 ICLK

Table 4.1 List of I/O Registers (Address Order) (3 / 42)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles	
						ICLK ≥ PCLK	ICLK < PCLK
0008 240Ch	DTC	DTC Module Start Register	DTCST	8	8		2 ICLK
0008 240Eh	DTC	DTC Status Register	DTCSTS	16	16		2 ICLK
0008 3002h	BSC	CS0 Mode Register	CS0MOD	16	16		1 or 2 BCLK
0008 3004h	BSC	CS0 Wait Control Register 1	CS0WCR1	32	32		1 or 2 BCLK
0008 3008h	BSC	CS0 Wait Control Register 2	CS0WCR2	32	32		1 or 2 BCLK
0008 3012h	BSC	CS1 Mode Register	CS1MOD	16	16		1 or 2 BCLK
0008 3014h	BSC	CS1 Wait Control Register 1	CS1WCR1	32	32		1 or 2 BCLK
0008 3018h	BSC	CS1 Wait Control Register 2	CS1WCR2	32	32		1 or 2 BCLK
0008 3022h	BSC	CS2 Mode Register	CS2MOD	16	16		1 or 2 BCLK
0008 3024h	BSC	CS2 Wait Control Register 1	CS2WCR1	32	32		1 or 2 BCLK
0008 3028h	BSC	CS2 Wait Control Register 2	CS2WCR2	32	32		1 or 2 BCLK
0008 3032h	BSC	CS3 Mode Register	CS3MOD	16	16		1 or 2 BCLK
0008 3034h	BSC	CS3 Wait Control Register 1	CS3WCR1	32	32		1 or 2 BCLK
0008 3038h	BSC	CS3 Wait Control Register 2	CS3WCR2	32	32		1 or 2 BCLK
0008 3802h	BSC	CS0 Control Register	CS0CR	16	16		1 or 2 BCLK
0008 380Ah	BSC	CS0 Recovery Cycle Register	CS0REC	16	16		1 or 2 BCLK
0008 3812h	BSC	CS1 Control Register	CS1CR	16	16		1 or 2 BCLK
0008 381Ah	BSC	CS1 Recovery Cycle Register	CS1REC	16	16		1 or 2 BCLK
0008 3822h	BSC	CS2 Control Register	CS2CR	16	16		1 or 2 BCLK
0008 382Ah	BSC	CS2 Recovery Cycle Register	CS2REC	16	16		1 or 2 BCLK
0008 3832h	BSC	CS3 Control Register	CS3CR	16	16		1 or 2 BCLK
0008 383Ah	BSC	CS3 Recovery Cycle Register	CS3REC	16	16		1 or 2 BCLK
0008 3880h	BSC	CS Recovery Cycle Insertion Enable Register	CSRECEN	16	16		1 or 2 BCLK
0008 6400h	MPU	Region-0 Start Page Number Register	RSPAGE0	32	32		1 ICLK
0008 6404h	MPU	Region-0 End Page Number Register	REPAGE0	32	32		1 ICLK
0008 6408h	MPU	Region-1 Start Page Number Register	RSPAGE1	32	32		1 ICLK
0008 640Ch	MPU	Region-1 End Page Number Register	REPAGE1	32	32		1 ICLK
0008 6410h	MPU	Region-2 Start Page Number Register	RSPAGE2	32	32		1 ICLK
0008 6414h	MPU	Region-2 End Page Number Register	REPAGE2	32	32		1 ICLK
0008 6418h	MPU	Region-3 Start Page Number Register	RSPAGE3	32	32		1 ICLK
0008 641Ch	MPU	Region-3 End Page Number Register	REPAGE3	32	32		1 ICLK
0008 6420h	MPU	Region-4 Start Page Number Register	RSPAGE4	32	32		1 ICLK
0008 6424h	MPU	Region-4 End Page Number Register	REPAGE4	32	32		1 ICLK
0008 6428h	MPU	Region-5 Start Page Number Register	RSPAGE5	32	32		1 ICLK
0008 642Ch	MPU	Region-5 End Page Number Register	REPAGE5	32	32		1 ICLK
0008 6430h	MPU	Region-6 Start Page Number Register	RSPAGE6	32	32		1 ICLK
0008 6434h	MPU	Region-6 End Page Number Register	REPAGE6	32	32		1 ICLK
0008 6438h	MPU	Region-7 Start Page Number Register	RSPAGE7	32	32		1 ICLK
0008 643Ch	MPU	Region-7 End Page Number Register	REPAGE7	32	32		1 ICLK
0008 6500h	MPU	Memory-Protection Enable Register	MPEN	32	32		1 ICLK
0008 6504h	MPU	Background Access Control Register	MPBAC	32	32		1 ICLK
0008 6508h	MPU	Memory-Protection Error Status-Clearing Register	MPECLR	32	32		1 ICLK
0008 650Ch	MPU	Memory-Protection Error Status Register	MPESTS	32	32		1 ICLK
0008 6514h	MPU	Data Memory-Protection Error Address Register	MPDEA	32	32		1 ICLK
0008 6520h	MPU	Region Search Address Register	MPSA	32	32		1 ICLK
0008 6524h	MPU	Region Search Operation Register	MPOPS	16	16		1 ICLK
0008 6526h	MPU	Region Invalidation Operation Register	MPOPI	16	16		1 ICLK
0008 6528h	MPU	Instruction-Hit Region Register	MHITI	32	32		1 ICLK
0008 652Ch	MPU	Data-Hit Region Register	MHITD	32	32		1 ICLK
0008 7010h	ICU	Interrupt Request Register 016	IR016	8	8		2 ICLK
0008 7017h	ICU	Interrupt Request Register 023	IR023	8	8		2 ICLK
0008 701Bh	ICU	Interrupt Request Register 027	IR027	8	8		2 ICLK

Table 4.1 List of I/O Registers (Address Order) (4 / 42)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles	
						ICLK ≥ PCLK	ICLK < PCLK
0008 701Ch	ICU	Interrupt Request Register 028	IR028	8	8		2 ICLK
0008 701Dh	ICU	Interrupt Request Register 029	IR029	8	8		2 ICLK
0008 701Eh	ICU	Interrupt Request Register 030	IR030	8	8		2 ICLK
0008 701Fh	ICU	Interrupt Request Register 031	IR031	8	8		2 ICLK
0008 7020h	ICU	Interrupt Request Register 032	IR032	8	8		2 ICLK
0008 7021h	ICU	Interrupt Request Register 033	IR033	8	8		2 ICLK
0008 7022h	ICU	Interrupt Request Register 034	IR034	8	8		2 ICLK
0008 7023h	ICU	Interrupt Request Register 035	IR035	8	8		2 ICLK
0008 7025h	ICU	Interrupt Request Register 037	IR037	8	8		2 ICLK
0008 7026h	ICU	Interrupt Request Register 038	IR038	8	8		2 ICLK
0008 7028h	ICU	Interrupt Request Register 040	IR040	8	8		2 ICLK
0008 7029h	ICU	Interrupt Request Register 041	IR041	8	8		2 ICLK
0008 702Ah	ICU	Interrupt Request Register 042	IR042	8	8		2 ICLK
0008 702Bh	ICU	Interrupt Request Register 043	IR043	8	8		2 ICLK
0008 702Ch	ICU	Interrupt Request Register 044	IR044	8	8		2 ICLK
0008 702Dh	ICU	Interrupt Request Register 045	IR045	8	8		2 ICLK
0008 702Eh	ICU	Interrupt Request Register 046	IR046	8	8		2 ICLK
0008 702Fh	ICU	Interrupt Request Register 047	IR047	8	8		2 ICLK
0008 7030h	ICU	Interrupt Request Register 048	IR048	8	8		2 ICLK
0008 7031h	ICU	Interrupt Request Register 049	IR049	8	8		2 ICLK
0008 7032h	ICU	Interrupt Request Register 050	IR050	8	8		2 ICLK
0008 7033h	ICU	Interrupt Request Register 051	IR051	8	8		2 ICLK
0008 7034h	ICU	Interrupt Request Register 052	IR052	8	8		2 ICLK
0008 7035h	ICU	Interrupt Request Register 053	IR053	8	8		2 ICLK
0008 7036h	ICU	Interrupt Request Register 054	IR054	8	8		2 ICLK
0008 7037h	ICU	Interrupt Request Register 055	IR055	8	8		2 ICLK
0008 7038h	ICU	Interrupt Request Register 056	IR056	8	8		2 ICLK
0008 7039h	ICU	Interrupt Request Register 057	IR057	8	8		2 ICLK
0008 703Ah	ICU	Interrupt Request Register 058	IR058	8	8		2 ICLK
0008 703Bh	ICU	Interrupt Request Register 059	IR059	8	8		2 ICLK
0008 703Ch	ICU	Interrupt Request Register 060	IR060	8	8		2 ICLK
0008 703Dh	ICU	Interrupt Request Register 061	IR061	8	8		2 ICLK
0008 703Eh	ICU	Interrupt Request Register 062	IR062	8	8		2 ICLK
0008 703Fh	ICU	Interrupt Request Register 063	IR063	8	8		2 ICLK
0008 7040h	ICU	Interrupt Request Register 064	IR064	8	8		2 ICLK
0008 7041h	ICU	Interrupt Request Register 065	IR065	8	8		2 ICLK
0008 7042h	ICU	Interrupt Request Register 066	IR066	8	8		2 ICLK
0008 7043h	ICU	Interrupt Request Register 067	IR067	8	8		2 ICLK
0008 7044h	ICU	Interrupt Request Register 068	IR068	8	8		2 ICLK
0008 7045h	ICU	Interrupt Request Register 069	IR069	8	8		2 ICLK
0008 7046h	ICU	Interrupt Request Register 070	IR070	8	8		2 ICLK
0008 7047h	ICU	Interrupt Request Register 071	IR071	8	8		2 ICLK
0008 7051h	ICU	Interrupt Request Register 081	IR081	8	8		2 ICLK
0008 7058h	ICU	Interrupt Request Register 088	IR088	8	8		2 ICLK
0008 7059h	ICU	Interrupt Request Register 089	IR089	8	8		2 ICLK
0008 705Ah	ICU	Interrupt Request Register 090	IR090	8	8		2 ICLK
0008 705Bh	ICU	Interrupt Request Register 091	IR091	8	8		2 ICLK
0008 705Ch	ICU	Interrupt Request Register 092	IR092	8	8		2 ICLK
0008 705Dh	ICU	Interrupt Request Register 093	IR093	8	8		2 ICLK
0008 7066h	ICU	Interrupt Request Register 102	IR102	8	8		2 ICLK
0008 7067h	ICU	Interrupt Request Register 103	IR103	8	8		2 ICLK
0008 7068h	ICU	Interrupt Request Register 104	IR104	8	8		2 ICLK

Table 4.1 List of I/O Registers (Address Order) (5 / 42)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles	
						ICLK \geq PCLK	ICLK $<$ PCLK
0008 7069h	ICU	Interrupt Request Register 105	IR105	8	8		2 ICLK
0008 706Ah	ICU	Interrupt Request Register 106	IR106	8	8		2 ICLK
0008 706Bh	ICU	Interrupt Request Register 107	IR107	8	8		2 ICLK
0008 706Ch	ICU	Interrupt Request Register 108	IR108	8	8		2 ICLK
0008 706Dh	ICU	Interrupt Request Register 109	IR109	8	8		2 ICLK
0008 706Eh	ICU	Interrupt Request Register 110	IR110	8	8		2 ICLK
0008 706Fh	ICU	Interrupt Request Register 111	IR111	8	8		2 ICLK
0008 7070h	ICU	Interrupt Request Register 112	IR112	8	8		2 ICLK
0008 7071h	ICU	Interrupt Request Register 113	IR113	8	8		2 ICLK
0008 7072h	ICU	Interrupt Request Register 114	IR114	8	8		2 ICLK
0008 7073h	ICU	Interrupt Request Register 115	IR115	8	8		2 ICLK
0008 7074h	ICU	Interrupt Request Register 116	IR116	8	8		2 ICLK
0008 7075h	ICU	Interrupt Request Register 117	IR117	8	8		2 ICLK
0008 7076h	ICU	Interrupt Request Register 118	IR118	8	8		2 ICLK
0008 7077h	ICU	Interrupt Request Register 119	IR119	8	8		2 ICLK
0008 7078h	ICU	Interrupt Request Register 120	IR120	8	8		2 ICLK
0008 7079h	ICU	Interrupt Request Register 121	IR121	8	8		2 ICLK
0008 707Ah	ICU	Interrupt Request Register 122	IR122	8	8		2 ICLK
0008 707Bh	ICU	Interrupt Request Register 123	IR123	8	8		2 ICLK
0008 707Ch	ICU	Interrupt Request Register 124	IR124	8	8		2 ICLK
0008 707Dh	ICU	Interrupt Request Register 125	IR125	8	8		2 ICLK
0008 707Eh	ICU	Interrupt Request Register 126	IR126	8	8		2 ICLK
0008 707Fh	ICU	Interrupt Request Register 127	IR127	8	8		2 ICLK
0008 7080h	ICU	Interrupt Request Register 128	IR128	8	8		2 ICLK
0008 7081h	ICU	Interrupt Request Register 129	IR129	8	8		2 ICLK
0008 7082h	ICU	Interrupt Request Register 130	IR130	8	8		2 ICLK
0008 7083h	ICU	Interrupt Request Register 131	IR131	8	8		2 ICLK
0008 7084h	ICU	Interrupt Request Register 132	IR132	8	8		2 ICLK
0008 7085h	ICU	Interrupt Request Register 133	IR133	8	8		2 ICLK
0008 7086h	ICU	Interrupt Request Register 134	IR134	8	8		2 ICLK
0008 7087h	ICU	Interrupt Request Register 135	IR135	8	8		2 ICLK
0008 7088h	ICU	Interrupt Request Register 136	IR136	8	8		2 ICLK
0008 7089h	ICU	Interrupt Request Register 137	IR137	8	8		2 ICLK
0008 708Ah	ICU	Interrupt Request Register 138	IR138	8	8		2 ICLK
0008 708Bh	ICU	Interrupt Request Register 139	IR139	8	8		2 ICLK
0008 708Ch	ICU	Interrupt Request Register 140	IR140	8	8		2 ICLK
0008 708Dh	ICU	Interrupt Request Register 141	IR141	8	8		2 ICLK
0008 708Eh	ICU	Interrupt Request Register 142	IR142	8	8		2 ICLK
0008 708Fh	ICU	Interrupt Request Register 143	IR143	8	8		2 ICLK
0008 7090h	ICU	Interrupt Request Register 144	IR144	8	8		2 ICLK
0008 7091h	ICU	Interrupt Request Register 145	IR145	8	8		2 ICLK
0008 7092h	ICU	Interrupt Request Register 146	IR146	8	8		2 ICLK
0008 7093h	ICU	Interrupt Request Register 147	IR147	8	8		2 ICLK
0008 7094h	ICU	Interrupt Request Register 148	IR148	8	8		2 ICLK
0008 7095h	ICU	Interrupt Request Register 149	IR149	8	8		2 ICLK
0008 7096h	ICU	Interrupt Request Register 150	IR150	8	8		2 ICLK
0008 7097h	ICU	Interrupt Request Register 151	IR151	8	8		2 ICLK
0008 7098h	ICU	Interrupt Request Register 152	IR152	8	8		2 ICLK
0008 7099h	ICU	Interrupt Request Register 153	IR153	8	8		2 ICLK
0008 709Ah	ICU	Interrupt Request Register 154	IR154	8	8		2 ICLK
0008 709Bh	ICU	Interrupt Request Register 155	IR155	8	8		2 ICLK
0008 709Ch	ICU	Interrupt Request Register 156	IR156	8	8		2 ICLK

Table 4.1 List of I/O Registers (Address Order) (6 / 42)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles	
						ICLK \geq PCLK	ICLK $<$ PCLK
0008 709Dh	ICU	Interrupt Request Register 157	IR157	8	8		2 ICLK
0008 709Eh	ICU	Interrupt Request Register 158	IR158	8	8		2 ICLK
0008 709Fh	ICU	Interrupt Request Register 159	IR159	8	8		2 ICLK
0008 70A0h	ICU	Interrupt Request Register 160	IR160	8	8		2 ICLK
0008 70A1h	ICU	Interrupt Request Register 161	IR161	8	8		2 ICLK
0008 70A2h	ICU	Interrupt Request Register 162	IR162	8	8		2 ICLK
0008 70A3h	ICU	Interrupt Request Register 163	IR163	8	8		2 ICLK
0008 70A4h	ICU	Interrupt Request Register 164	IR164	8	8		2 ICLK
0008 70A5h	ICU	Interrupt Request Register 165	IR165	8	8		2 ICLK
0008 70A6h	ICU	Interrupt Request Register 166	IR166	8	8		2 ICLK
0008 70A7h	ICU	Interrupt Request Register 167	IR167	8	8		2 ICLK
0008 70AAh	ICU	Interrupt Request Register 170	IR170	8	8		2 ICLK
0008 70ABh	ICU	Interrupt Request Register 171	IR171	8	8		2 ICLK
0008 70AEh	ICU	Interrupt Request Register 174	IR174	8	8		2 ICLK
0008 70AFh	ICU	Interrupt Request Register 175	IR175	8	8		2 ICLK
0008 70B0h	ICU	Interrupt Request Register 176	IR176	8	8		2 ICLK
0008 70B1h	ICU	Interrupt Request Register 177	IR177	8	8		2 ICLK
0008 70B2h	ICU	Interrupt Request Register 178	IR178	8	8		2 ICLK
0008 70B3h	ICU	Interrupt Request Register 179	IR179	8	8		2 ICLK
0008 70B4h	ICU	Interrupt Request Register 180	IR180	8	8		2 ICLK
0008 70B5h	ICU	Interrupt Request Register 181	IR181	8	8		2 ICLK
0008 70B6h	ICU	Interrupt Request Register 182	IR182	8	8		2 ICLK
0008 70B7h	ICU	Interrupt Request Register 183	IR183	8	8		2 ICLK
0008 70B8h	ICU	Interrupt Request Register 184	IR184	8	8		2 ICLK
0008 70B9h	ICU	Interrupt Request Register 185	IR185	8	8		2 ICLK
0008 70C6h	ICU	Interrupt Request Register 198	IR198	8	8		2 ICLK
0008 70C7h	ICU	Interrupt Request Register 199	IR199	8	8		2 ICLK
0008 70C8h	ICU	Interrupt Request Register 200	IR200	8	8		2 ICLK
0008 70C9h	ICU	Interrupt Request Register 201	IR201	8	8		2 ICLK
0008 70D6h	ICU	Interrupt Request Register 214	IR214	8	8		2 ICLK
0008 70D7h	ICU	Interrupt Request Register 215	IR215	8	8		2 ICLK
0008 70D8h	ICU	Interrupt Request Register 216	IR216	8	8		2 ICLK
0008 70D9h	ICU	Interrupt Request Register 217	IR217	8	8		2 ICLK
0008 70DAh	ICU	Interrupt Request Register 218	IR218	8	8		2 ICLK
0008 70DBh	ICU	Interrupt Request Register 219	IR219	8	8		2 ICLK
0008 70DCh	ICU	Interrupt Request Register 220	IR220	8	8		2 ICLK
0008 70DDh	ICU	Interrupt Request Register 221	IR221	8	8		2 ICLK
0008 70DEh	ICU	Interrupt Request Register 222	IR222	8	8		2 ICLK
0008 70DFh	ICU	Interrupt Request Register 223	IR223	8	8		2 ICLK
0008 70E0h	ICU	Interrupt Request Register 224	IR224	8	8		2 ICLK
0008 70E1h	ICU	Interrupt Request Register 225	IR225	8	8		2 ICLK
0008 70E2h	ICU	Interrupt Request Register 226	IR226	8	8		2 ICLK
0008 70E3h	ICU	Interrupt Request Register 227	IR227	8	8		2 ICLK
0008 70E4h	ICU	Interrupt Request Register 228	IR228	8	8		2 ICLK
0008 70E5h	ICU	Interrupt Request Register 229	IR229	8	8		2 ICLK
0008 70E6h	ICU	Interrupt Request Register 230	IR230	8	8		2 ICLK
0008 70E7h	ICU	Interrupt Request Register 231	IR231	8	8		2 ICLK
0008 70E8h	ICU	Interrupt Request Register 232	IR232	8	8		2 ICLK
0008 70E9h	ICU	Interrupt Request Register 233	IR233	8	8		2 ICLK
0008 70EAh	ICU	Interrupt Request Register 234	IR234	8	8		2 ICLK
0008 70EBh	ICU	Interrupt Request Register 235	IR235	8	8		2 ICLK
0008 70ECh	ICU	Interrupt Request Register 236	IR236	8	8		2 ICLK

Table 4.1 List of I/O Registers (Address Order) (7 / 42)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles	
						ICLK \geq PCLK	ICLK $<$ PCLK
0008 70EDh	ICU	Interrupt Request Register 237	IR237	8	8		2 ICLK
0008 70EEh	ICU	Interrupt Request Register 238	IR238	8	8		2 ICLK
0008 70EFh	ICU	Interrupt Request Register 239	IR239	8	8		2 ICLK
0008 70F0h	ICU	Interrupt Request Register 240	IR240	8	8		2 ICLK
0008 70F1h	ICU	Interrupt Request Register 241	IR241	8	8		2 ICLK
0008 70F2h	ICU	Interrupt Request Register 242	IR242	8	8		2 ICLK
0008 70F3h	ICU	Interrupt Request Register 243	IR243	8	8		2 ICLK
0008 70F4h	ICU	Interrupt Request Register 244	IR244	8	8		2 ICLK
0008 70F5h	ICU	Interrupt Request Register 245	IR245	8	8		2 ICLK
0008 70F6h	ICU	Interrupt Request Register 246	IR246	8	8		2 ICLK
0008 70F7h	ICU	Interrupt Request Register 247	IR247	8	8		2 ICLK
0008 70F8h	ICU	Interrupt Request Register 248	IR248	8	8		2 ICLK
0008 70F9h	ICU	Interrupt Request Register 249	IR249	8	8		2 ICLK
0008 70FAh	ICU	Interrupt Request Register 250	IR250	8	8		2 ICLK
0008 70FBh	ICU	Interrupt Request Register 251	IR251	8	8		2 ICLK
0008 70FCh	ICU	Interrupt Request Register 252	IR252	8	8		2 ICLK
0008 70FDh	ICU	Interrupt Request Register 253	IR253	8	8		2 ICLK
0008 70FEh	ICU	Interrupt Request Register 254	IR254	8	8		2 ICLK
0008 70FFh	ICU	Interrupt Request Register 255	IR255	8	8		2 ICLK
0008 711Bh	ICU	DTC Activation Enable Register 027	DTCER027	8	8		2 ICLK
0008 711Ch	ICU	DTC Activation Enable Register 028	DTCER028	8	8		2 ICLK
0008 711Dh	ICU	DTC Activation Enable Register 029	DTCER029	8	8		2 ICLK
0008 711Eh	ICU	DTC Activation Enable Register 030	DTCER030	8	8		2 ICLK
0008 711Fh	ICU	DTC Activation Enable Register 031	DTCER031	8	8		2 ICLK
0008 7124h	ICU	DTC Activation Enable Register 036	DTCER036	8	8		2 ICLK
0008 7125h	ICU	DTC Activation Enable Register 037	DTCER037	8	8		2 ICLK
0008 7128h	ICU	DTC Activation Enable Register 040	DTCER040	8	8		2 ICLK
0008 712Dh	ICU	DTC Activation Enable Register 045	DTCER045	8	8		2 ICLK
0008 712Eh	ICU	DTC Activation Enable Register 046	DTCER046	8	8		2 ICLK
0008 7134h	ICU	DTC Activation Enable Register 052	DTCER052	8	8		2 ICLK
0008 713Ah	ICU	DTC Activation Enable Register 058	DTCER058	8	8		2 ICLK
0008 713Bh	ICU	DTC Activation Enable Register 059	DTCER059	8	8		2 ICLK
0008 713Ch	ICU	DTC Activation Enable Register 060	DTCER060	8	8		2 ICLK
0008 713Dh	ICU	DTC Activation Enable Register 061	DTCER061	8	8		2 ICLK
0008 7140h	ICU	DTC Activation Enable Register 064	DTCER064	8	8		2 ICLK
0008 7141h	ICU	DTC Activation Enable Register 065	DTCER065	8	8		2 ICLK
0008 7142h	ICU	DTC Activation Enable Register 066	DTCER066	8	8		2 ICLK
0008 7143h	ICU	DTC Activation Enable Register 067	DTCER067	8	8		2 ICLK
0008 7144h	ICU	DTC Activation Enable Register 068	DTCER068	8	8		2 ICLK
0008 7145h	ICU	DTC Activation Enable Register 069	DTCER069	8	8		2 ICLK
0008 7146h	ICU	DTC Activation Enable Register 070	DTCER070	8	8		2 ICLK
0008 7147h	ICU	DTC Activation Enable Register 071	DTCER071	8	8		2 ICLK
0008 7166h	ICU	DTC Activation Enable Register 102	DTCER102	8	8		2 ICLK
0008 7167h	ICU	DTC Activation Enable Register 103	DTCER103	8	8		2 ICLK
0008 7168h	ICU	DTC Activation Enable Register 104	DTCER104	8	8		2 ICLK
0008 7169h	ICU	DTC Activation Enable Register 105	DTCER105	8	8		2 ICLK
0008 716Ah	ICU	DTC Activation Enable Register 106	DTCER106	8	8		2 ICLK
0008 716Bh	ICU	DTC Activation Enable Register 107	DTCER107	8	8		2 ICLK
0008 716Dh	ICU	DTC Activation Enable Register 109	DTCER109	8	8		2 ICLK
0008 716Eh	ICU	DTC Activation Enable Register 110	DTCER110	8	8		2 ICLK
0008 716Fh	ICU	DTC Activation Enable Register 111	DTCER111	8	8		2 ICLK
0008 7170h	ICU	DTC Activation Enable Register 112	DTCER112	8	8		2 ICLK

Table 4.1 List of I/O Registers (Address Order) (8 / 42)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles	
						ICLK \geq PCLK	ICLK $<$ PCLK
0008 7172h	ICU	DTC Activation Enable Register 114	DTCER114	8	8		2 ICLK
0008 7173h	ICU	DTC Activation Enable Register 115	DTCER115	8	8		2 ICLK
0008 7174h	ICU	DTC Activation Enable Register 116	DTCER116	8	8		2 ICLK
0008 7175h	ICU	DTC Activation Enable Register 117	DTCER117	8	8		2 ICLK
0008 7179h	ICU	DTC Activation Enable Register 121	DTCER121	8	8		2 ICLK
0008 717Ah	ICU	DTC Activation Enable Register 122	DTCER122	8	8		2 ICLK
0008 717Dh	ICU	DTC Activation Enable Register 125	DTCER125	8	8		2 ICLK
0008 717Eh	ICU	DTC Activation Enable Register 126	DTCER126	8	8		2 ICLK
0008 7181h	ICU	DTC Activation Enable Register 129	DTCER129	8	8		2 ICLK
0008 7182h	ICU	DTC Activation Enable Register 130	DTCER130	8	8		2 ICLK
0008 7183h	ICU	DTC Activation Enable Register 131	DTCER131	8	8		2 ICLK
0008 7184h	ICU	DTC Activation Enable Register 132	DTCER132	8	8		2 ICLK
0008 7186h	ICU	DTC Activation Enable Register 134	DTCER134	8	8		2 ICLK
0008 7187h	ICU	DTC Activation Enable Register 135	DTCER135	8	8		2 ICLK
0008 7188h	ICU	DTC Activation Enable Register 136	DTCER136	8	8		2 ICLK
0008 7189h	ICU	DTC Activation Enable Register 137	DTCER137	8	8		2 ICLK
0008 718Ah	ICU	DTC Activation Enable Register 138	DTCER138	8	8		2 ICLK
0008 718Bh	ICU	DTC Activation Enable Register 139	DTCER139	8	8		2 ICLK
0008 718Ch	ICU	DTC Activation Enable Register 140	DTCER140	8	8		2 ICLK
0008 718Dh	ICU	DTC Activation Enable Register 141	DTCER141	8	8		2 ICLK
0008 718Eh	ICU	DTC Activation Enable Register 142	DTCER142	8	8		2 ICLK
0008 7193h	ICU	DTC Activation Enable Register 147	DTCER147	8	8		2 ICLK
0008 7194h	ICU	DTC Activation Enable Register 148	DTCER148	8	8		2 ICLK
0008 7197h	ICU	DTC Activation Enable Register 151	DTCER151	8	8		2 ICLK
0008 7198h	ICU	DTC Activation Enable Register 152	DTCER152	8	8		2 ICLK
0008 719Bh	ICU	DTC Activation Enable Register 155	DTCER155	8	8		2 ICLK
0008 719Ch	ICU	DTC Activation Enable Register 156	DTCER156	8	8		2 ICLK
0008 719Dh	ICU	DTC Activation Enable Register 157	DTCER157	8	8		2 ICLK
0008 719Eh	ICU	DTC Activation Enable Register 158	DTCER158	8	8		2 ICLK
0008 71A0h	ICU	DTC Activation Enable Register 160	DTCER160	8	8		2 ICLK
0008 71A1h	ICU	DTC Activation Enable Register 161	DTCER161	8	8		2 ICLK
0008 71A4h	ICU	DTC Activation Enable Register 164	DTCER164	8	8		2 ICLK
0008 71A5h	ICU	DTC Activation Enable Register 165	DTCER165	8	8		2 ICLK
0008 71AEh	ICU	DTC Activation Enable Register 174	DTCER174	8	8		2 ICLK
0008 71AFh	ICU	DTC Activation Enable Register 175	DTCER175	8	8		2 ICLK
0008 71B1h	ICU	DTC Activation Enable Register 177	DTCER177	8	8		2 ICLK
0008 71B2h	ICU	DTC Activation Enable Register 178	DTCER178	8	8		2 ICLK
0008 71B4h	ICU	DTC Activation Enable Register 180	DTCER180	8	8		2 ICLK
0008 71B5h	ICU	DTC Activation Enable Register 181	DTCER181	8	8		2 ICLK
0008 71B7h	ICU	DTC Activation Enable Register 183	DTCER183	8	8		2 ICLK
0008 71B8h	ICU	DTC Activation Enable Register 184	DTCER184	8	8		2 ICLK
0008 71C6h	ICU	DTC Activation Enable Register 198	DTCER198	8	8		2 ICLK
0008 71C7h	ICU	DTC Activation Enable Register 199	DTCER199	8	8		2 ICLK
0008 71C8h	ICU	DTC Activation Enable Register 200	DTCER200	8	8		2 ICLK
0008 71C9h	ICU	DTC Activation Enable Register 201	DTCER201	8	8		2 ICLK
0008 71D7h	ICU	DTC Activation Enable Register 215	DTCER215	8	8		2 ICLK
0008 71D8h	ICU	DTC Activation Enable Register 216	DTCER216	8	8		2 ICLK
0008 71DBh	ICU	DTC Activation Enable Register 219	DTCER219	8	8		2 ICLK
0008 71DCh	ICU	DTC Activation Enable Register 220	DTCER220	8	8		2 ICLK
0008 71DFh	ICU	DTC Activation Enable Register 223	DTCER223	8	8		2 ICLK
0008 71E0h	ICU	DTC Activation Enable Register 224	DTCER224	8	8		2 ICLK
0008 71E3h	ICU	DTC Activation Enable Register 227	DTCER227	8	8		2 ICLK

Table 4.1 List of I/O Registers (Address Order) (9 / 42)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles	
						ICLK ≥ PCLK	ICLK < PCLK
0008 71E4h	ICU	DTC Activation Enable Register 228	DTCER228	8	8		2 ICLK
0008 71E7h	ICU	DTC Activation Enable Register 231	DTCER231	8	8		2 ICLK
0008 71E8h	ICU	DTC Activation Enable Register 232	DTCER232	8	8		2 ICLK
0008 71EBh	ICU	DTC Activation Enable Register 235	DTCER235	8	8		2 ICLK
0008 71ECh	ICU	DTC Activation Enable Register 236	DTCER236	8	8		2 ICLK
0008 71EFh	ICU	DTC Activation Enable Register 239	DTCER239	8	8		2 ICLK
0008 71F0h	ICU	DTC Activation Enable Register 240	DTCER240	8	8		2 ICLK
0008 71F7h	ICU	DTC Activation Enable Register 247	DTCER247	8	8		2 ICLK
0008 71F8h	ICU	DTC Activation Enable Register 248	DTCER248	8	8		2 ICLK
0008 71FBh	ICU	DTC Activation Enable Register 251	DTCER251	8	8		2 ICLK
0008 71FCh	ICU	DTC Activation Enable Register 252	DTCER252	8	8		2 ICLK
0008 71FDh	ICU	DTC Activation Enable Register 253	DTCER253	8	8		2 ICLK
0008 71FEh	ICU	DTC Activation Enable Register 254	DTCER254	8	8		2 ICLK
0008 71FFh	ICU	DTC Activation Enable Register 255	DTCER255	8	8		2 ICLK
0008 7202h	ICU	Interrupt Request Enable Register 02	IER02	8	8		2 ICLK
0008 7203h	ICU	Interrupt Request Enable Register 03	IER03	8	8		2 ICLK
0008 7204h	ICU	Interrupt Request Enable Register 04	IER04	8	8		2 ICLK
0008 7205h	ICU	Interrupt Request Enable Register 05	IER05	8	8		2 ICLK
0008 7206h	ICU	Interrupt Request Enable Register 06	IER06	8	8		2 ICLK
0008 7207h	ICU	Interrupt Request Enable Register 07	IER07	8	8		2 ICLK
0008 7208h	ICU	Interrupt Request Enable Register 08	IER08	8	8		2 ICLK
0008 720Ah	ICU	Interrupt Request Enable Register 0A	IER0A	8	8		2 ICLK
0008 720Bh	ICU	Interrupt Request Enable Register 0B	IER0B	8	8		2 ICLK
0008 720Ch	ICU	Interrupt Request Enable Register 0C	IER0C	8	8		2 ICLK
0008 720Dh	ICU	Interrupt Request Enable Register 0D	IER0D	8	8		2 ICLK
0008 720Eh	ICU	Interrupt Request Enable Register 0E	IER0E	8	8		2 ICLK
0008 720Fh	ICU	Interrupt Request Enable Register 0F	IER0F	8	8		2 ICLK
0008 7210h	ICU	Interrupt Request Enable Register 10	IER10	8	8		2 ICLK
0008 7211h	ICU	Interrupt Request Enable Register 11	IER11	8	8		2 ICLK
0008 7212h	ICU	Interrupt Request Enable Register 12	IER12	8	8		2 ICLK
0008 7213h	ICU	Interrupt Request Enable Register 13	IER13	8	8		2 ICLK
0008 7214h	ICU	Interrupt Request Enable Register 14	IER14	8	8		2 ICLK
0008 7215h	ICU	Interrupt Request Enable Register 15	IER15	8	8		2 ICLK
0008 7216h	ICU	Interrupt Request Enable Register 16	IER16	8	8		2 ICLK
0008 7217h	ICU	Interrupt Request Enable Register 17	IER17	8	8		2 ICLK
0008 7218h	ICU	Interrupt Request Enable Register 18	IER18	8	8		2 ICLK
0008 7219h	ICU	Interrupt Request Enable Register 19	IER19	8	8		2 ICLK
0008 721Ah	ICU	Interrupt Request Enable Register 1A	IER1A	8	8		2 ICLK
0008 721Bh	ICU	Interrupt Request Enable Register 1B	IER1B	8	8		2 ICLK
0008 721Ch	ICU	Interrupt Request Enable Register 1C	IER1C	8	8		2 ICLK
0008 721Dh	ICU	Interrupt Request Enable Register 1D	IER1D	8	8		2 ICLK
0008 721Eh	ICU	Interrupt Request Enable Register 1E	IER1E	8	8		2 ICLK
0008 721Fh	ICU	Interrupt Request Enable Register 1F	IER1F	8	8		2 ICLK
0008 72E0h	ICU	Software Interrupt Activation Register	SWINTR	8	8		2 ICLK
0008 72F0h	ICU	Fast Interrupt Set Register	FIR	16	16		2 ICLK
0008 7300h	ICU	Interrupt Source Priority Register 000	IPR000	8	8		2 ICLK
0008 7302h	ICU	Interrupt Source Priority Register 002	IPR002	8	8		2 ICLK
0008 7303h	ICU	Interrupt Source Priority Register 003	IPR003	8	8		2 ICLK
0008 7304h	ICU	Interrupt Source Priority Register 004	IPR004	8	8		2 ICLK
0008 7305h	ICU	Interrupt Source Priority Register 005	IPR005	8	8		2 ICLK
0008 7306h	ICU	Interrupt Source Priority Register 006	IPR006	8	8		2 ICLK
0008 7307h	ICU	Interrupt Source Priority Register 007	IPR007	8	8		2 ICLK

Table 4.1 List of I/O Registers (Address Order) (10 / 42)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles	
						ICLK ≥ PCLK	ICLK < PCLK
0008 7320h	ICU	Interrupt Source Priority Register 032	IPR032	8	8		2 ICLK
0008 7321h	ICU	Interrupt Source Priority Register 033	IPR033	8	8		2 ICLK
0008 7322h	ICU	Interrupt Source Priority Register 034	IPR034	8	8		2 ICLK
0008 7324h	ICU	Interrupt Source Priority Register 036	IPR036	8	8		2 ICLK
0008 7325h	ICU	Interrupt Source Priority Register 037	IPR037	8	8		2 ICLK
0008 7326h	ICU	Interrupt Source Priority Register 038	IPR038	8	8		2 ICLK
0008 7328h	ICU	Interrupt Source Priority Register 040	IPR040	8	8		2 ICLK
0008 7329h	ICU	Interrupt Source Priority Register 041	IPR041	8	8		2 ICLK
0008 732Ah	ICU	Interrupt Source Priority Register 042	IPR042	8	8		2 ICLK
0008 732Bh	ICU	Interrupt Source Priority Register 043	IPR043	8	8		2 ICLK
0008 732Ch	ICU	Interrupt Source Priority Register 044	IPR044	8	8		2 ICLK
0008 7334h	ICU	Interrupt Source Priority Register 052	IPR052	8	8		2 ICLK
0008 7335h	ICU	Interrupt Source Priority Register 053	IPR053	8	8		2 ICLK
0008 7336h	ICU	Interrupt Source Priority Register 054	IPR054	8	8		2 ICLK
0008 7337h	ICU	Interrupt Source Priority Register 055	IPR055	8	8		2 ICLK
0008 7338h	ICU	Interrupt Source Priority Register 056	IPR056	8	8		2 ICLK
0008 7339h	ICU	Interrupt Source Priority Register 057	IPR057	8	8		2 ICLK
0008 733Ah	ICU	Interrupt Source Priority Register 058	IPR058	8	8		2 ICLK
0008 733Bh	ICU	Interrupt Source Priority Register 059	IPR059	8	8		2 ICLK
0008 733Ch	ICU	Interrupt Source Priority Register 060	IPR060	8	8		2 ICLK
0008 733Fh	ICU	Interrupt Source Priority Register 063	IPR063	8	8		2 ICLK
0008 7340h	ICU	Interrupt Source Priority Register 064	IPR064	8	8		2 ICLK
0008 7341h	ICU	Interrupt Source Priority Register 065	IPR065	8	8		2 ICLK
0008 7342h	ICU	Interrupt Source Priority Register 066	IPR066	8	8		2 ICLK
0008 7343h	ICU	Interrupt Source Priority Register 067	IPR067	8	8		2 ICLK
0008 7344h	ICU	Interrupt Source Priority Register 068	IPR068	8	8		2 ICLK
0008 7345h	ICU	Interrupt Source Priority Register 069	IPR069	8	8		2 ICLK
0008 7346h	ICU	Interrupt Source Priority Register 070	IPR070	8	8		2 ICLK
0008 7347h	ICU	Interrupt Source Priority Register 071	IPR071	8	8		2 ICLK
0008 7350h	ICU	Interrupt Source Priority Register 080	IPR080	8	8		2 ICLK
0008 7358h	ICU	Interrupt Source Priority Register 088	IPR088	8	8		2 ICLK
0008 7359h	ICU	Interrupt Source Priority Register 089	IPR089	8	8		2 ICLK
0008 735Ch	ICU	Interrupt Source Priority Register 092	IPR092	8	8		2 ICLK
0008 735Dh	ICU	Interrupt Source Priority Register 093	IPR093	8	8		2 ICLK
0008 7366h	ICU	Interrupt Source Priority Register 102	IPR102	8	8		2 ICLK
0008 7367h	ICU	Interrupt Source Priority Register 103	IPR103	8	8		2 ICLK
0008 7368h	ICU	Interrupt Source Priority Register 104	IPR104	8	8		2 ICLK
0008 7369h	ICU	Interrupt Source Priority Register 105	IPR105	8	8		2 ICLK
0008 736Ah	ICU	Interrupt Source Priority Register 106	IPR106	8	8		2 ICLK
0008 736Bh	ICU	Interrupt Source Priority Register 107	IPR107	8	8		2 ICLK
0008 736Ch	ICU	Interrupt Source Priority Register 108	IPR108	8	8		2 ICLK
0008 736Fh	ICU	Interrupt Source Priority Register 111	IPR111	8	8		2 ICLK
0008 7371h	ICU	Interrupt Source Priority Register 113	IPR113	8	8		2 ICLK
0008 7372h	ICU	Interrupt Source Priority Register 114	IPR114	8	8		2 ICLK
0008 7376h	ICU	Interrupt Source Priority Register 118	IPR118	8	8		2 ICLK
0008 7379h	ICU	Interrupt Source Priority Register 121	IPR121	8	8		2 ICLK
0008 737Bh	ICU	Interrupt Source Priority Register 123	IPR123	8	8		2 ICLK
0008 737Dh	ICU	Interrupt Source Priority Register 125	IPR125	8	8		2 ICLK
0008 737Fh	ICU	Interrupt Source Priority Register 127	IPR127	8	8		2 ICLK
0008 7381h	ICU	Interrupt Source Priority Register 129	IPR129	8	8		2 ICLK
0008 7385h	ICU	Interrupt Source Priority Register 133	IPR133	8	8		2 ICLK
0008 7386h	ICU	Interrupt Source Priority Register 134	IPR134	8	8		2 ICLK

Table 4.1 List of I/O Registers (Address Order) (11 / 42)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles	
						ICLK ≥ PCLK	ICLK < PCLK
0008 738Ah	ICU	Interrupt Source Priority Register 138	IPR138	8	8		2 ICLK
0008 738Bh	ICU	Interrupt Source Priority Register 139	IPR139	8	8		2 ICLK
0008 738Eh	ICU	Interrupt Source Priority Register 142	IPR142	8	8		2 ICLK
0008 7392h	ICU	Interrupt Source Priority Register 146	IPR146	8	8		2 ICLK
0008 7393h	ICU	Interrupt Source Priority Register 147	IPR147	8	8		2 ICLK
0008 7395h	ICU	Interrupt Source Priority Register 149	IPR149	8	8		2 ICLK
0008 7397h	ICU	Interrupt Source Priority Register 151	IPR151	8	8		2 ICLK
0008 7399h	ICU	Interrupt Source Priority Register 153	IPR153	8	8		2 ICLK
0008 739Bh	ICU	Interrupt Source Priority Register 155	IPR155	8	8		2 ICLK
0008 739Fh	ICU	Interrupt Source Priority Register 159	IPR159	8	8		2 ICLK
0008 73A0h	ICU	Interrupt Source Priority Register 160	IPR160	8	8		2 ICLK
0008 73A2h	ICU	Interrupt Source Priority Register 162	IPR162	8	8		2 ICLK
0008 73A4h	ICU	Interrupt Source Priority Register 164	IPR164	8	8		2 ICLK
0008 73A6h	ICU	Interrupt Source Priority Register 166	IPR166	8	8		2 ICLK
0008 73AAh	ICU	Interrupt Source Priority Register 170	IPR170	8	8		2 ICLK
0008 73ABh	ICU	Interrupt Source Priority Register 171	IPR171	8	8		2 ICLK
0008 73AEh	ICU	Interrupt Source Priority Register 174	IPR174	8	8		2 ICLK
0008 73B1h	ICU	Interrupt Source Priority Register 177	IPR177	8	8		2 ICLK
0008 73B4h	ICU	Interrupt Source Priority Register 180	IPR180	8	8		2 ICLK
0008 73B7h	ICU	Interrupt Source Priority Register 183	IPR183	8	8		2 ICLK
0008 73C6h	ICU	Interrupt Source Priority Register 198	IPR198	8	8		2 ICLK
0008 73C7h	ICU	Interrupt Source Priority Register 199	IPR199	8	8		2 ICLK
0008 73C8h	ICU	Interrupt Source Priority Register 200	IPR200	8	8		2 ICLK
0008 73C9h	ICU	Interrupt Source Priority Register 201	IPR201	8	8		2 ICLK
0008 73D6h	ICU	Interrupt Source Priority Register 214	IPR214	8	8		2 ICLK
0008 73DAh	ICU	Interrupt Source Priority Register 218	IPR218	8	8		2 ICLK
0008 73DEh	ICU	Interrupt Source Priority Register 222	IPR222	8	8		2 ICLK
0008 73E2h	ICU	Interrupt Source Priority Register 226	IPR226	8	8		2 ICLK
0008 73E6h	ICU	Interrupt Source Priority Register 230	IPR230	8	8		2 ICLK
0008 73EAh	ICU	Interrupt Source Priority Register 234	IPR234	8	8		2 ICLK
0008 73EEh	ICU	Interrupt Source Priority Register 238	IPR238	8	8		2 ICLK
0008 73F2h	ICU	Interrupt Source Priority Register 242	IPR242	8	8		2 ICLK
0008 73F3h	ICU	Interrupt Source Priority Register 243	IPR243	8	8		2 ICLK
0008 73F4h	ICU	Interrupt Source Priority Register 244	IPR244	8	8		2 ICLK
0008 73F5h	ICU	Interrupt Source Priority Register 245	IPR245	8	8		2 ICLK
0008 73F6h	ICU	Interrupt Source Priority Register 246	IPR246	8	8		2 ICLK
0008 73F7h	ICU	Interrupt Source Priority Register 247	IPR247	8	8		2 ICLK
0008 73F8h	ICU	Interrupt Source Priority Register 248	IPR248	8	8		2 ICLK
0008 73F9h	ICU	Interrupt Source Priority Register 249	IPR249	8	8		2 ICLK
0008 73FAh	ICU	Interrupt Source Priority Register 250	IPR250	8	8		2 ICLK
0008 73FBh	ICU	Interrupt Source Priority Register 251	IPR251	8	8		2 ICLK
0008 73FCh	ICU	Interrupt Source Priority Register 252	IPR252	8	8		2 ICLK
0008 73FDh	ICU	Interrupt Source Priority Register 253	IPR253	8	8		2 ICLK
0008 73FEh	ICU	Interrupt Source Priority Register 254	IPR254	8	8		2 ICLK
0008 73FFh	ICU	Interrupt Source Priority Register 255	IPR255	8	8		2 ICLK
0008 7400h	ICU	DMAC Activation Request Select Register 0	DMRSR0	8	8		2 ICLK
0008 7404h	ICU	DMAC Activation Request Select Register 1	DMRSR1	8	8		2 ICLK
0008 7408h	ICU	DMAC Activation Request Select Register 2	DMRSR2	8	8		2 ICLK
0008 740Ch	ICU	DMAC Activation Request Select Register 3	DMRSR3	8	8		2 ICLK
0008 7500h	ICU	IRQ Control Register 0	IRQCR0	8	8		2 ICLK
0008 7501h	ICU	IRQ Control Register 1	IRQCR1	8	8		2 ICLK
0008 7502h	ICU	IRQ Control Register 2	IRQCR2	8	8		2 ICLK

Table 4.1 List of I/O Registers (Address Order) (12 / 42)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles	
						ICLK ≥ PCLK	ICLK < PCLK
0008 7503h	ICU	IRQ Control Register 3	IRQCR3	8	8		2 ICLK
0008 7504h	ICU	IRQ Control Register 4	IRQCR4	8	8		2 ICLK
0008 7505h	ICU	IRQ Control Register 5	IRQCR5	8	8		2 ICLK
0008 7506h	ICU	IRQ Control Register 6	IRQCR6	8	8		2 ICLK
0008 7507h	ICU	IRQ Control Register 7	IRQCR7	8	8		2 ICLK
0008 7510h	ICU	IRQ Pin Digital Filter Enable Register 0	IRQFLTE0	8	8		2 ICLK
0008 7514h	ICU	IRQ Pin Digital Filter Setting Register 0	IRQFLTC0	16	16		2 ICLK
0008 7580h	ICU	Non-Maskable Interrupt Status Register	NMISR	8	8		2 ICLK
0008 7581h	ICU	Non-Maskable Interrupt Enable Register	NMIER	8	8		2 ICLK
0008 7582h	ICU	Non-Maskable Interrupt Status Clear Register	NMICLR	8	8		2 ICLK
0008 7583h	ICU	NMI Pin Interrupt Control Register	NMICR	8	8		2 ICLK
0008 7590h	ICU	NMI Pin Digital Filter Enable Register	NMIFLTE	8	8		2 ICLK
0008 7594h	ICU	NMI Pin Digital Filter Setting Register	NMIFLTC	8	8		2 ICLK
0008 8000h	CMT	Compare Match Timer Start Register 0	CMSTR0	16	16	2 or 3 PCLKB	2 ICLK
0008 8002h	CMT0	Compare Match Timer Control Register	CMCR	16	16	2 or 3 PCLKB	2 ICLK
0008 8004h	CMT0	Compare Match Counter	CMCNT	16	16	2 or 3 PCLKB	2 ICLK
0008 8006h	CMT0	Compare Match Constant Register	CMCOR	16	16	2 or 3 PCLKB	2 ICLK
0008 8008h	CMT1	Compare Match Timer Control Register	CMCR	16	16	2 or 3 PCLKB	2 ICLK
0008 800Ah	CMT1	Compare Match Counter	CMCNT	16	16	2 or 3 PCLKB	2 ICLK
0008 800Ch	CMT1	Compare Match Constant Register	CMCOR	16	16	2 or 3 PCLKB	2 ICLK
0008 8010h	CMT	Compare Match Timer Start Register 1	CMSTR1	16	16	2 or 3 PCLKB	2 ICLK
0008 8012h	CMT2	Compare Match Timer Control Register	CMCR	16	16	2 or 3 PCLKB	2 ICLK
0008 8014h	CMT2	Compare Match Counter	CMCNT	16	16	2 or 3 PCLKB	2 ICLK
0008 8016h	CMT2	Compare Match Constant Register	CMCOR	16	16	2 or 3 PCLKB	2 ICLK
0008 8018h	CMT3	Compare Match Timer Control Register	CMCR	16	16	2 or 3 PCLKB	2 ICLK
0008 801Ah	CMT3	Compare Match Counter	CMCNT	16	16	2 or 3 PCLKB	2 ICLK
0008 801Ch	CMT3	Compare Match Constant Register	CMCOR	16	16	2 or 3 PCLKB	2 ICLK
0008 8020h	WDT	WDT Refresh Register	WDTRR	8	8	2 or 3 PCLKB	2 ICLK
0008 8022h	WDT	WDT Control Register	WDTCR	16	16	2 or 3 PCLKB	2 ICLK
0008 8024h	WDT	WDT Status Register	WDTSR	16	16	2 or 3 PCLKB	2 ICLK
0008 8026h	WDT	WDT Reset Control Register	WDTRCR	8	8	2 or 3 PCLKB	2 ICLK
0008 8030h	IWDT	IWDT Refresh Register	IWDTRR	8	8	2 or 3 PCLKB	2 ICLK
0008 8032h	IWDT	IWDT Control Register	IWDTCR	16	16	2 or 3 PCLKB	2 ICLK
0008 8034h	IWDT	IWDT Status Register	IWDTSR	16	16	2 or 3 PCLKB	2 ICLK
0008 8036h	IWDT	IWDT Reset Control Register	IWDTRCR	8	8	2 or 3 PCLKB	2 ICLK
0008 8038h	IWDT	IWDT Count Stop Control Register	IWDTGSTPR	8	8	2 or 3 PCLKB	2 ICLK
0008 8040h	DA	D/A Data Register 0	DADR0	16	16	2 or 3 PCLKB	2 ICLK
0008 8042h	DA	D/A Data Register 1	DADR1	16	16	2 or 3 PCLKB	2 ICLK
0008 8044h	DA	D/A Control Register	DACR	8	8	2 or 3 PCLKB	2 ICLK
0008 8045h	DA	DADRm Format Select Register	DADPR	8	8	2 or 3 PCLKB	2 ICLK
0008 8046h	DA	D/A A/D Synchronous Start Control Register	DAADSCR	8	8	2 or 3 PCLKB	2 ICLK
0008 8047h	DA	D/A VREF Control Register	DAVREFCR	8	8	2 or 3 PCLKB	2 ICLK
0008 8100h	TPU	Timer Start Register	TSTR	8	8	2 or 3 PCLKB	2 ICLK
0008 8101h	TPU	Timer Synchronous Register	TSYR	8	8	2 or 3 PCLKB	2 ICLK
0008 8108h	TPU0	Noise Filter Control Register	NFCR	8	8	2 or 3 PCLKB	2 ICLK
0008 8109h	TPU1	Noise Filter Control Register	NFCR	8	8	2 or 3 PCLKB	2 ICLK
0008 810Ah	TPU2	Noise Filter Control Register	NFCR	8	8	2 or 3 PCLKB	2 ICLK
0008 810Bh	TPU3	Noise Filter Control Register	NFCR	8	8	2 or 3 PCLKB	2 ICLK
0008 810Ch	TPU4	Noise Filter Control Register	NFCR	8	8	2 or 3 PCLKB	2 ICLK
0008 810Dh	TPU5	Noise Filter Control Register	NFCR	8	8	2 or 3 PCLKB	2 ICLK
0008 8110h	TPU0	Timer Control Register	TCR	8	8	2 or 3 PCLKB	2 ICLK
0008 8111h	TPU0	Timer Mode Register	TMDR	8	8	2 or 3 PCLKB	2 ICLK

Table 4.1 List of I/O Registers (Address Order) (13 / 42)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles	
						ICLK ≥ PCLK	ICLK < PCLK
0008 8112h	TPU0	Timer I/O Control Register H	TIORH	8	8	2 or 3 PCLKB	2 ICLK
0008 8113h	TPU0	Timer I/O Control Register L	TIORL	8	8	2 or 3 PCLKB	2 ICLK
0008 8114h	TPU0	Timer Interrupt Enable Register	TIER	8	8	2 or 3 PCLKB	2 ICLK
0008 8115h	TPU0	Timer Status Register	TSR	8	8	2 or 3 PCLKB	2 ICLK
0008 8116h	TPU0	Timer Counter	TCNT	16	16	2 or 3 PCLKB	2 ICLK
0008 8118h	TPU0	Timer General Register A	TGRA	16	16	2 or 3 PCLKB	2 ICLK
0008 811Ah	TPU0	Timer General Register B	TGRB	16	16	2 or 3 PCLKB	2 ICLK
0008 811Ch	TPU0	Timer General Register C	TGRC	16	16	2 or 3 PCLKB	2 ICLK
0008 811Eh	TPU0	Timer General Register D	TGRD	16	16	2 or 3 PCLKB	2 ICLK
0008 8120h	TPU1	Timer Control Register	TCR	8	8	2 or 3 PCLKB	2 ICLK
0008 8121h	TPU1	Timer Mode Register	TMDR	8	8	2 or 3 PCLKB	2 ICLK
0008 8122h	TPU1	Timer I/O Control Register	TIOR	8	8	2 or 3 PCLKB	2 ICLK
0008 8124h	TPU1	Timer Interrupt Enable Register	TIER	8	8	2 or 3 PCLKB	2 ICLK
0008 8125h	TPU1	Timer Status Register	TSR	8	8	2 or 3 PCLKB	2 ICLK
0008 8126h	TPU1	Timer Counter	TCNT	16	16	2 or 3 PCLKB	2 ICLK
0008 8128h	TPU1	Timer General Register A	TGRA	16	16	2 or 3 PCLKB	2 ICLK
0008 812Ah	TPU1	Timer General Register B	TGRB	16	16	2 or 3 PCLKB	2 ICLK
0008 8130h	TPU2	Timer Control Register	TCR	8	8	2 or 3 PCLKB	2 ICLK
0008 8131h	TPU2	Timer Mode Register	TMDR	8	8	2 or 3 PCLKB	2 ICLK
0008 8132h	TPU2	Timer I/O Control Register	TIOR	8	8	2 or 3 PCLKB	2 ICLK
0008 8134h	TPU2	Timer Interrupt Enable Register	TIER	8	8	2 or 3 PCLKB	2 ICLK
0008 8135h	TPU2	Timer Status Register	TSR	8	8	2 or 3 PCLKB	2 ICLK
0008 8136h	TPU2	Timer Counter	TCNT	16	16	2 or 3 PCLKB	2 ICLK
0008 8138h	TPU2	Timer General Register A	TGRA	16	16	2 or 3 PCLKB	2 ICLK
0008 813Ah	TPU2	Timer General Register B	TGRB	16	16	2 or 3 PCLKB	2 ICLK
0008 8140h	TPU3	Timer Control Register	TCR	8	8	2 or 3 PCLKB	2 ICLK
0008 8141h	TPU3	Timer Mode Register	TMDR	8	8	2 or 3 PCLKB	2 ICLK
0008 8142h	TPU3	Timer I/O Control Register H	TIORH	8	8	2 or 3 PCLKB	2 ICLK
0008 8143h	TPU3	Timer I/O Control Register L	TIORL	8	8	2 or 3 PCLKB	2 ICLK
0008 8144h	TPU3	Timer Interrupt Enable Register	TIER	8	8	2 or 3 PCLKB	2 ICLK
0008 8145h	TPU3	Timer Status Register	TSR	8	8	2 or 3 PCLKB	2 ICLK
0008 8146h	TPU3	Timer Counter	TCNT	16	16	2 or 3 PCLKB	2 ICLK
0008 8148h	TPU3	Timer General Register A	TGRA	16	16	2 or 3 PCLKB	2 ICLK
0008 814Ah	TPU3	Timer General Register B	TGRB	16	16	2 or 3 PCLKB	2 ICLK
0008 814Ch	TPU3	Timer General Register C	TGRC	16	16	2 or 3 PCLKB	2 ICLK
0008 814Eh	TPU3	Timer General Register D	TGRD	16	16	2 or 3 PCLKB	2 ICLK
0008 8150h	TPU4	Timer Control Register	TCR	8	8	2 or 3 PCLKB	2 ICLK
0008 8151h	TPU4	Timer Mode Register	TMDR	8	8	2 or 3 PCLKB	2 ICLK
0008 8152h	TPU4	Timer I/O Control Register	TIOR	8	8	2 or 3 PCLKB	2 ICLK
0008 8154h	TPU4	Timer Interrupt Enable Register	TIER	8	8	2 or 3 PCLKB	2 ICLK
0008 8155h	TPU4	Timer Status Register	TSR	8	8	2 or 3 PCLKB	2 ICLK
0008 8156h	TPU4	Timer Counter	TCNT	16	16	2 or 3 PCLKB	2 ICLK
0008 8158h	TPU4	Timer General Register A	TGRA	16	16	2 or 3 PCLKB	2 ICLK
0008 815Ah	TPU4	Timer General Register B	TGRB	16	16	2 or 3 PCLKB	2 ICLK
0008 8160h	TPU5	Timer Control Register	TCR	8	8	2 or 3 PCLKB	2 ICLK
0008 8161h	TPU5	Timer Mode Register	TMDR	8	8	2 or 3 PCLKB	2 ICLK
0008 8162h	TPU5	Timer I/O Control Register	TIOR	8	8	2 or 3 PCLKB	2 ICLK
0008 8164h	TPU5	Timer Interrupt Enable Register	TIER	8	8	2 or 3 PCLKB	2 ICLK
0008 8165h	TPU5	Timer Status Register	TSR	8	8	2 or 3 PCLKB	2 ICLK
0008 8166h	TPU5	Timer Counter	TCNT	16	16	2 or 3 PCLKB	2 ICLK
0008 8168h	TPU5	Timer General Register A	TGRA	16	16	2 or 3 PCLKB	2 ICLK
0008 816Ah	TPU5	Timer General Register B	TGRB	16	16	2 or 3 PCLKB	2 ICLK

Table 4.1 List of I/O Registers (Address Order) (14 / 42)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles	
						ICLK ≥ PCLK	ICLK < PCLK
0008 8200h	TMR0	Timer Control Register	TCR	8	8	2 or 3 PCLKB	2 ICLK
0008 8201h	TMR1	Timer Control Register	TCR	8	8	2 or 3 PCLKB	2 ICLK
0008 8202h	TMR0	Timer Control/Status Register	TCSR	8	8	2 or 3 PCLKB	2 ICLK
0008 8203h	TMR1	Timer Control/Status Register	TCSR	8	8	2 or 3 PCLKB	2 ICLK
0008 8204h	TMR0	Time Constant Register A	TCORA	8	8	2 or 3 PCLKB	2 ICLK
0008 8205h	TMR1	Time Constant Register A	TCORA	8	8 ^{*1}	2 or 3 PCLKB	2 ICLK
0008 8206h	TMR0	Time Constant Register B	TCORB	8	8	2 or 3 PCLKB	2 ICLK
0008 8207h	TMR1	Time Constant Register B	TCORB	8	8 ^{*1}	2 or 3 PCLKB	2 ICLK
0008 8208h	TMR0	Timer Counter	TCNT	8	8	2 or 3 PCLKB	2 ICLK
0008 8209h	TMR1	Timer Counter	TCNT	8	8 ^{*1}	2 or 3 PCLKB	2 ICLK
0008 820Ah	TMR0	Timer Counter Control Register	TCCR	8	8	2 or 3 PCLKB	2 ICLK
0008 820Bh	TMR1	Timer Counter Control Register	TCCR	8	8 ^{*1}	2 or 3 PCLKB	2 ICLK
0008 820Ch	TMR0	Timer Count Start Register	TCSTR	8	8	2 or 3 PCLKB	2 ICLK
0008 8210h	TMR2	Timer Control Register	TCR	8	8	2 or 3 PCLKB	2 ICLK
0008 8211h	TMR3	Timer Control Register	TCR	8	8	2 or 3 PCLKB	2 ICLK
0008 8212h	TMR2	Timer Control/Status Register	TCSR	8	8	2 or 3 PCLKB	2 ICLK
0008 8213h	TMR3	Timer Control/Status Register	TCSR	8	8	2 or 3 PCLKB	2 ICLK
0008 8214h	TMR2	Time Constant Register A	TCORA	8	8	2 or 3 PCLKB	2 ICLK
0008 8215h	TMR3	Time Constant Register A	TCORA	8	8 ^{*1}	2 or 3 PCLKB	2 ICLK
0008 8216h	TMR2	Time Constant Register B	TCORB	8	8	2 or 3 PCLKB	2 ICLK
0008 8217h	TMR3	Time Constant Register B	TCORB	8	8 ^{*1}	2 or 3 PCLKB	2 ICLK
0008 8218h	TMR2	Timer Counter	TCNT	8	8	2 or 3 PCLKB	2 ICLK
0008 8219h	TMR3	Timer Counter	TCNT	8	8 ^{*1}	2 or 3 PCLKB	2 ICLK
0008 821Ah	TMR2	Timer Counter Control Register	TCCR	8	8	2 or 3 PCLKB	2 ICLK
0008 821Bh	TMR3	Timer Counter Control Register	TCCR	8	8 ^{*1}	2 or 3 PCLKB	2 ICLK
0008 821Ch	TMR2	Timer Count Start Register	TCSTR	8	8	2 or 3 PCLKB	2 ICLK
0008 8280h	CRC	CRC Control Register	CRCCR	8	8	2 or 3 PCLKB	2 ICLK
0008 8281h	CRC	CRC Data Input Register	CRCDIR	8	8	2 or 3 PCLKB	2 ICLK
0008 8282h	CRC	CRC Data Output Register	CRCDOR	16	16	2 or 3 PCLKB	2 ICLK
0008 8300h	RIIC0	I ² C Bus Control Register 1	ICCR1	8	8	2 or 3 PCLKB	2 ICLK
0008 8301h	RIIC0	I ² C Bus Control Register 2	ICCR2	8	8	2 or 3 PCLKB	2 ICLK
0008 8302h	RIIC0	I ² C Bus Mode Register 1	ICMR1	8	8	2 or 3 PCLKB	2 ICLK
0008 8303h	RIIC0	I ² C Bus Mode Register 2	ICMR2	8	8	2 or 3 PCLKB	2 ICLK
0008 8304h	RIIC0	I ² C Bus Mode Register 3	ICMR3	8	8	2 or 3 PCLKB	2 ICLK
0008 8305h	RIIC0	I ² C Bus Function Enable Register	ICFER	8	8	2 or 3 PCLKB	2 ICLK
0008 8306h	RIIC0	I ² C Bus Status Enable Register	ICSER	8	8	2 or 3 PCLKB	2 ICLK
0008 8307h	RIIC0	I ² C Bus Interrupt Enable Register	ICIER	8	8	2 or 3 PCLKB	2 ICLK
0008 8308h	RIIC0	I ² C Bus Status Register 1	ICSR1	8	8	2 or 3 PCLKB	2 ICLK
0008 8309h	RIIC0	I ² C Bus Status Register 2	ICSR2	8	8	2 or 3 PCLKB	2 ICLK
0008 830Ah	RIIC0	Slave Address Register L0	SARL0	8	8	2 or 3 PCLKB	2 ICLK
0008 830Bh	RIIC0	Slave Address Register U0	SARU0	8	8	2 or 3 PCLKB	2 ICLK
0008 830Ch	RIIC0	Slave Address Register L1	SARL1	8	8	2 or 3 PCLKB	2 ICLK
0008 830Dh	RIIC0	Slave Address Register U1	SARU1	8	8	2 or 3 PCLKB	2 ICLK
0008 830Eh	RIIC0	Slave Address Register L2	SARL2	8	8	2 or 3 PCLKB	2 ICLK
0008 830Fh	RIIC0	Slave Address Register U2	SARU2	8	8	2 or 3 PCLKB	2 ICLK
0008 8310h	RIIC0	I ² C Bus Bit Rate Low-Level Register	ICBRL	8	8	2 or 3 PCLKB	2 ICLK
0008 8311h	RIIC0	I ² C Bus Bit Rate High-Level Register	ICBRH	8	8	2 or 3 PCLKB	2 ICLK
0008 8312h	RIIC0	I ² C Bus Transmit Data Register	ICDRT	8	8	2 or 3 PCLKB	2 ICLK
0008 8313h	RIIC0	I ² C Bus Receive Data Register	ICDRR	8	8	2 or 3 PCLKB	2 ICLK
0008 8380h	RSPI0	RSPI Control Register	SPCR	8	8	2 or 3 PCLKB	2 ICLK
0008 8381h	RSPI0	RSPI Slave Select Polarity Register	SSLP	8	8	2 or 3 PCLKB	2 ICLK
0008 8382h	RSPI0	RSPI Pin Control Register	SPPCR	8	8	2 or 3 PCLKB	2 ICLK

Table 4.1 List of I/O Registers (Address Order) (15 / 42)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles	
						ICLK ≥ PCLK	ICLK < PCLK
0008 8383h	RSPI0	RSPI Status Register	SPSR	8	8	2 or 3 PCLKB	2 ICLK
0008 8384h	RSPI0	RSPI Data Register	SPDR	32	16, 32	2 or 3 PCLKB	2 ICLK
0008 8388h	RSPI0	RSPI Sequence Control Register	SPSCR	8	8	2 or 3 PCLKB	2 ICLK
0008 8389h	RSPI0	RSPI Sequence Status Register	SPSSR	8	8	2 or 3 PCLKB	2 ICLK
0008 838Ah	RSPI0	RSPI Bit Rate Register	SPBR	8	8	2 or 3 PCLKB	2 ICLK
0008 838Bh	RSPI0	RSPI Data Control Register	SPDCR	8	8	2 or 3 PCLKB	2 ICLK
0008 838Ch	RSPI0	RSPI Clock Delay Register	SPCKD	8	8	2 or 3 PCLKB	2 ICLK
0008 838Dh	RSPI0	RSPI Slave Select Negation Delay Register	SSLND	8	8	2 or 3 PCLKB	2 ICLK
0008 838Eh	RSPI0	RSPI Next-Access Delay Register	SPND	8	8	2 or 3 PCLKB	2 ICLK
0008 838Fh	RSPI0	RSPI Control Register 2	SPCR2	8	8	2 or 3 PCLKB	2 ICLK
0008 8390h	RSPI0	RSPI Command Register 0	SPCMD0	16	16	2 or 3 PCLKB	2 ICLK
0008 8392h	RSPI0	RSPI Command Register 1	SPCMD1	16	16	2 or 3 PCLKB	2 ICLK
0008 8394h	RSPI0	RSPI Command Register 2	SPCMD2	16	16	2 or 3 PCLKB	2 ICLK
0008 8396h	RSPI0	RSPI Command Register 3	SPCMD3	16	16	2 or 3 PCLKB	2 ICLK
0008 8398h	RSPI0	RSPI Command Register 4	SPCMD4	16	16	2 or 3 PCLKB	2 ICLK
0008 839Ah	RSPI0	RSPI Command Register 5	SPCMD5	16	16	2 or 3 PCLKB	2 ICLK
0008 839Ch	RSPI0	RSPI Command Register 6	SPCMD6	16	16	2 or 3 PCLKB	2 ICLK
0008 839Eh	RSPI0	RSPI Command Register 7	SPCMD7	16	16	2 or 3 PCLKB	2 ICLK
0008 8410h	IrDA	IrDA Control Register	IRCR	8	8	2 or 3 PCLKB	2 ICLK
0008 8900h	POE	Input Level Control/Status Register 1	ICSR1	16	8, 16	2 or 3 PCLKB	2 ICLK
0008 8902h	POE	Output Level Control/Status Register 1	OCSR1	16	8, 16	2 or 3 PCLKB	2 ICLK
0008 8908h	POE	Input Level Control/Status Register 2	ICSR2	16	8, 16	2 or 3 PCLKB	2 ICLK
0008 890Ah	POE	Software Port Output Enable Register	SPOER	8	8	2 or 3 PCLKB	2 ICLK
0008 890Bh	POE	Port Output Enable Control Register 1	POECR1	8	8	2 or 3 PCLKB	2 ICLK
0008 890Ch	POE	Port Output Enable Control Register 2	POECR2	8	8	2 or 3 PCLKB	2 ICLK
0008 890Eh	POE	Input Level Control/Status Register 3	ICSR3	16	8, 16	2 or 3 PCLKB	2 ICLK
0008 9000h	S12AD	A/D Control Register	ADCSR	16	16	2 or 3 PCLKB	2 ICLK
0008 9004h	S12AD	A/D Channel Select Register A0	ADANSA0	16	16	2 or 3 PCLKB	2 ICLK
0008 9006h	S12AD	A/D Channel Select Register A1	ADANSA1	16	16	2 or 3 PCLKB	2 ICLK
0008 9008h	S12AD	A/D-Converted Value Addition/Average Function Select Register 0	ADADS0	16	16	2 or 3 PCLKB	2 ICLK
0008 900Ah	S12AD	A/D-Converted Value Addition/Average Function Select Register 1	ADADS1	16	16	2 or 3 PCLKB	2 ICLK
0008 900Ch	S12AD	A/D-Converted Value Addition/Average Count Select Register	ADADC	8	8	2 or 3 PCLKB	2 ICLK
0008 900Eh	S12AD	A/D Control Extended Register	ADCER	16	16	2 or 3 PCLKB	2 ICLK
0008 9010h	S12AD	A/D Conversion Start Trigger Select Register	ADSTRGR	16	16	2 or 3 PCLKB	2 ICLK
0008 9012h	S12AD	A/D Conversion Extended Input Control Register	ADEXICR	16	16	2 or 3 PCLKB	2 ICLK
0008 9014h	S12AD	A/D Channel Select Register B0	ADANSB0	16	16	2 or 3 PCLKB	2 ICLK
0008 9016h	S12AD	A/D Channel Select Register B1	ADANSB1	16	16	2 or 3 PCLKB	2 ICLK
0008 9018h	S12AD	A/D Data Duplication Register	ADDBLDR	16	16	2 or 3 PCLKB	2 ICLK
0008 901Ah	S12AD	A/D Temperature Sensor Data Register	ADTSDR	16	16	2 or 3 PCLKB	2 ICLK
0008 901Ch	S12AD	A/D Internal Reference Voltage Data Register	ADOCDR	16	16	2 or 3 PCLKB	2 ICLK
0008 901Eh	S12AD	A/D Self-Diagnosis Data Register	ADRD	16	16	2 or 3 PCLKB	2 ICLK
0008 9020h	S12AD	A/D Data Register 0	ADDR0	16	16	2 or 3 PCLKB	2 ICLK
0008 9022h	S12AD	A/D Data Register 1	ADDR1	16	16	2 or 3 PCLKB	2 ICLK
0008 9024h	S12AD	A/D Data Register 2	ADDR2	16	16	2 or 3 PCLKB	2 ICLK
0008 9026h	S12AD	A/D Data Register 3	ADDR3	16	16	2 or 3 PCLKB	2 ICLK
0008 9028h	S12AD	A/D Data Register 4	ADDR4	16	16	2 or 3 PCLKB	2 ICLK
0008 902Ah	S12AD	A/D Data Register 5	ADDR5	16	16	2 or 3 PCLKB	2 ICLK
0008 902Ch	S12AD	A/D Data Register 6	ADDR6	16	16	2 or 3 PCLKB	2 ICLK
0008 902Eh	S12AD	A/D Data Register 7	ADDR7	16	16	2 or 3 PCLKB	2 ICLK
0008 9040h	S12AD	A/D Data Register 16	ADDR16	16	16	2 or 3 PCLKB	2 ICLK

Table 4.1 List of I/O Registers (Address Order) (16 / 42)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles	
						ICLK ≥ PCLK	ICLK < PCLK
0008 9042h	S12AD	A/D Data Register 17	ADDR17	16	16	2 or 3 PCLKB	2 ICLK
0008 9044h	S12AD	A/D Data Register 18	ADDR18	16	16	2 or 3 PCLKB	2 ICLK
0008 9046h	S12AD	A/D Data Register 19	ADDR19	16	16	2 or 3 PCLKB	2 ICLK
0008 9048h	S12AD	A/D Data Register 20	ADDR20	16	16	2 or 3 PCLKB	2 ICLK
0008 904Ah	S12AD	A/D Data Register 21	ADDR21	16	16	2 or 3 PCLKB	2 ICLK
0008 904Ch	S12AD	A/D Data Register 22	ADDR22	16	16	2 or 3 PCLKB	2 ICLK
0008 904Eh	S12AD	A/D Data Register 23	ADDR23	16	16	2 or 3 PCLKB	2 ICLK
0008 9050h	S12AD	A/D Data Register 24	ADDR24	16	16	2 or 3 PCLKB	2 ICLK
0008 9052h	S12AD	A/D Data Register 25	ADDR25	16	16	2 or 3 PCLKB	2 ICLK
0008 9055h	S12AD	A/D Data Register 26	ADDR26	16	16	2 or 3 PCLKB	2 ICLK
0008 9056h	S12AD	A/D Data Register 27	ADDR27	16	16	2 or 3 PCLKB	2 ICLK
0008 9058h	S12AD	A/D Data Register 28	ADDR28	16	16	2 or 3 PCLKB	2 ICLK
0008 905Ah	S12AD	A/D Data Register 29	ADDR29	16	16	2 or 3 PCLKB	2 ICLK
0008 905Ch	S12AD	A/D Data Register 30	ADDR30	16	16	2 or 3 PCLKB	2 ICLK
0008 905Eh	S12AD	A/D Data Register 31	ADDR31	16	16	2 or 3 PCLKB	2 ICLK
0008 907Ah	S12AD	A/D Disconnection Detection Control Register	ADDISCR	8	8	2 or 3 PCLKB	2 ICLK
0008 907Dh	S12AD	A/D Event Link Control Register	ADELCCR	8	8	2 or 3 PCLKB	2 ICLK
0008 9080h	S12AD	A/D Group Scan Priority Control Register	ADGSPCR	16	16	2 or 3 PCLKB	2 ICLK
0008 908Ah	S12AD	A/D High-Side/Low-Side Reference Voltage Control Register	ADHVREFCNT	8	8	2 or 3 PCLKB	2 ICLK
0008 908Ch	S12AD	A/D Compare Function Window A/B Status Monitor Register	ADWINMON	8	8	2 or 3 PCLKB	2 ICLK
0008 9090h	S12AD	A/D Compare Function Control Register	ADCMPCR	16	16	2 or 3 PCLKB	2 ICLK
0008 9092h	S12AD	A/D Compare Function Window A Extended Input Select Register	ADCMPSER	8	8	2 or 3 PCLKB	2 ICLK
0008 9093h	S12AD	A/D Compare Function Window A Extended Input Comparison Condition Setting Register	ADCMPLER	8	8	2 or 3 PCLKB	2 ICLK
0008 9094h	S12AD	A/D Compare Function Window A Channel Select Register 0	ADCMPSR0	16	16	2 or 3 PCLKB	2 ICLK
0008 9096h	S12AD	A/D Compare Function Window A Channel Select Register 1	ADCMPSR1	16	16	2 or 3 PCLKB	2 ICLK
0008 9098h	S12AD	A/D Compare Function Window A Comparison Condition Setting Register 0	ADCMPLR0	16	16	2 or 3 PCLKB	2 ICLK
0008 909Ah	S12AD	A/D Compare Function Window A Comparison Condition Setting Register 1	ADCMPLR1	16	16	2 or 3 PCLKB	2 ICLK
0008 909Ch	S12AD	A/D Compare Function Window A Lower-Side Level Setting Register	ADCMPSR0	16	16	2 or 3 PCLKB	2 ICLK
0008 909Eh	S12AD	A/D Compare Function Window A Upper-Side Level Setting Register	ADCMPSR1	16	16	2 or 3 PCLKB	2 ICLK
0008 90A0h	S12AD	A/D Compare Function Window A Channel Status Register 0	ADCMPSR0	16	16	2 or 3 PCLKB	2 ICLK
0008 90A2h	S12AD	A/D Compare Function Window A Channel Status Register 1	ADCMPSR1	16	16	2 or 3 PCLKB	2 ICLK
0008 90A4h	S12AD	A/D Compare Function Window A Extended Input Channel Status Register	ADCMPSER	16	16	2 or 3 PCLKB	2 ICLK
0008 90A6h	S12AD	A/D Compare Function Window B Channel Select Register	ADCMPSR	8	8	2 or 3 PCLKB	2 ICLK
0008 90A8h	S12AD	A/D Compare Function Window B Lower-Side Level Setting Register	ADWINLLB	16	16	2 or 3 PCLKB	2 ICLK
0008 90AAh	S12AD	A/D Compare Function Window B Upper-Side Level Setting Register	ADWINULB	16	16	2 or 3 PCLKB	2 ICLK
0008 90ACh	S12AD	A/D Compare Function Window B Channel Status Register	ADCMPSR	8	8	2 or 3 PCLKB	2 ICLK
0008 90B0h	S12AD	A/D Data Storage Buffer Register 0	ADBUF0	16	16	2 or 3 PCLKB	2 ICLK
0008 90B2h	S12AD	A/D Data Storage Buffer Register 1	ADBUF1	16	16	2 or 3 PCLKB	2 ICLK
0008 90B4h	S12AD	A/D Data Storage Buffer Register 2	ADBUF2	16	16	2 or 3 PCLKB	2 ICLK
0008 90B6h	S12AD	A/D Data Storage Buffer Register 3	ADBUF3	16	16	2 or 3 PCLKB	2 ICLK
0008 90B8h	S12AD	A/D Data Storage Buffer Register 4	ADBUF4	16	16	2 or 3 PCLKB	2 ICLK
0008 90BAh	S12AD	A/D Data Storage Buffer Register 5	ADBUF5	16	16	2 or 3 PCLKB	2 ICLK
0008 90BCh	S12AD	A/D Data Storage Buffer Register 6	ADBUF6	16	16	2 or 3 PCLKB	2 ICLK
0008 90BEh	S12AD	A/D Data Storage Buffer Register 7	ADBUF7	16	16	2 or 3 PCLKB	2 ICLK

Table 4.1 List of I/O Registers (Address Order) (17 / 42)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles	
						ICLK ≥ PCLK	ICLK < PCLK
0008 90C0h	S12AD	A/D Data Storage Buffer Register 8	ADBUF8	16	16	2 or 3 PCLKB	2 ICLK
0008 90C2h	S12AD	A/D Data Storage Buffer Register 9	ADBUF9	16	16	2 or 3 PCLKB	2 ICLK
0008 90C4h	S12AD	A/D Data Storage Buffer Register 10	ADBUF10	16	16	2 or 3 PCLKB	2 ICLK
0008 90C6h	S12AD	A/D Data Storage Buffer Register 11	ADBUF11	16	16	2 or 3 PCLKB	2 ICLK
0008 90C8h	S12AD	A/D Data Storage Buffer Register 12	ADBUF12	16	16	2 or 3 PCLKB	2 ICLK
0008 90CAh	S12AD	A/D Data Storage Buffer Register 13	ADBUF13	16	16	2 or 3 PCLKB	2 ICLK
0008 90CCh	S12AD	A/D Data Storage Buffer Register 14	ADBUF14	16	16	2 or 3 PCLKB	2 ICLK
0008 90CEh	S12AD	A/D Data Storage Buffer Register 15	ADBUF15	16	16	2 or 3 PCLKB	2 ICLK
0008 90D0h	S12AD	A/D Data Storage Buffer Enable Register	ADBUFEN	8	8	2 or 3 PCLKB	2 ICLK
0008 90D2h	S12AD	A/D Data Storage Buffer Pointer Register	ADBUFPTR	8	8	2 or 3 PCLKB	2 ICLK
0008 90DDh	S12AD	A/D Sampling State Register L	ADSSTRL	8	8	2 or 3 PCLKB	2 ICLK
0008 90DEh	S12AD	A/D Sampling State Register T	ADSSTRT	8	8	2 or 3 PCLKB	2 ICLK
0008 90DFh	S12AD	A/D Sampling State Register O	ADSSTRO	8	8	2 or 3 PCLKB	2 ICLK
0008 90E0h	S12AD	A/D Sampling State Register 0	ADSSTR0	8	8	2 or 3 PCLKB	2 ICLK
0008 90E1h	S12AD	A/D Sampling State Register 1	ADSSTR1	8	8	2 or 3 PCLKB	2 ICLK
0008 90E2h	S12AD	A/D Sampling State Register 2	ADSSTR2	8	8	2 or 3 PCLKB	2 ICLK
0008 90E3h	S12AD	A/D Sampling State Register 3	ADSSTR3	8	8	2 or 3 PCLKB	2 ICLK
0008 90E4h	S12AD	A/D Sampling State Register 4	ADSSTR4	8	8	2 or 3 PCLKB	2 ICLK
0008 90E5h	S12AD	A/D Sampling State Register 5	ADSSTR5	8	8	2 or 3 PCLKB	2 ICLK
0008 90E6h	S12AD	A/D Sampling State Register 6	ADSSTR6	8	8	2 or 3 PCLKB	2 ICLK
0008 90E7h	S12AD	A/D Sampling State Register 7	ADSSTR7	8	8	2 or 3 PCLKB	2 ICLK
0008 A000h	SCI0	Serial Mode Register	SMR	8	8	2 or 3 PCLKB	2 ICLK
0008 A001h	SCI0	Bit Rate Register	BRR	8	8	2 or 3 PCLKB	2 ICLK
0008 A002h	SCI0	Serial Control Register	SCR	8	8	2 or 3 PCLKB	2 ICLK
0008 A003h	SCI0	Transmit Data Register	TDR	8	8	2 or 3 PCLKB	2 ICLK
0008 A004h	SCI0	Serial Status Register	SSR	8	8	2 or 3 PCLKB	2 ICLK
0008 A005h	SCI0	Receive Data Register	RDR	8	8	2 or 3 PCLKB	2 ICLK
0008 A006h	SCI0	Smart Card Mode Register	SCMR	8	8	2 or 3 PCLKB	2 ICLK
0008 A007h	SCI0	Serial Extended Mode Register	SEMR	8	8	2 or 3 PCLKB	2 ICLK
0008 A008h	SCI0	Noise Filter Setting Register	SNFR	8	8	2 or 3 PCLKB	2 ICLK
0008 A009h	SCI0	I ² C Mode Register 1	SIMR1	8	8	2 or 3 PCLKB	2 ICLK
0008 A00Ah	SCI0	I ² C Mode Register 2	SIMR2	8	8	2 or 3 PCLKB	2 ICLK
0008 A00Bh	SCI0	I ² C Mode Register 3	SIMR3	8	8	2 or 3 PCLKB	2 ICLK
0008 A00Ch	SCI0	I ² C Status Register	SISR	8	8	2 or 3 PCLKB	2 ICLK
0008 A00Dh	SCI0	SPI Mode Register	SPMR	8	8	2 or 3 PCLKB	2 ICLK
0008 A00Eh	SCI0	Transmit Data Register HL	TDRHL	16	16	4 or 5 PCLKB	2 ICLK
0008 A00Eh	SCI0	Transmit Data Register H	TDRH	8	8	2 or 3 PCLKB	2 ICLK
0008 A00Fh	SCI0	Transmit Data Register L	TDRL	8	8	2 or 3 PCLKB	2 ICLK
0008 A010h	SCI0	Receive Data Register HL	RDRHL	16	16	4 or 5 PCLKB	2 ICLK
0008 A010h	SCI0	Receive Data Register H	RDRH	8	8	2 or 3 PCLKB	2 ICLK
0008 A011h	SCI0	Receive Data Register L	RDRL	8	8	2 or 3 PCLKB	2 ICLK
0008 A012h	SCI0	Modulation Duty Register	MDDR	8	8	2 or 3 PCLKB	2 ICLK
0008 A020h	SCI1	Serial Mode Register	SMR	8	8	2 or 3 PCLKB	2 ICLK
0008 A021h	SCI1	Bit Rate Register	BRR	8	8	2 or 3 PCLKB	2 ICLK
0008 A022h	SCI1	Serial Control Register	SCR	8	8	2 or 3 PCLKB	2 ICLK
0008 A023h	SCI1	Transmit Data Register	TDR	8	8	2 or 3 PCLKB	2 ICLK
0008 A024h	SCI1	Serial Status Register	SSR	8	8	2 or 3 PCLKB	2 ICLK
0008 A025h	SCI1	Receive Data Register	RDR	8	8	2 or 3 PCLKB	2 ICLK
0008 A026h	SCI1	Smart Card Mode Register	SCMR	8	8	2 or 3 PCLKB	2 ICLK
0008 A027h	SCI1	Serial Extended Mode Register	SEMR	8	8	2 or 3 PCLKB	2 ICLK
0008 A028h	SCI1	Noise Filter Setting Register	SNFR	8	8	2 or 3 PCLKB	2 ICLK
0008 A029h	SCI1	I ² C Mode Register 1	SIMR1	8	8	2 or 3 PCLKB	2 ICLK

Table 4.1 List of I/O Registers (Address Order) (18 / 42)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles	
						ICLK ≥ PCLK	ICLK < PCLK
0008 A02Ah	SCI1	I ² C Mode Register 2	SIMR2	8	8	2 or 3 PCLKB	2 ICLK
0008 A02Bh	SCI1	I ² C Mode Register 3	SIMR3	8	8	2 or 3 PCLKB	2 ICLK
0008 A02Ch	SCI1	I ² C Status Register	SISR	8	8	2 or 3 PCLKB	2 ICLK
0008 A02Dh	SCI1	SPI Mode Register	SPMR	8	8	2 or 3 PCLKB	2 ICLK
0008 A02Eh	SCI1	Transmit Data Register HL	TDRHL	16	16	4 or 5 PCLKB	2 ICLK
0008 A02Eh	SCI1	Transmit Data Register H	TDRH	8	8	2 or 3 PCLKB	2 ICLK
0008 A02Fh	SCI1	Transmit Data Register L	TDRL	8	8	2 or 3 PCLKB	2 ICLK
0008 A030h	SCI1	Receive Data Register HL	RDRHL	16	16	4 or 5 PCLKB	2 ICLK
0008 A030h	SCI1	Receive Data Register H	RDRH	8	8	2 or 3 PCLKB	2 ICLK
0008 A031h	SCI1	Receive Data Register L	RDRL	8	8	2 or 3 PCLKB	2 ICLK
0008 A032h	SCI1	Modulation Duty Register	MDDR	8	8	2 or 3 PCLKB	2 ICLK
0008 A0A0h	SCI5	Serial Mode Register	SMR	8	8	2 or 3 PCLKB	2 ICLK
0008 A0A1h	SCI5	Bit Rate Register	BRR	8	8	2 or 3 PCLKB	2 ICLK
0008 A0A2h	SCI5	Serial Control Register	SCR	8	8	2 or 3 PCLKB	2 ICLK
0008 A0A3h	SCI5	Transmit Data Register	TDR	8	8	2 or 3 PCLKB	2 ICLK
0008 A0A4h	SCI5	Serial Status Register	SSR	8	8	2 or 3 PCLKB	2 ICLK
0008 A0A5h	SCI5	Receive Data Register	RDR	8	8	2 or 3 PCLKB	2 ICLK
0008 A0A6h	SCI5	Smart Card Mode Register	SCMR	8	8	2 or 3 PCLKB	2 ICLK
0008 A0A7h	SCI5	Serial Extended Mode Register	SEMR	8	8	2 or 3 PCLKB	2 ICLK
0008 A0A8h	SCI5	Noise Filter Setting Register	SNFR	8	8	2 or 3 PCLKB	2 ICLK
0008 A0A9h	SCI5	I ² C Mode Register 1	SIMR1	8	8	2 or 3 PCLKB	2 ICLK
0008 A0AAh	SCI5	I ² C Mode Register 2	SIMR2	8	8	2 or 3 PCLKB	2 ICLK
0008 A0ABh	SCI5	I ² C Mode Register 3	SIMR3	8	8	2 or 3 PCLKB	2 ICLK
0008 A0ACh	SCI5	I ² C Status Register	SISR	8	8	2 or 3 PCLKB	2 ICLK
0008 A0ADh	SCI5	SPI Mode Register	SPMR	8	8	2 or 3 PCLKB	2 ICLK
0008 A0AEh	SCI5	Transmit Data Register HL	TDRHL	16	16	4 or 5 PCLKB	2 ICLK
0008 A0AEh	SCI5	Transmit Data Register H	TDRH	8	8	2 or 3 PCLKB	2 ICLK
0008 A0AFh	SCI5	Transmit Data Register L	TDRL	8	8	2 or 3 PCLKB	2 ICLK
0008 A0B0h	SCI5	Receive Data Register HL	RDRHL	16	16	4 or 5 PCLKB	2 ICLK
0008 A0B0h	SCI5	Receive Data Register H	RDRH	8	8	2 or 3 PCLKB	2 ICLK
0008 A0B1h	SCI5	Receive Data Register L	RDRL	8	8	2 or 3 PCLKB	2 ICLK
0008 A0B2h	SCI5	Modulation Duty Register	MDDR	8	8	2 or 3 PCLKB	2 ICLK
0008 A0C0h	SCI6	Serial Mode Register	SMR	8	8	2 or 3 PCLKB	2 ICLK
0008 A0C1h	SCI6	Bit Rate Register	BRR	8	8	2 or 3 PCLKB	2 ICLK
0008 A0C2h	SCI6	Serial Control Register	SCR	8	8	2 or 3 PCLKB	2 ICLK
0008 A0C3h	SCI6	Transmit Data Register	TDR	8	8	2 or 3 PCLKB	2 ICLK
0008 A0C4h	SCI6	Serial Status Register	SSR	8	8	2 or 3 PCLKB	2 ICLK
0008 A0C5h	SCI6	Receive Data Register	RDR	8	8	2 or 3 PCLKB	2 ICLK
0008 A0C6h	SCI6	Smart Card Mode Register	SCMR	8	8	2 or 3 PCLKB	2 ICLK
0008 A0C7h	SCI6	Serial Extended Mode Register	SEMR	8	8	2 or 3 PCLKB	2 ICLK
0008 A0C8h	SCI6	Noise Filter Setting Register	SNFR	8	8	2 or 3 PCLKB	2 ICLK
0008 A0C9h	SCI6	I ² C Mode Register 1	SIMR1	8	8	2 or 3 PCLKB	2 ICLK
0008 A0CAh	SCI6	I ² C Mode Register 2	SIMR2	8	8	2 or 3 PCLKB	2 ICLK
0008 A0CBh	SCI6	I ² C Mode Register 3	SIMR3	8	8	2 or 3 PCLKB	2 ICLK
0008 A0CCh	SCI6	I ² C Status Register	SISR	8	8	2 or 3 PCLKB	2 ICLK
0008 A0CDh	SCI6	SPI Mode Register	SPMR	8	8	2 or 3 PCLKB	2 ICLK
0008 A0CEh	SCI6	Transmit Data Register HL	TDRHL	16	16	4 or 5 PCLKB	2 ICLK
0008 A0CEh	SCI6	Transmit Data Register H	TDRH	8	8	2 or 3 PCLKB	2 ICLK
0008 A0CFh	SCI6	Transmit Data Register L	TDRL	8	8	2 or 3 PCLKB	2 ICLK
0008 A0D0h	SCI6	Receive Data Register HL	RDRHL	16	16	4 or 5 PCLKB	2 ICLK
0008 A0D0h	SCI6	Receive Data Register H	RDRH	8	8	2 or 3 PCLKB	2 ICLK
0008 A0D1h	SCI6	Receive Data Register L	RDRL	8	8	2 or 3 PCLKB	2 ICLK

Table 4.1 List of I/O Registers (Address Order) (19 / 42)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles	
						ICLK ≥ PCLK	ICLK < PCLK
0008 A0D2h	SCI6	Modulation Duty Register	MDDR	8	8	2 or 3 PCLKB	2 ICLK
0008 A100h	SCI8	Serial Mode Register	SMR	8	8	2 or 3 PCLKB	2 ICLK
0008 A101h	SCI8	Bit Rate Register	BRR	8	8	2 or 3 PCLKB	2 ICLK
0008 A102h	SCI8	Serial Control Register	SCR	8	8	2 or 3 PCLKB	2 ICLK
0008 A103h	SCI8	Transmit Data Register	TDR	8	8	2 or 3 PCLKB	2 ICLK
0008 A104h	SCI8	Serial Status Register	SSR	8	8	2 or 3 PCLKB	2 ICLK
0008 A105h	SCI8	Receive Data Register	RDR	8	8	2 or 3 PCLKB	2 ICLK
0008 A106h	SCI8	Smart Card Mode Register	SCMR	8	8	2 or 3 PCLKB	2 ICLK
0008 A107h	SCI8	Serial Extended Mode Register	SEMR	8	8	2 or 3 PCLKB	2 ICLK
0008 A108h	SCI8	Noise Filter Setting Register	SNFR	8	8	2 or 3 PCLKB	2 ICLK
0008 A109h	SCI8	I ² C Mode Register 1	SIMR1	8	8	2 or 3 PCLKB	2 ICLK
0008 A10Ah	SCI8	I ² C Mode Register 2	SIMR2	8	8	2 or 3 PCLKB	2 ICLK
0008 A10Bh	SCI8	I ² C Mode Register 3	SIMR3	8	8	2 or 3 PCLKB	2 ICLK
0008 A10Ch	SCI8	I ² C Status Register	SISR	8	8	2 or 3 PCLKB	2 ICLK
0008 A10Dh	SCI8	SPI Mode Register	SPMR	8	8	2 or 3 PCLKB	2 ICLK
0008 A10Eh	SCI8	Transmit Data Register HL	TDRHL	16	16	4 or 5 PCLKB	2 ICLK
0008 A10Eh	SCI8	Transmit Data Register H	TDRH	8	8	2 or 3 PCLKB	2 ICLK
0008 A10Fh	SCI8	Transmit Data Register L	TDRL	8	8	2 or 3 PCLKB	2 ICLK
0008 A110h	SCI8	Receive Data Register HL	RDRHL	16	16	4 or 5 PCLKB	2 ICLK
0008 A110h	SCI8	Receive Data Register H	RDRH	8	8	2 or 3 PCLKB	2 ICLK
0008 A111h	SCI8	Receive Data Register L	RDRL	8	8	2 or 3 PCLKB	2 ICLK
0008 A112h	SCI8	Modulation Duty Register	MDDR	8	8	2 or 3 PCLKB	2 ICLK
0008 A120h	SCI9	Serial Mode Register	SMR	8	8	2 or 3 PCLKB	2 ICLK
0008 A121h	SCI9	Bit Rate Register	BRR	8	8	2 or 3 PCLKB	2 ICLK
0008 A122h	SCI9	Serial Control Register	SCR	8	8	2 or 3 PCLKB	2 ICLK
0008 A123h	SCI9	Transmit Data Register	TDR	8	8	2 or 3 PCLKB	2 ICLK
0008 A124h	SCI9	Serial Status Register	SSR	8	8	2 or 3 PCLKB	2 ICLK
0008 A125h	SCI9	Receive Data Register	RDR	8	8	2 or 3 PCLKB	2 ICLK
0008 A126h	SCI9	Smart Card Mode Register	SCMR	8	8	2 or 3 PCLKB	2 ICLK
0008 A127h	SCI9	Serial Extended Mode Register	SEMR	8	8	2 or 3 PCLKB	2 ICLK
0008 A128h	SCI9	Noise Filter Setting Register	SNFR	8	8	2 or 3 PCLKB	2 ICLK
0008 A129h	SCI9	I ² C Mode Register 1	SIMR1	8	8	2 or 3 PCLKB	2 ICLK
0008 A12Ah	SCI9	I ² C Mode Register 2	SIMR2	8	8	2 or 3 PCLKB	2 ICLK
0008 A12Bh	SCI9	I ² C Mode Register 3	SIMR3	8	8	2 or 3 PCLKB	2 ICLK
0008 A12Ch	SCI9	I ² C Status Register	SISR	8	8	2 or 3 PCLKB	2 ICLK
0008 A12Dh	SCI9	SPI Mode Register	SPMR	8	8	2 or 3 PCLKB	2 ICLK
0008 A12Eh	SCI9	Transmit Data Register HL	TDRHL	16	16	4 or 5 PCLKB	2 ICLK
0008 A12Eh	SCI9	Transmit Data Register H	TDRH	8	8	2 or 3 PCLKB	2 ICLK
0008 A12Fh	SCI9	Transmit Data Register L	TDRL	8	8	2 or 3 PCLKB	2 ICLK
0008 A130h	SCI9	Receive Data Register HL	RDRHL	16	16	4 or 5 PCLKB	2 ICLK
0008 A130h	SCI9	Receive Data Register H	RDRH	8	8	2 or 3 PCLKB	2 ICLK
0008 A131h	SCI9	Receive Data Register L	RDRL	8	8	2 or 3 PCLKB	2 ICLK
0008 A132h	SCI9	Modulation Duty Register	MDDR	8	8	2 or 3 PCLKB	2 ICLK
0008 A500h	SSI0	Control Register	SSICR	32	32	2 or 3 PCLKB	2 ICLK
0008 A504h	SSI0	Status Register	SSISR	32	32	2 or 3 PCLKB	2 ICLK
0008 A510h	SSI0	FIFO Control Register	SSIFCR	32	32	2 or 3 PCLKB	2 ICLK
0008 A514h	SSI0	FIFO Status Register	SSIFSR	32	32	2 or 3 PCLKB	2 ICLK
0008 A518h	SSI0	Transmit FIFO Data Register	SSIFTDR	32	32	2 or 3 PCLKB	2 ICLK
0008 A51Ch	SSI0	Receive FIFO Data Register	SSIFRDR	32	32	2 or 3 PCLKB	2 ICLK
0008 A520h	SSI0	TDM Mode Register	SSITDMR	32	32	2 or 3 PCLKB	2 ICLK

Table 4.1 List of I/O Registers (Address Order) (20 / 42)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles	
						ICLK ≥ PCLK	ICLK < PCLK
0008 AC00h	SDHI	Command Register	SDCMD	32	32	3 or 4 PCLKB cycles when reading, 2 or 3 PCLKB cycles when writing	3 ICLK cycles when reading, 2 ICLK cycles when writing
0008 AC08h	SDHI	Argument Register	SDARG	32	32	3 or 4 PCLKB cycles when reading, 2 or 3 PCLKB cycles when writing	3 ICLK cycles when reading, 2 ICLK cycles when writing
0008 AC10h	SDHI	Data Stop Register	SDSTOP	32	32	3 or 4 PCLKB cycles when reading, 2 or 3 PCLKB cycles when writing	3 ICLK cycles when reading, 2 ICLK cycles when writing
0008 AC14h	SDHI	Block Count Register	SDBLKCNT	32	32	3 or 4 PCLKB cycles when reading, 2 or 3 PCLKB cycles when writing	3 ICLK cycles when reading, 2 ICLK cycles when writing
0008 AC18h	SDHI	Response Register 10	SDRSP10	32	32	3 or 4 PCLKB cycles when reading, 2 or 3 PCLKB cycles when writing	3 ICLK cycles when reading, 2 ICLK cycles when writing
0008 AC20h	SDHI	Response Register 32	SDRSP32	32	32	3 or 4 PCLKB cycles when reading, 2 or 3 PCLKB cycles when writing	3 ICLK cycles when reading, 2 ICLK cycles when writing
0008 AC28h	SDHI	Response Register 54	SDRSP54	32	32	3 or 4 PCLKB cycles when reading, 2 or 3 PCLKB cycles when writing	3 ICLK cycles when reading, 2 ICLK cycles when writing
0008 AC30h	SDHI	Response Register 76	SDRSP76	32	32	3 or 4 PCLKB cycles when reading, 2 or 3 PCLKB cycles when writing	3 ICLK cycles when reading, 2 ICLK cycles when writing
0008 AC38h	SDHI	SD Status Register 1	SDSTS1	32	32	3 or 4 PCLKB cycles when reading, 2 or 3 PCLKB cycles when writing	3 ICLK cycles when reading, 2 ICLK cycles when writing
0008 AC3Ch	SDHI	SD Status Register 2	SDSTS2	32	32	3 or 4 PCLKB cycles when reading, 2 or 3 PCLKB cycles when writing	3 ICLK cycles when reading, 2 ICLK cycles when writing
0008 AC40h	SDHI	SD Interrupt Mask Register 1	SDIMSK1	32	32	3 or 4 PCLKB cycles when reading, 2 or 3 PCLKB cycles when writing	3 ICLK cycles when reading, 2 ICLK cycles when writing
0008 AC44h	SDHI	SD Interrupt Mask Register 2	SDIMSK2	32	32	3 or 4 PCLKB cycles when reading, 2 or 3 PCLKB cycles when writing	3 ICLK cycles when reading, 2 ICLK cycles when writing
0008 AC48h	SDHI	SDHI Clock Control Register	SDCLKCR	32	32	3 or 4 PCLKB cycles when reading, 2 or 3 PCLKB cycles when writing	3 ICLK cycles when reading, 2 ICLK cycles when writing

Table 4.1 List of I/O Registers (Address Order) (21 / 42)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles	
						ICLK ≥ PCLK	ICLK < PCLK
0008 AC4Ch	SDHI	Transfer Data Size Register	SDSIZE	32	32	3 or 4 PCLKB cycles when reading, 2 or 3 PCLKB cycles when writing	3 ICLK cycles when reading, 2 ICLK cycles when writing
0008 AC50h	SDHI	Card Access Option Register	SDOPT	32	32	3 or 4 PCLKB cycles when reading, 2 or 3 PCLKB cycles when writing	3 ICLK cycles when reading, 2 ICLK cycles when writing
0008 AC58h	SDHI	SD Error Status Register 1	SDERSTS1	32	32	3 or 4 PCLKB cycles when reading, 2 or 3 PCLKB cycles when writing	3 ICLK cycles when reading, 2 ICLK cycles when writing
0008 AC5Ch	SDHI	SD Error Status Register 2	SDERSTS2	32	32	3 or 4 PCLKB cycles when reading, 2 or 3 PCLKB cycles when writing	3 ICLK cycles when reading, 2 ICLK cycles when writing
0008 AC60h	SDHI	SD Buffer Register	SDBUFR	32	32	3 or 4 PCLKB cycles when reading, 2 or 3 PCLKB cycles when writing	3 ICLK cycles when reading, 2 ICLK cycles when writing
0008 AC68h	SDHI	SDIO Mode Control Register	SDIOMD	32	32	3 or 4 PCLKB cycles when reading, 2 or 3 PCLKB cycles when writing	3 ICLK cycles when reading, 2 ICLK cycles when writing
0008 AC6Ch	SDHI	SDIO Status Register	SDIOSTS	32	32	3 or 4 PCLKB cycles when reading, 2 or 3 PCLKB cycles when writing	3 ICLK cycles when reading, 2 ICLK cycles when writing
0008 AC70h	SDHI	SDIO Interrupt Mask Register	SDIOIMSK	32	32	3 or 4 PCLKB cycles when reading, 2 or 3 PCLKB cycles when writing	3 ICLK cycles when reading, 2 ICLK cycles when writing
0008 ADB0h	SDHI	DMA Transfer Enable Register	SDDMAEN	32	32	3 or 4 PCLKB cycles when reading, 2 or 3 PCLKB cycles when writing	3 ICLK cycles when reading, 2 ICLK cycles when writing
0008 ADC0h	SDHI	SDHI Software Reset Register	SDRST	32	32	3 or 4 PCLKB cycles when reading, 2 or 3 PCLKB cycles when writing	3 ICLK cycles when reading, 2 ICLK cycles when writing
0008 ADE0h	SDHI	Swap Control Register	SDSWAP	32	32	3 or 4 PCLKB cycles when reading, 2 or 3 PCLKB cycles when writing	3 ICLK cycles when reading, 2 ICLK cycles when writing
0008 B000h	CAC	CAC Control Register 0	CACR0	8	8	2 or 3 PCLKB	2 ICLK
0008 B001h	CAC	CAC Control Register 1	CACR1	8	8	2 or 3 PCLKB	2 ICLK
0008 B002h	CAC	CAC Control Register 2	CACR2	8	8	2 or 3 PCLKB	2 ICLK
0008 B003h	CAC	CAC Interrupt Request Enable Register	CAICR	8	8	2 or 3 PCLKB	2 ICLK
0008 B004h	CAC	CAC Status Register	CASTR	8	8	2 or 3 PCLKB	2 ICLK
0008 B006h	CAC	CAC Upper-Limit Value Setting Register	CAULVR	16	16	2 or 3 PCLKB	2 ICLK
0008 B008h	CAC	CAC Lower-Limit Value Setting Register	CALLVR	16	16	2 or 3 PCLKB	2 ICLK
0008 B00Ah	CAC	CAC Counter Buffer Register	CACNTBR	16	16	2 or 3 PCLKB	2 ICLK
0008 B080h	DOC	DOC Control Register	DOCR	8	8	2 or 3 PCLKB	2 ICLK
0008 B082h	DOC	DOC Data Input Register	DODIR	16	16	2 or 3 PCLKB	2 ICLK

Table 4.1 List of I/O Registers (Address Order) (22 / 42)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles	
						ICLK ≥ PCLK	ICLK < PCLK
0008 B084h	DOC	DOC Data Setting Register	DODSR	16	16	2 or 3 PCLKB	2 ICLK
0008 B100h	ELC	Event Link Control Register	ELCR	8	8	2 or 3 PCLKB	2 ICLK
0008 B102h	ELC	Event Link Setting Register 1	ELSR1	8	8	2 or 3 PCLKB	2 ICLK
0008 B103h	ELC	Event Link Setting Register 2	ELSR2	8	8	2 or 3 PCLKB	2 ICLK
0008 B104h	ELC	Event Link Setting Register 3	ELSR3	8	8	2 or 3 PCLKB	2 ICLK
0008 B105h	ELC	Event Link Setting Register 4	ELSR4	8	8	2 or 3 PCLKB	2 ICLK
0008 B108h	ELC	Event Link Setting Register 7	ELSR7	8	8	2 or 3 PCLKB	2 ICLK
0008 B109h	ELC	Event Link Setting Register 8	ELSR8	8	8	2 or 3 PCLKB	2 ICLK
0008 B10Bh	ELC	Event Link Setting Register 10	ELSR10	8	8	2 or 3 PCLKB	2 ICLK
0008 B10Dh	ELC	Event Link Setting Register 12	ELSR12	8	8	2 or 3 PCLKB	2 ICLK
0008 B10Fh	ELC	Event Link Setting Register 14	ELSR14	8	8	2 or 3 PCLKB	2 ICLK
0008 B110h	ELC	Event Link Setting Register 15	ELSR15	8	8	2 or 3 PCLKB	2 ICLK
0008 B111h	ELC	Event Link Setting Register 16	ELSR16	8	8	2 or 3 PCLKB	2 ICLK
0008 B113h	ELC	Event Link Setting Register 18	ELSR18	8	8	2 or 3 PCLKB	2 ICLK
0008 B114h	ELC	Event Link Setting Register 19	ELSR19	8	8	2 or 3 PCLKB	2 ICLK
0008 B115h	ELC	Event Link Setting Register 20	ELSR20	8	8	2 or 3 PCLKB	2 ICLK
0008 B116h	ELC	Event Link Setting Register 21	ELSR21	8	8	2 or 3 PCLKB	2 ICLK
0008 B117h	ELC	Event Link Setting Register 22	ELSR22	8	8	2 or 3 PCLKB	2 ICLK
0008 B118h	ELC	Event Link Setting Register 23	ELSR23	8	8	2 or 3 PCLKB	2 ICLK
0008 B119h	ELC	Event Link Setting Register 24	ELSR24	8	8	2 or 3 PCLKB	2 ICLK
0008 B11Ah	ELC	Event Link Setting Register 25	ELSR25	8	8	2 or 3 PCLKB	2 ICLK
0008 B11Bh	ELC	Event Link Setting Register 26	ELSR26	8	8	2 or 3 PCLKB	2 ICLK
0008 B11Ch	ELC	Event Link Setting Register 27	ELSR27	8	8	2 or 3 PCLKB	2 ICLK
0008 B11Dh	ELC	Event Link Setting Register 28	ELSR28	8	8	2 or 3 PCLKB	2 ICLK
0008 B11Eh	ELC	Event Link Setting Register 29	ELSR29	8	8	2 or 3 PCLKB	2 ICLK
0008 B11Fh	ELC	Event Link Option Setting Register A	ELOPA	8	8	2 or 3 PCLKB	2 ICLK
0008 B120h	ELC	Event Link Option Setting Register B	ELOPB	8	8	2 or 3 PCLKB	2 ICLK
0008 B121h	ELC	Event Link Option Setting Register C	ELOPC	8	8	2 or 3 PCLKB	2 ICLK
0008 B122h	ELC	Event Link Option Setting Register D	ELOPD	8	8	2 or 3 PCLKB	2 ICLK
0008 B123h	ELC	Port Group Setting Register 1	PGR1	8	8	2 or 3 PCLKB	2 ICLK
0008 B124h	ELC	Port Group Setting Register 2	PGR2	8	8	2 or 3 PCLKB	2 ICLK
0008 B125h	ELC	Port Group Control Register 1	PGC1	8	8	2 or 3 PCLKB	2 ICLK
0008 B126h	ELC	Port Group Control Register 2	PGC2	8	8	2 or 3 PCLKB	2 ICLK
0008 B127h	ELC	Port Buffer Register 1	PDBF1	8	8	2 or 3 PCLKB	2 ICLK
0008 B128h	ELC	Port Buffer Register 2	PDBF2	8	8	2 or 3 PCLKB	2 ICLK
0008 B129h	ELC	Event Link Port Setting Register 0	PEL0	8	8	2 or 3 PCLKB	2 ICLK
0008 B12Ah	ELC	Event Link Port Setting Register 1	PEL1	8	8	2 or 3 PCLKB	2 ICLK
0008 B12Bh	ELC	Event Link Port Setting Register 2	PEL2	8	8	2 or 3 PCLKB	2 ICLK
0008 B12Ch	ELC	Event Link Port Setting Register 3	PEL3	8	8	2 or 3 PCLKB	2 ICLK
0008 B12Dh	ELC	Event Link Software Event Generation Register	ELSEGR	8	8	2 or 3 PCLKB	2 ICLK
0008 B300h	SCI12	Serial Mode Register	SMR	8	8	2 or 3 PCLKB	2 ICLK
0008 B301h	SCI12	Bit Rate Register	BRR	8	8	2 or 3 PCLKB	2 ICLK
0008 B302h	SCI12	Serial Control Register	SCR	8	8	2 or 3 PCLKB	2 ICLK
0008 B303h	SCI12	Transmit Data Register	TDR	8	8	2 or 3 PCLKB	2 ICLK
0008 B304h	SCI12	Serial Status Register	SSR	8	8	2 or 3 PCLKB	2 ICLK
0008 B305h	SCI12	Receive Data Register	RDR	8	8	2 or 3 PCLKB	2 ICLK
0008 B306h	SCI12	Smart Card Mode Register	SCMR	8	8	2 or 3 PCLKB	2 ICLK
0008 B307h	SCI12	Serial Extended Mode Register	SEMR	8	8	2 or 3 PCLKB	2 ICLK
0008 B308h	SCI12	Noise Filter Setting Register	SNFR	8	8	2 or 3 PCLKB	2 ICLK
0008 B309h	SCI12	I ² C Mode Register 1	SIMR1	8	8	2 or 3 PCLKB	2 ICLK
0008 B30Ah	SCI12	I ² C Mode Register 2	SIMR2	8	8	2 or 3 PCLKB	2 ICLK
0008 B30Bh	SCI12	I ² C Mode Register 3	SIMR3	8	8	2 or 3 PCLKB	2 ICLK

Table 4.1 List of I/O Registers (Address Order) (23 / 42)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles	
						ICLK ≥ PCLK	ICLK < PCLK
0008 B30Ch	SCI12	I ² C Status Register	SISR	8	8	2 or 3 PCLKB	2 ICLK
0008 B30Dh	SCI12	SPI Mode Register	SPMR	8	8	2 or 3 PCLKB	2 ICLK
0008 B30Eh	SCI12	Transmit Data Register HL	TDRHL	16	16	4 or 5 PCLKB	2 ICLK
0008 B30Eh	SCI12	Transmit Data Register H	TDRH	8	8	2 or 3 PCLKB	2 ICLK
0008 B30Fh	SCI12	Transmit Data Register L	TDRL	8	8	2 or 3 PCLKB	2 ICLK
0008 B310h	SCI12	Receive Data Register HL	RDRHL	16	16	4 or 5 PCLKB	2 ICLK
0008 B310h	SCI12	Receive Data Register H	RDRH	8	8	2 or 3 PCLKB	2 ICLK
0008 B311h	SCI12	Receive Data Register L	RDRL	8	8	2 or 3 PCLKB	2 ICLK
0008 B312h	SCI12	Modulation Duty Register	MDDR	8	8	2 or 3 PCLKB	2 ICLK
0008 B320h	SCI12	Extended Serial Module Enable Register	ESMER	8	8	2 or 3 PCLKB	2 ICLK
0008 B321h	SCI12	Control Register 0	CR0	8	8	2 or 3 PCLKB	2 ICLK
0008 B322h	SCI12	Control Register 1	CR1	8	8	2 or 3 PCLKB	2 ICLK
0008 B323h	SCI12	Control Register 2	CR2	8	8	2 or 3 PCLKB	2 ICLK
0008 B324h	SCI12	Control Register 3	CR3	8	8	2 or 3 PCLKB	2 ICLK
0008 B325h	SCI12	Port Control Register	PCR	8	8	2 or 3 PCLKB	2 ICLK
0008 B326h	SCI12	Interrupt Control Register	ICR	8	8	2 or 3 PCLKB	2 ICLK
0008 B327h	SCI12	Status Register	STR	8	8	2 or 3 PCLKB	2 ICLK
0008 B328h	SCI12	Status Clear Register	STCR	8	8	2 or 3 PCLKB	2 ICLK
0008 B329h	SCI12	Control Field 0 Data Register	CF0DR	8	8	2 or 3 PCLKB	2 ICLK
0008 B32Ah	SCI12	Control Field 0 Compare Enable Register	CF0CR	8	8	2 or 3 PCLKB	2 ICLK
0008 B32Bh	SCI12	Control Field 0 Receive Data Register	CF0RR	8	8	2 or 3 PCLKB	2 ICLK
0008 B32Ch	SCI12	Primary Control Field 1 Data Register	PCF1DR	8	8	2 or 3 PCLKB	2 ICLK
0008 B32Dh	SCI12	Secondary Control Field 1 Data Register	SCF1DR	8	8	2 or 3 PCLKB	2 ICLK
0008 B32Eh	SCI12	Control Field 1 Compare Enable Register	CF1CR	8	8	2 or 3 PCLKB	2 ICLK
0008 B32Fh	SCI12	Control Field 1 Receive Data Register	CF1RR	8	8	2 or 3 PCLKB	2 ICLK
0008 B330h	SCI12	Timer Control Register	TCR	8	8	2 or 3 PCLKB	2 ICLK
0008 B331h	SCI12	Timer Mode Register	TMR	8	8	2 or 3 PCLKB	2 ICLK
0008 B332h	SCI12	Timer Prescaler Register	TPRE	8	8	2 or 3 PCLKB	2 ICLK
0008 B333h	SCI12	Timer Count Register	TCNT	8	8	2 or 3 PCLKB	2 ICLK
0008 C000h	PORT0	Port Direction Register	PDR	8	8	2 or 3 PCLKB	2 ICLK
0008 C001h	PORT1	Port Direction Register	PDR	8	8	2 or 3 PCLKB	2 ICLK
0008 C002h	PORT2	Port Direction Register	PDR	8	8	2 or 3 PCLKB	2 ICLK
0008 C003h	PORT3	Port Direction Register	PDR	8	8	2 or 3 PCLKB	2 ICLK
0008 C004h	PORT4	Port Direction Register	PDR	8	8	2 or 3 PCLKB	2 ICLK
0008 C005h	PORT5	Port Direction Register	PDR	8	8	2 or 3 PCLKB	2 ICLK
0008 C00Ah	PORTA	Port Direction Register	PDR	8	8	2 or 3 PCLKB	2 ICLK
0008 C00Bh	PORTB	Port Direction Register	PDR	8	8	2 or 3 PCLKB	2 ICLK
0008 C00Ch	PORTC	Port Direction Register	PDR	8	8	2 or 3 PCLKB	2 ICLK
0008 C00Dh	PORTD	Port Direction Register	PDR	8	8	2 or 3 PCLKB	2 ICLK
0008 C00Eh	PORTE	Port Direction Register	PDR	8	8	2 or 3 PCLKB	2 ICLK
0008 C011h	PORTH	Port Direction Register	PDR	8	8	2 or 3 PCLKB	2 ICLK
0008 C012h	PORTJ	Port Direction Register	PDR	8	8	2 or 3 PCLKB	2 ICLK
0008 C020h	PORT0	Port Output Data Register	PODR	8	8	2 or 3 PCLKB	2 ICLK
0008 C021h	PORT1	Port Output Data Register	PODR	8	8	2 or 3 PCLKB	2 ICLK
0008 C022h	PORT2	Port Output Data Register	PODR	8	8	2 or 3 PCLKB	2 ICLK
0008 C023h	PORT3	Port Output Data Register	PODR	8	8	2 or 3 PCLKB	2 ICLK
0008 C024h	PORT4	Port Output Data Register	PODR	8	8	2 or 3 PCLKB	2 ICLK
0008 C025h	PORT5	Port Output Data Register	PODR	8	8	2 or 3 PCLKB	2 ICLK
0008 C02Ah	PORTA	Port Output Data Register	PODR	8	8	2 or 3 PCLKB	2 ICLK
0008 C02Bh	PORTB	Port Output Data Register	PODR	8	8	2 or 3 PCLKB	2 ICLK
0008 C02Ch	PORTC	Port Output Data Register	PODR	8	8	2 or 3 PCLKB	2 ICLK
0008 C02Dh	PORTD	Port Output Data Register	PODR	8	8	2 or 3 PCLKB	2 ICLK

Table 4.1 List of I/O Registers (Address Order) (24 / 42)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles	
						ICLK ≥ PCLK	ICLK < PCLK
0008 C02Eh	PORTE	Port Output Data Register	PODR	8	8	2 or 3 PCLKB	2 ICLK
0008 C031h	PORTH	Port Output Data Register	PODR	8	8	2 or 3 PCLKB	2 ICLK
0008 C032h	PORTJ	Port Output Data Register	PODR	8	8	2 or 3 PCLKB	2 ICLK
0008 C040h	PORT0	Port Input Data Register	PIDR	8	8	3 or 4 PCLKB cycles when reading, 2 or 3 PCLKB cycles when writing	3 ICLK cycles when reading, 2 ICLK cycles when writing
0008 C041h	PORT1	Port Input Data Register	PIDR	8	8	3 or 4 PCLKB cycles when reading, 2 or 3 PCLKB cycles when writing	3 ICLK cycles when reading, 2 ICLK cycles when writing
0008 C042h	PORT2	Port Input Data Register	PIDR	8	8	3 or 4 PCLKB cycles when reading, 2 or 3 PCLKB cycles when writing	3 ICLK cycles when reading, 2 ICLK cycles when writing
0008 C043h	PORT3	Port Input Data Register	PIDR	8	8	3 or 4 PCLKB cycles when reading, 2 or 3 PCLKB cycles when writing	3 ICLK cycles when reading, 2 ICLK cycles when writing
0008 C044h	PORT4	Port Input Data Register	PIDR	8	8	3 or 4 PCLKB cycles when reading, 2 or 3 PCLKB cycles when writing	3 ICLK cycles when reading, 2 ICLK cycles when writing
0008 C045h	PORT5	Port Input Data Register	PIDR	8	8	3 or 4 PCLKB cycles when reading, 2 or 3 PCLKB cycles when writing	3 ICLK cycles when reading, 2 ICLK cycles when writing
0008 C04Ah	PORTA	Port Input Data Register	PIDR	8	8	3 or 4 PCLKB cycles when reading, 2 or 3 PCLKB cycles when writing	3 ICLK cycles when reading, 2 ICLK cycles when writing
0008 C04Bh	PORTB	Port Input Data Register	PIDR	8	8	3 or 4 PCLKB cycles when reading, 2 or 3 PCLKB cycles when writing	3 ICLK cycles when reading, 2 ICLK cycles when writing
0008 C04Ch	PORTC	Port Input Data Register	PIDR	8	8	3 or 4 PCLKB cycles when reading, 2 or 3 PCLKB cycles when writing	3 ICLK cycles when reading, 2 ICLK cycles when writing
0008 C04Dh	PORTD	Port Input Data Register	PIDR	8	8	3 or 4 PCLKB cycles when reading, 2 or 3 PCLKB cycles when writing	3 ICLK cycles when reading, 2 ICLK cycles when writing
0008 C04Eh	PORTE	Port Input Data Register	PIDR	8	8	3 or 4 PCLKB cycles when reading, 2 or 3 PCLKB cycles when writing	3 ICLK cycles when reading, 2 ICLK cycles when writing
0008 C051h	PORTH	Port Input Data Register	PIDR	8	8	3 or 4 PCLKB cycles when reading, 2 or 3 PCLKB cycles when writing	3 ICLK cycles when reading, 2 ICLK cycles when writing
0008 C052h	PORTJ	Port Input Data Register	PIDR	8	8	3 or 4 PCLKB cycles when reading, 2 or 3 PCLKB cycles when writing	3 ICLK cycles when reading, 2 ICLK cycles when writing
0008 C060h	PORT0	Port Mode Register	PMR	8	8	2 or 3 PCLKB	2 ICLK
0008 C061h	PORT1	Port Mode Register	PMR	8	8	2 or 3 PCLKB	2 ICLK
0008 C062h	PORT2	Port Mode Register	PMR	8	8	2 or 3 PCLKB	2 ICLK
0008 C063h	PORT3	Port Mode Register	PMR	8	8	2 or 3 PCLKB	2 ICLK
0008 C064h	PORT4	Port Mode Register	PMR	8	8	2 or 3 PCLKB	2 ICLK
0008 C065h	PORT5	Port Mode Register	PMR	8	8	2 or 3 PCLKB	2 ICLK
0008 C06Ah	PORTA	Port Mode Register	PMR	8	8	2 or 3 PCLKB	2 ICLK
0008 C06Bh	PORTB	Port Mode Register	PMR	8	8	2 or 3 PCLKB	2 ICLK
0008 C06Ch	PORTC	Port Mode Register	PMR	8	8	2 or 3 PCLKB	2 ICLK
0008 C06Dh	PORTD	Port Mode Register	PMR	8	8	2 or 3 PCLKB	2 ICLK
0008 C06Eh	PORTE	Port Mode Register	PMR	8	8	2 or 3 PCLKB	2 ICLK
0008 C071h	PORTH	Port Mode Register	PMR	8	8	2 or 3 PCLKB	2 ICLK
0008 C072h	PORTJ	Port Mode Register	PMR	8	8	2 or 3 PCLKB	2 ICLK
0008 C082h	PORT1	Open Drain Control Register 0	ODR0	8	8, 16	2 or 3 PCLKB	2 ICLK

Table 4.1 List of I/O Registers (Address Order) (25 / 42)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles	
						ICLK ≥ PCLK	ICLK < PCLK
0008 C083h	PORT1	Open Drain Control Register 1	ODR1	8	8, 16	2 or 3 PCLKB	2 ICLK
0008 C084h	PORT2	Open Drain Control Register 0	ODR0	8	8, 16	2 or 3 PCLKB	2 ICLK
0008 C085h	PORT2	Open Drain Control Register 1	ODR1	8	8, 16	2 or 3 PCLKB	2 ICLK
0008 C086h	PORT3	Open Drain Control Register 0	ODR0	8	8, 16	2 or 3 PCLKB	2 ICLK
0008 C087h	PORT3	Open Drain Control Register 1	ODR1	8	8, 16	2 or 3 PCLKB	2 ICLK
0008 C08Ah	PORT5	Open Drain Control Register 0	ODR0	8	8, 16	2 or 3 PCLKB	2 ICLK
0008 C08Bh	PORT5	Open Drain Control Register 1	ODR1	8	8, 16	2 or 3 PCLKB	2 ICLK
0008 C094h	PORTA	Open Drain Control Register 0	ODR0	8	8, 16	2 or 3 PCLKB	2 ICLK
0008 C095h	PORTA	Open Drain Control Register 1	ODR1	8	8, 16	2 or 3 PCLKB	2 ICLK
0008 C096h	PORTB	Open Drain Control Register 0	ODR0	8	8, 16	2 or 3 PCLKB	2 ICLK
0008 C097h	PORTB	Open Drain Control Register 1	ODR1	8	8, 16	2 or 3 PCLKB	2 ICLK
0008 C098h	PORTC	Open Drain Control Register 0	ODR0	8	8, 16	2 or 3 PCLKB	2 ICLK
0008 C099h	PORTC	Open Drain Control Register 1	ODR1	8	8, 16	2 or 3 PCLKB	2 ICLK
0008 C09Ch	PORTE	Open Drain Control Register 0	ODR0	8	8, 16	2 or 3 PCLKB	2 ICLK
0008 C09Dh	PORTE	Open Drain Control Register 1	ODR1	8	8, 16	2 or 3 PCLKB	2 ICLK
0008 C0A4h	PORTJ	Open Drain Control Register 0	ODR0	8	8, 16	2 or 3 PCLKB	2 ICLK
0008 C0C0h	PORT0	Pull-Up Control Register	PCR	8	8	2 or 3 PCLKB	2 ICLK
0008 C0C1h	PORT1	Pull-Up Control Register	PCR	8	8	2 or 3 PCLKB	2 ICLK
0008 C0C2h	PORT2	Pull-Up Control Register	PCR	8	8	2 or 3 PCLKB	2 ICLK
0008 C0C3h	PORT3	Pull-Up Control Register	PCR	8	8	2 or 3 PCLKB	2 ICLK
0008 C0C4h	PORT4	Pull-Up Control Register	PCR	8	8	2 or 3 PCLKB	2 ICLK
0008 C0C5h	PORT5	Pull-Up Control Register	PCR	8	8	2 or 3 PCLKB	2 ICLK
0008 C0CAh	PORTA	Pull-Up Control Register	PCR	8	8	2 or 3 PCLKB	2 ICLK
0008 C0CBh	PORTB	Pull-Up Control Register	PCR	8	8	2 or 3 PCLKB	2 ICLK
0008 C0CCh	PORTC	Pull-Up Control Register	PCR	8	8	2 or 3 PCLKB	2 ICLK
0008 C0CDh	PORTD	Pull-Up Control Register	PCR	8	8	2 or 3 PCLKB	2 ICLK
0008 C0CEh	PORTE	Pull-Up Control Register	PCR	8	8	2 or 3 PCLKB	2 ICLK
0008 C0D1h	PORTH	Pull-Up Control Register	PCR	8	8	2 or 3 PCLKB	2 ICLK
0008 C0D2h	PORTJ	Pull-Up Control Register	PCR	8	8	2 or 3 PCLKB	2 ICLK
0008 C0E1h	PORT1	Drive Capacity Control Register	DSCR	8	8	2 or 3 PCLKB	2 ICLK
0008 C0E2h	PORT2	Drive Capacity Control Register	DSCR	8	8	2 or 3 PCLKB	2 ICLK
0008 C0E3h	PORT3	Drive Capacity Control Register	DSCR	8	8	2 or 3 PCLKB	2 ICLK
0008 C0E5h	PORT5	Drive Capacity Control Register	DSCR	8	8	2 or 3 PCLKB	2 ICLK
0008 C0EAh	PORTA	Drive Capacity Control Register	DSCR	8	8	2 or 3 PCLKB	2 ICLK
0008 C0EBh	PORTB	Drive Capacity Control Register	DSCR	8	8	2 or 3 PCLKB	2 ICLK
0008 C0ECh	PORTC	Drive Capacity Control Register	DSCR	8	8	2 or 3 PCLKB	2 ICLK
0008 C0EDh	PORTD	Drive Capacity Control Register	DSCR	8	8	2 or 3 PCLKB	2 ICLK
0008 C0EEh	PORTE	Drive Capacity Control Register	DSCR	8	8	2 or 3 PCLKB	2 ICLK
0008 C0F1h	PORTH	Drive Capacity Control Register	DSCR	8	8	2 or 3 PCLKB	2 ICLK
0008 C0F2h	PORTJ	Drive Capacity Control Register	DSCR	8	8	2 or 3 PCLKB	2 ICLK
0008 C100h	MPC	CS Output Enable Register	PFCSE	8	8	2 or 3 PCLKB	2 ICLK
0008 C104h	MPC	Address Output Enable Register 0	PFAOE0	8	8, 16	2 or 3 PCLKB	2 ICLK
0008 C105h	MPC	Address Output Enable Register 1	PFAOE1	8	8, 16	2 or 3 PCLKB	2 ICLK
0008 C106h	MPC	External Bus Control Register 0	PFBCR0	8	8, 16	2 or 3 PCLKB	2 ICLK
0008 C107h	MPC	External Bus Control Register 1	PFBCR1	8	8, 16	2 or 3 PCLKB	2 ICLK
0008 C11Fh	MPC	Write-Protect Register	PWPR	8	8	2 or 3 PCLKB	2 ICLK
0008 C120h	PORT	Port Switching Register B	PSRB	8	8	2 or 3 PCLKB	2 ICLK
0008 C121h	PORT	Port Switching Register A	PSRA	8	8	2 or 3 PCLKB	2 ICLK
0008 C143h	MPC	P03 Pin Function Control Register	P03PFS	8	8	2 or 3 PCLKB	2 ICLK
0008 C145h	MPC	P05 Pin Function Control Register	P05PFS	8	8	2 or 3 PCLKB	2 ICLK
0008 C147h	MPC	P07 Pin Function Control Register	P07PFS	8	8	2 or 3 PCLKB	2 ICLK
0008 C14Ah	MPC	P12 Pin Function Control Register	P12PFS	8	8	2 or 3 PCLKB	2 ICLK

Table 4.1 List of I/O Registers (Address Order) (26 / 42)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles	
						ICLK ≥ PCLK	ICLK < PCLK
0008 C14Bh	MPC	P13 Pin Function Control Register	P13PFS	8	8	2 or 3 PCLKB	2 ICLK
0008 C14Ch	MPC	P14 Pin Function Control Register	P14PFS	8	8	2 or 3 PCLKB	2 ICLK
0008 C14Dh	MPC	P15 Pin Function Control Register	P15PFS	8	8	2 or 3 PCLKB	2 ICLK
0008 C14Eh	MPC	P16 Pin Function Control Register	P16PFS	8	8	2 or 3 PCLKB	2 ICLK
0008 C14Fh	MPC	P17 Pin Function Control Register	P17PFS	8	8	2 or 3 PCLKB	2 ICLK
0008 C150h	MPC	P20 Pin Function Control Register	P20PFS	8	8	2 or 3 PCLKB	2 ICLK
0008 C151h	MPC	P21 Pin Function Control Register	P21PFS	8	8	2 or 3 PCLKB	2 ICLK
0008 C152h	MPC	P22 Pin Function Control Register	P22PFS	8	8	2 or 3 PCLKB	2 ICLK
0008 C153h	MPC	P23 Pin Function Control Register	P23PFS	8	8	2 or 3 PCLKB	2 ICLK
0008 C154h	MPC	P24 Pin Function Control Register	P24PFS	8	8	2 or 3 PCLKB	2 ICLK
0008 C155h	MPC	P25 Pin Function Control Register	P25PFS	8	8	2 or 3 PCLKB	2 ICLK
0008 C156h	MPC	P26 Pin Function Control Register	P26PFS	8	8	2 or 3 PCLKB	2 ICLK
0008 C157h	MPC	P27 Pin Function Control Register	P27PFS	8	8	2 or 3 PCLKB	2 ICLK
0008 C158h	MPC	P30 Pin Function Control Register	P30PFS	8	8	2 or 3 PCLKB	2 ICLK
0008 C159h	MPC	P31 Pin Function Control Register	P31PFS	8	8	2 or 3 PCLKB	2 ICLK
0008 C15Ah	MPC	P32 Pin Function Control Register	P32PFS	8	8	2 or 3 PCLKB	2 ICLK
0008 C15Bh	MPC	P33 Pin Function Control Register	P33PFS	8	8	2 or 3 PCLKB	2 ICLK
0008 C15Ch	MPC	P34 Pin Function Control Register	P34PFS	8	8	2 or 3 PCLKB	2 ICLK
0008 C160h	MPC	P40 Pin Function Control Register	P40PFS	8	8	2 or 3 PCLKB	2 ICLK
0008 C161h	MPC	P41 Pin Function Control Register	P41PFS	8	8	2 or 3 PCLKB	2 ICLK
0008 C162h	MPC	P42 Pin Function Control Register	P42PFS	8	8	2 or 3 PCLKB	2 ICLK
0008 C163h	MPC	P43 Pin Function Control Register	P43PFS	8	8	2 or 3 PCLKB	2 ICLK
0008 C164h	MPC	P44 Pin Function Control Register	P44PFS	8	8	2 or 3 PCLKB	2 ICLK
0008 C165h	MPC	P45 Pin Function Control Register	P45PFS	8	8	2 or 3 PCLKB	2 ICLK
0008 C166h	MPC	P46 Pin Function Control Register	P46PFS	8	8	2 or 3 PCLKB	2 ICLK
0008 C167h	MPC	P47 Pin Function Control Register	P47PFS	8	8	2 or 3 PCLKB	2 ICLK
0008 C168h	MPC	P50 Pin Function Control Register	P50PFS	8	8	2 or 3 PCLKB	2 ICLK
0008 C169h	MPC	P51 Pin Function Control Register	P51PFS	8	8	2 or 3 PCLKB	2 ICLK
0008 C16Ah	MPC	P52 Pin Function Control Register	P52PFS	8	8	2 or 3 PCLKB	2 ICLK
0008 C16Bh	MPC	P53 Pin Function Control Register	P53PFS	8	8	2 or 3 PCLKB	2 ICLK
0008 C16Ch	MPC	P54 Pin Function Control Register	P54PFS	8	8	2 or 3 PCLKB	2 ICLK
0008 C16Dh	MPC	P55 Pin Function Control Register	P55PFS	8	8	2 or 3 PCLKB	2 ICLK
0008 C190h	MPC	PA0 Pin Function Control Register	PA0PFS	8	8	2 or 3 PCLKB	2 ICLK
0008 C191h	MPC	PA1 Pin Function Control Register	PA1PFS	8	8	2 or 3 PCLKB	2 ICLK
0008 C192h	MPC	PA2 Pin Function Control Register	PA2PFS	8	8	2 or 3 PCLKB	2 ICLK
0008 C193h	MPC	PA3 Pin Function Control Register	PA3PFS	8	8	2 or 3 PCLKB	2 ICLK
0008 C194h	MPC	PA4 Pin Function Control Register	PA4PFS	8	8	2 or 3 PCLKB	2 ICLK
0008 C195h	MPC	PA5 Pin Function Control Register	PA5PFS	8	8	2 or 3 PCLKB	2 ICLK
0008 C196h	MPC	PA6 Pin Function Control Register	PA6PFS	8	8	2 or 3 PCLKB	2 ICLK
0008 C197h	MPC	PA7 Pin Function Control Register	PA7PFS	8	8	2 or 3 PCLKB	2 ICLK
0008 C198h	MPC	PB0 Pin Function Control Register	PB0PFS	8	8	2 or 3 PCLKB	2 ICLK
0008 C199h	MPC	PB1 Pin Function Control Register	PB1PFS	8	8	2 or 3 PCLKB	2 ICLK
0008 C19Ah	MPC	PB2 Pin Function Control Register	PB2PFS	8	8	2 or 3 PCLKB	2 ICLK
0008 C19Bh	MPC	PB3 Pin Function Control Register	PB3PFS	8	8	2 or 3 PCLKB	2 ICLK
0008 C19Ch	MPC	PB4 Pin Function Control Register	PB4PFS	8	8	2 or 3 PCLKB	2 ICLK
0008 C19Dh	MPC	PB5 Pin Function Control Register	PB5PFS	8	8	2 or 3 PCLKB	2 ICLK
0008 C19Eh	MPC	PB6 Pin Function Control Register	PB6PFS	8	8	2 or 3 PCLKB	2 ICLK
0008 C19Fh	MPC	PB7 Pin Function Control Register	PB7PFS	8	8	2 or 3 PCLKB	2 ICLK
0008 C1A0h	MPC	PC0 Pin Function Control Register	PC0PFS	8	8	2 or 3 PCLKB	2 ICLK
0008 C1A1h	MPC	PC1 Pin Function Control Register	PC1PFS	8	8	2 or 3 PCLKB	2 ICLK
0008 C1A2h	MPC	PC2 Pin Function Control Register	PC2PFS	8	8	2 or 3 PCLKB	2 ICLK
0008 C1A3h	MPC	PC3 Pin Function Control Register	PC3PFS	8	8	2 or 3 PCLKB	2 ICLK

Table 4.1 List of I/O Registers (Address Order) (27 / 42)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles	
						ICLK ≥ PCLK	ICLK < PCLK
0008 C1A4h	MPC	PC4 Pin Function Control Register	PC4PFS	8	8	2 or 3 PCLKB	2 ICLK
0008 C1A5h	MPC	PC5 Pin Function Control Register	PC5PFS	8	8	2 or 3 PCLKB	2 ICLK
0008 C1A6h	MPC	PC6 Pin Function Control Register	PC6PFS	8	8	2 or 3 PCLKB	2 ICLK
0008 C1A7h	MPC	PC7 Pin Function Control Register	PC7PFS	8	8	2 or 3 PCLKB	2 ICLK
0008 C1A8h	MPC	PD0 Pin Function Control Register	PD0PFS	8	8	2 or 3 PCLKB	2 ICLK
0008 C1A9h	MPC	PD1 Pin Function Control Register	PD1PFS	8	8	2 or 3 PCLKB	2 ICLK
0008 C1AAh	MPC	PD2 Pin Function Control Register	PD2PFS	8	8	2 or 3 PCLKB	2 ICLK
0008 C1ABh	MPC	PD3 Pin Function Control Register	PD3PFS	8	8	2 or 3 PCLKB	2 ICLK
0008 C1ACh	MPC	PD4 Pin Function Control Register	PD4PFS	8	8	2 or 3 PCLKB	2 ICLK
0008 C1ADh	MPC	PD5 Pin Function Control Register	PD5PFS	8	8	2 or 3 PCLKB	2 ICLK
0008 C1AEh	MPC	PD6 Pin Function Control Register	PD6PFS	8	8	2 or 3 PCLKB	2 ICLK
0008 C1AFh	MPC	PD7 Pin Function Control Register	PD7PFS	8	8	2 or 3 PCLKB	2 ICLK
0008 C1B0h	MPC	PE0 Pin Function Control Register	PE0PFS	8	8	2 or 3 PCLKB	2 ICLK
0008 C1B1h	MPC	PE1 Pin Function Control Register	PE1PFS	8	8	2 or 3 PCLKB	2 ICLK
0008 C1B2h	MPC	PE2 Pin Function Control Register	PE2PFS	8	8	2 or 3 PCLKB	2 ICLK
0008 C1B3h	MPC	PE3 Pin Function Control Register	PE3PFS	8	8	2 or 3 PCLKB	2 ICLK
0008 C1B4h	MPC	PE4 Pin Function Control Register	PE4PFS	8	8	2 or 3 PCLKB	2 ICLK
0008 C1B5h	MPC	PE5 Pin Function Control Register	PE5PFS	8	8	2 or 3 PCLKB	2 ICLK
0008 C1B6h	MPC	PE6 Pin Function Control Register	PE6PFS	8	8	2 or 3 PCLKB	2 ICLK
0008 C1B7h	MPC	PE7 Pin Function Control Register	PE7PFS	8	8	2 or 3 PCLKB	2 ICLK
0008 C1C8h	MPC	PH0 Pin Function Control Register	PH0PFS	8	8	2 or 3 PCLKB	2 ICLK
0008 C1C9h	MPC	PH1 Pin Function Control Register	PH1PFS	8	8	2 or 3 PCLKB	2 ICLK
0008 C1CAh	MPC	PH2 Pin Function Control Register	PH2PFS	8	8	2 or 3 PCLKB	2 ICLK
0008 C1CBh	MPC	PH3 Pin Function Control Register	PH3PFS	8	8	2 or 3 PCLKB	2 ICLK
0008 C1D3h	MPC	PJ3 Pin Function Control Register	PJ3PFS	8	8	2 or 3 PCLKB	2 ICLK
0008 C290h	SYSTEM	Reset Status Register 0	RSTSR0	8	8	4 or 5 PCLKB	2 or 3 ICLK
0008 C291h	SYSTEM	Reset Status Register 1	RSTSR1	8	8	4 or 5 PCLKB	2 or 3 ICLK
0008 C293h	SYSTEM	Main Clock Oscillator Forced Oscillation Control Register	MOFCR	8	8	4 or 5 PCLKB	2 or 3 ICLK
0008 C297h	SYSTEM	Voltage Monitoring Circuit Control Register	LVMPCR	8	8	4 or 5 PCLKB	2 or 3 ICLK
0008 C298h	SYSTEM	Voltage Detection Level Select Register	LVDLVL	8	8	4 or 5 PCLKB	2 or 3 ICLK
0008 C29Ah	SYSTEM	Voltage Monitoring 1 Circuit Control Register 0	LVD1CR0	8	8	4 or 5 PCLKB	2 or 3 ICLK
0008 C29Bh	SYSTEM	Voltage Monitoring 2 Circuit Control Register 0	LVD2CR0	8	8	4 or 5 PCLKB	2 or 3 ICLK
0008 C29Dh	SYSTEM	VBATT Control Register	VBATTCT	8	8	4 or 5 PCLKB	2 or 3 ICLK
0008 C29Eh	SYSTEM	VBATT Status Register	VBATTST	8	8	4 or 5 PCLKB	2 or 3 ICLK
0008 C29Fh	SYSTEM	VBATT Pin Voltage Drop Detection Interrupt Control Register	VBTLVDICR	8	8	4 or 5 PCLKB	2 or 3 ICLK
0008 C400h	RTC	64-Hz Counter	R64CNT	8	8	2 or 3 PCLKB	2 ICLK
0008 C402h	RTC	Second Counter	RSECCNT	8	8	2 or 3 PCLKB	2 ICLK
0008 C402h	RTC	Binary Counter 0	BCNT0	8	8	2 or 3 PCLKB	2 ICLK
0008 C404h	RTC	Minute Counter	RMINCNT	8	8	2 or 3 PCLKB	2 ICLK
0008 C404h	RTC	Binary Counter 1	BCNT1	8	8	2 or 3 PCLKB	2 ICLK
0008 C406h	RTC	Hour Counter	RHRCNT	8	8	2 or 3 PCLKB	2 ICLK
0008 C406h	RTC	Binary Counter 2	BCNT2	8	8	2 or 3 PCLKB	2 ICLK
0008 C408h	RTC	Day-of-Week Counter	RWKCNT	8	8	2 or 3 PCLKB	2 ICLK
0008 C408h	RTC	Binary Counter 3	BCNT3	8	8	2 or 3 PCLKB	2 ICLK
0008 C40Ah	RTC	Date Counter	RDAYCNT	8	8	2 or 3 PCLKB	2 ICLK
0008 C40Ch	RTC	Month Counter	RMONCNT	8	8	2 or 3 PCLKB	2 ICLK
0008 C40Eh	RTC	Year Counter	RYRCNT	16	16	2 or 3 PCLKB	2 ICLK
0008 C410h	RTC	Second Alarm Register	RSECAR	8	8	2 or 3 PCLKB	2 ICLK
0008 C410h	RTC	Binary Counter 0 Alarm Register	BCNT0AR	8	8	2 or 3 PCLKB	2 ICLK
0008 C412h	RTC	Minute Alarm Register	RMINAR	8	8	2 or 3 PCLKB	2 ICLK
0008 C412h	RTC	Binary Counter 1 Alarm Register	BCNT1AR	8	8	2 or 3 PCLKB	2 ICLK

Table 4.1 List of I/O Registers (Address Order) (28 / 42)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles	
						ICLK ≥ PCLK	ICLK < PCLK
0008 C414h	RTC	Hour Alarm Register	RHRAR	8	8	2 or 3 PCLKB	2 ICLK
0008 C414h	RTC	Binary Counter 2 Alarm Register	BCNT2AR	8	8	2 or 3 PCLKB	2 ICLK
0008 C416h	RTC	Day-of-Week Alarm Register	RWKAR	8	8	2 or 3 PCLKB	2 ICLK
0008 C416h	RTC	Binary Counter 3 Alarm Register	BCNT3AR	8	8	2 or 3 PCLKB	2 ICLK
0008 C418h	RTC	Date Alarm Register	RDAYAR	8	8	2 or 3 PCLKB	2 ICLK
0008 C418h	RTC	Binary Counter 0 Alarm Enable Register	BCNT0AER	8	8	2 or 3 PCLKB	2 ICLK
0008 C41Ah	RTC	Month Alarm Register	RMONAR	8	8	2 or 3 PCLKB	2 ICLK
0008 C41Ah	RTC	Binary Counter 1 Alarm Enable Register	BCNT1AER	8	8	2 or 3 PCLKB	2 ICLK
0008 C41Ch	RTC	Year Alarm Register	RYRAR	16	16	2 or 3 PCLKB	2 ICLK
0008 C41Ch	RTC	Binary Counter 2 Alarm Enable Register	BCNT2AER	16	16	2 or 3 PCLKB	2 ICLK
0008 C41Eh	RTC	Year Alarm Enable Register	RYRAREN	8	8	2 or 3 PCLKB	2 ICLK
0008 C41Eh	RTC	Binary Counter 3 Alarm Enable Register	BCNT3AER	8	8	2 or 3 PCLKB	2 ICLK
0008 C422h	RTC	RTC Control Register 1	RCR1	8	8	2 or 3 PCLKB	2 ICLK
0008 C424h	RTC	RTC Control Register 2	RCR2	8	8	2 or 3 PCLKB	2 ICLK
0008 C426h	RTC	RTC Control Register 3	RCR3	8	8	2 or 3 PCLKB	2 ICLK
0008 C42Eh	RTC	Time Error Adjustment Register	RADJ	8	8	2 or 3 PCLKB	2 ICLK
0008 C440h	RTC	Time Capture Control Register 0	RTCCR0	8	8	2 or 3 PCLKB	2 ICLK
0008 C442h	RTC	Time Capture Control Register 1	RTCCR1	8	8	2 or 3 PCLKB	2 ICLK
0008 C444h	RTC	Time Capture Control Register 2	RTCCR2	8	8	2 or 3 PCLKB	2 ICLK
0008 C452h	RTC	Second Capture Register 0	RSECCP0	8	8	2 or 3 PCLKB	2 ICLK
0008 C452h	RTC	BCNT0 Capture Register 0	BCNT0CP0	8	8	2 or 3 PCLKB	2 ICLK
0008 C454h	RTC	Minute Capture Register 0	RMINCP0	8	8	2 or 3 PCLKB	2 ICLK
0008 C454h	RTC	BCNT1 Capture Register 0	BCNT1CP0	8	8	2 or 3 PCLKB	2 ICLK
0008 C456h	RTC	Hour Capture Register 0	RHRCP0	8	8	2 or 3 PCLKB	2 ICLK
0008 C456h	RTC	BCNT2 Capture Register 0	BCNT2CP0	8	8	2 or 3 PCLKB	2 ICLK
0008 C45Ah	RTC	Date Capture Register 0	RDAYCP0	8	8	2 or 3 PCLKB	2 ICLK
0008 C45Ah	RTC	BCNT3 Capture Register 0	BCNT3CP0	8	8	2 or 3 PCLKB	2 ICLK
0008 C45Ch	RTC	Month Capture Register 0	RMONCP0	8	8	2 or 3 PCLKB	2 ICLK
0008 C462h	RTC	Second Capture Register 1	RSECCP1	8	8	2 or 3 PCLKB	2 ICLK
0008 C462h	RTC	BCNT0 Capture Register 1	BCNT0CP1	8	8	2 or 3 PCLKB	2 ICLK
0008 C464h	RTC	Minute Capture Register 1	RMINCP1	8	8	2 or 3 PCLKB	2 ICLK
0008 C464h	RTC	BCNT1 Capture Register 1	BCNT1CP1	8	8	2 or 3 PCLKB	2 ICLK
0008 C466h	RTC	Hour Capture Register 1	RHRCP1	8	8	2 or 3 PCLKB	2 ICLK
0008 C466h	RTC	BCNT2 Capture Register 1	BCNT2CP1	8	8	2 or 3 PCLKB	2 ICLK
0008 C46Ah	RTC	Date Capture Register 1	RDAYCP1	8	8	2 or 3 PCLKB	2 ICLK
0008 C46Ah	RTC	BCNT3 Capture Register 1	BCNT3CP1	8	8	2 or 3 PCLKB	2 ICLK
0008 C46Ch	RTC	Month Capture Register 1	RMONCP1	8	8	2 or 3 PCLKB	2 ICLK
0008 C472h	RTC	Second Capture Register 2	RSECCP2	8	8	2 or 3 PCLKB	2 ICLK
0008 C472h	RTC	BCNT0 Capture Register 2	BCNT0CP2	8	8	2 or 3 PCLKB	2 ICLK
0008 C474h	RTC	Minute Capture Register 2	RMINCP2	8	8	2 or 3 PCLKB	2 ICLK
0008 C474h	RTC	BCNT1 Capture Register 2	BCNT1CP2	8	8	2 or 3 PCLKB	2 ICLK
0008 C476h	RTC	Hour Capture Register 2	RHRCP2	8	8	2 or 3 PCLKB	2 ICLK
0008 C476h	RTC	BCNT2 Capture Register 2	BCNT2CP2	8	8	2 or 3 PCLKB	2 ICLK
0008 C47Ah	RTC	Date Capture Register 2	RDAYCP2	8	8	2 or 3 PCLKB	2 ICLK
0008 C47Ah	RTC	BCNT3 Capture Register 2	BCNT3CP2	8	8	2 or 3 PCLKB	2 ICLK
0008 C47Ch	RTC	Month Capture Register 2	RMONCP2	8	8	2 or 3 PCLKB	2 ICLK
0008 C580h	CMPB	Comparator B Control Register 1	CPBCNT1	8	8	2 or 3 PCLKB	2 ICLK
0008 C581h	CMPB	Comparator B Control Register 2	CPBCNT2	8	8	2 or 3 PCLKB	2 ICLK
0008 C582h	CMPB	Comparator B Flag Register	CPBFLG	8	8	2 or 3 PCLKB	2 ICLK
0008 C583h	CMPB	Comparator B Interrupt Control Register	CPBINT	8	8	2 or 3 PCLKB	2 ICLK
0008 C584h	CMPB	Comparator B Filter Select Register	CPBF	8	8	2 or 3 PCLKB	2 ICLK
0008 C585h	CMPB	Comparator B Mode Select Register	CPBMD	8	8	2 or 3 PCLKB	2 ICLK

Table 4.1 List of I/O Registers (Address Order) (29 / 42)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles	
						ICLK ≥ PCLK	ICLK < PCLK
0008 C586h	CMPB	Comparator B Reference Input Voltage Select Register	CPBREF	8	8	2 or 3 PCLKB	2 ICLK
0008 C587h	CMPB	Comparator B Output Control Register	CPBOCR	8	8	2 or 3 PCLKB	2 ICLK
0008 C5A0h	CMPB	Comparator B1 Control Register 1	CPB1CNT1	8	8	2 or 3 PCLKB	2 ICLK
0008 C5A1h	CMPB	Comparator B1 Control Register 2	CPB1CNT2	8	8	2 or 3 PCLKB	2 ICLK
0008 C5A2h	CMPB	Comparator B1 Flag Register	CPB1FLG	8	8	2 or 3 PCLKB	2 ICLK
0008 C5A3h	CMPB	Comparator B1 Interrupt Control Register	CPB1INT	8	8	2 or 3 PCLKB	2 ICLK
0008 C5A4h	CMPB	Comparator B1 Filter Select Register	CPB1F	8	8	2 or 3 PCLKB	2 ICLK
0008 C5A5h	CMPB	Comparator B1 Mode Select Register	CPB1MD	8	8	2 or 3 PCLKB	2 ICLK
0008 C5A6h	CMPB	Comparator B1 Reference Input Voltage Select Register	CPB1REF	8	8	2 or 3 PCLKB	2 ICLK
0008 C5A7h	CMPB	Comparator B1 Output Control Register	CPB1OCR	8	8	2 or 3 PCLKB	2 ICLK
000A 0000h	USB0	System Configuration Control Register	SYSCFG	16	16	3, 4 PCLKB	2 ICLK
000A 0004h	USB0	System Configuration Status Register 0	SYSSTS0	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than $1 + 9 \times (\text{frequency ratio of ICLK/PCLKB})^2$
000A 0008h	USB0	Device State Control Register 0	DVSTCTR0	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than $1 + 9 \times (\text{frequency ratio of ICLK/PCLKB})^2$
000A 0014h	USB0	CFIFO Port Register	CFIFO	16	16	3, 4 PCLKB	2 ICLK
000A 0018h	USB0	D0FIFO Port Register	D0FIFO	16	16	3, 4 PCLKB	2 ICLK
000A 001Ch	USB0	D1FIFO Port Register	D1FIFO	16	16	3, 4 PCLKB	2 ICLK
000A 0020h	USB0	CFIFO Port Select Register	CFIFOSEL	16	16	3, 4 PCLKB	2 ICLK
000A 0022h	USB0	CFIFO Port Control Register	CFIFOCTR	16	16	3, 4 PCLKB	2 ICLK
000A 0028h	USB0	D0FIFO Port Select Register	D0FIFOSEL	16	16	3, 4 PCLKB	2 ICLK
000A 002Ah	USB0	D0FIFO Port Control Register	D0FIFOCTR	16	16	3, 4 PCLKB	2 ICLK
000A 002Ch	USB0	D1FIFO Port Select Register	D1FIFOSEL	16	16	3, 4 PCLKB	2 ICLK
000A 002Eh	USB0	D1FIFO Port Control Register	D1FIFOCTR	16	16	3, 4 PCLKB	2 ICLK
000A 0030h	USB0	Interrupt Enable Register 0	INTENB0	16	16	9 PCLKB or more	Frequency with $1 + 9 \times (\text{frequency ratio of ICLK/PCLKB})^2$
000A 0032h	USB0	Interrupt Enable Register 1	INTENB1	16	16	9 PCLKB or more	Frequency with $1 + 9 \times (\text{frequency ratio of ICLK/PCLKB})^2$
000A 0036h	USB0	BRDY Interrupt Enable Register	BRDYENB	16	16	9 PCLKB or more	Frequency with $1 + 9 \times (\text{frequency ratio of ICLK/PCLKB})^2$
000A 0038h	USB0	NRDY Interrupt Enable Register	NRDYENB	16	16	9 PCLKB or more	Frequency with $1 + 9 \times (\text{frequency ratio of ICLK/PCLKB})^2$
000A 003Ah	USB0	BEMP Interrupt Enable Register	BEMPENB	16	16	9 PCLKB or more	Frequency with $1 + 9 \times (\text{frequency ratio of ICLK/PCLKB})^2$
000A 003Ch	USB0	SOF Output Configuration Register	SOFCFG	16	16	9 PCLKB or more	Frequency with $1 + 9 \times (\text{frequency ratio of ICLK/PCLKB})^2$
000A 0040h	USB0	Interrupt Status Register 0	INTSTS0	16	16	9 PCLKB or more	Frequency with $1 + 9 \times (\text{frequency ratio of ICLK/PCLKB})^2$
000A 0042h	USB0	Interrupt Status Register 1	INTSTS1	16	16	9 PCLKB or more	Frequency with $1 + 9 \times (\text{frequency ratio of ICLK/PCLKB})^2$
000A 0046h	USB0	BRDY Interrupt Status Register	BRDYSTS	16	16	9 PCLKB or more	Frequency with $1 + 9 \times (\text{frequency ratio of ICLK/PCLKB})^2$
000A 0048h	USB0	NRDY Interrupt Status Register	NRDYSTS	16	16	9 PCLKB or more	Frequency with $1 + 9 \times (\text{frequency ratio of ICLK/PCLKB})^2$
000A 004Ah	USB0	BEMP Interrupt Status Register	BEMPSTS	16	16	9 PCLKB or more	Frequency with $1 + 9 \times (\text{frequency ratio of ICLK/PCLKB})^2$
000A 004Ch	USB0	Frame Number Register	FRMNUM	16	16	9 PCLKB or more	Frequency with $1 + 9 \times (\text{frequency ratio of ICLK/PCLKB})^2$

Table 4.1 List of I/O Registers (Address Order) (30 / 42)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles	
						ICLK ≥ PCLK	ICLK < PCLK
000A 0054h	USB0	USB Request Type Register	USBREQ	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB) ^{*2}
000A 0056h	USB0	USB Request Value Register	USBVAL	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB) ^{*2}
000A 0058h	USB0	USB Request Index Register	USBINDX	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB) ^{*2}
000A 005Ah	USB0	USB Request Length Register	USBLENG	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB) ^{*2}
000A 005Ch	USB0	DCP Configuration Register	DCPCFG	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB) ^{*2}
000A 005Eh	USB0	DCP Maximum Packet Size Register	DCPMAXP	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB) ^{*2}
000A 0060h	USB0	DCP Control Register	DCPCTR	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB) ^{*2}
000A 0064h	USB0	Pipe Window Select Register	PIPESEL	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB) ^{*2}
000A 0068h	USB0	Pipe Configuration Register	PIPECFG	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB) ^{*2}
000A 006Ch	USB0	Pipe Maximum Packet Size Register	PIPEMAXP	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB) ^{*2}
000A 006Eh	USB0	Pipe Cycle Control Register	PIPEPERI	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB) ^{*2}
000A 0070h	USB0	PIPE1 Control Register	PIPE1CTR	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB) ^{*2}
000A 0072h	USB0	PIPE2 Control Register	PIPE2CTR	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB) ^{*2}
000A 0074h	USB0	PIPE3 Control Register	PIPE3CTR	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB) ^{*2}
000A 0076h	USB0	PIPE4 Control Register	PIPE4CTR	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB) ^{*2}
000A 0078h	USB0	PIPE5 Control Register	PIPE5CTR	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB) ^{*2}
000A 007Ah	USB0	PIPE6 Control Register	PIPE6CTR	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB) ^{*2}
000A 007Ch	USB0	PIPE7 Control Register	PIPE7CTR	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB) ^{*2}
000A 007Eh	USB0	PIPE8 Control Register	PIPE8CTR	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB) ^{*2}
000A 0080h	USB0	PIPE9 Control Register	PIPE9CTR	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB) ^{*2}
000A 0090h	USB0	PIPE1 Transaction Counter Enable Register	PIPE1TRE	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB) ^{*2}
000A 0092h	USB0	PIPE1 Transaction Counter Register	PIPE1TRN	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB) ^{*2}
000A 0094h	USB0	PIPE2 Transaction Counter Enable Register	PIPE2TRE	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB) ^{*2}
000A 0096h	USB0	PIPE2 Transaction Counter Register	PIPE2TRN	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB) ^{*2}

Table 4.1 List of I/O Registers (Address Order) (31 / 42)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles	
						ICLK ≥ PCLK	ICLK < PCLK
000A 0098h	USB0	PIPE3 Transaction Counter Enable Register	PIPE3TRE	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB) ^{*2}
000A 009Ah	USB0	PIPE3 Transaction Counter Register	PIPE3TRN	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB) ^{*2}
000A 009Ch	USB0	PIPE4 Transaction Counter Enable Register	PIPE4TRE	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB) ^{*2}
000A 009Eh	USB0	PIPE4 Transaction Counter Register	PIPE4TRN	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB) ^{*2}
000A 00A0h	USB0	PIPE5 Transaction Counter Enable Register	PIPE5TRE	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB) ^{*2}
000A 00A2h	USB0	PIPE5 Transaction Counter Register	PIPE5TRN	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB) ^{*2}
000A 00B0h	USB0	BC Control Register 0	USBBCCTRL0	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB) ^{*2}
000A 00CCh	USB0	USB Module Control Register	USBMC	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB) ^{*2}
000A 00D0h	USB0	Device Address 0 Configuration Register	DEVADD0	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB) ^{*2}
000A 00D2h	USB0	Device Address 1 Configuration Register	DEVADD1	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB) ^{*2}
000A 00D4h	USB0	Device Address 2 Configuration Register	DEVADD2	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB) ^{*2}
000A 00D6h	USB0	Device Address 3 Configuration Register	DEVADD3	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB) ^{*2}
000A 00D8h	USB0	Device Address 4 Configuration Register	DEVADD4	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB) ^{*2}
000A 00DAh	USB0	Device Address 5 Configuration Register	DEVADD5	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB) ^{*2}
000A 0900h	CTSU	CTSU Control Register 0	CTSUCR0	8	8	2 or 3 PCLKB	2 ICLK
000A 0901h	CTSU	CTSU Control Register 1	CTSUCR1	8	8	2 or 3 PCLKB	2 ICLK
000A 0902h	CTSU	CTSU Synchronous Noise Reduction Setting Register	CTSUSDPRS	8	8	2 or 3 PCLKB	2 ICLK
000A 0903h	CTSU	CTSU Sensor Stabilization Wait Control Register	CTSUSST	8	8	2 or 3 PCLKB	2 ICLK
000A 0904h	CTSU	CTSU Measurement Channel Register 0	CTSUSMCH0	8	8	2 or 3 PCLKB	2 ICLK
000A 0905h	CTSU	CTSU Measurement Channel Register 1	CTSUSMCH1	8	8	2 or 3 PCLKB	2 ICLK
000A 0906h	CTSU	CTSU Channel Enable Control Register 0	CTSUSCHAC0	8	8	2 or 3 PCLKB	2 ICLK
000A 0907h	CTSU	CTSU Channel Enable Control Register 1	CTSUSCHAC1	8	8	2 or 3 PCLKB	2 ICLK
000A 0908h	CTSU	CTSU Channel Enable Control Register 2	CTSUSCHAC2	8	8	2 or 3 PCLKB	2 ICLK
000A 0909h	CTSU	CTSU Channel Enable Control Register 3	CTSUSCHAC3	8	8	2 or 3 PCLKB	2 ICLK
000A 090Ah	CTSU	CTSU Channel Enable Control Register 4	CTSUSCHAC4	8	8	2 or 3 PCLKB	2 ICLK
000A 090Bh	CTSU	CTSU Channel Transmit/Receive Control Register 0	CTSUSCHTRC0	8	8	2 or 3 PCLKB	2 ICLK
000A 090Ch	CTSU	CTSU Channel Transmit/Receive Control Register 1	CTSUSCHTRC1	8	8	2 or 3 PCLKB	2 ICLK
000A 090Dh	CTSU	CTSU Channel Transmit/Receive Control Register 2	CTSUSCHTRC2	8	8	2 or 3 PCLKB	2 ICLK
000A 090Eh	CTSU	CTSU Channel Transmit/Receive Control Register 3	CTSUSCHTRC3	8	8	2 or 3 PCLKB	2 ICLK
000A 090Fh	CTSU	CTSU Channel Transmit/Receive Control Register 4	CTSUSCHTRC4	8	8	2 or 3 PCLKB	2 ICLK
000A 0910h	CTSU	CTSU High-Pass Noise Reduction Control Register	CTSUSUDCLKC	8	8	2 or 3 PCLKB	2 ICLK
000A 0911h	CTSU	CTSU Status Register	CTSUSUST	8	8	2 or 3 PCLKB	2 ICLK
000A 0912h	CTSU	CTSU High-Pass Noise Reduction Spectrum Diffusion Control Register	CTSUSUSSC	16	16	2 or 3 PCLKB	2 ICLK
000A 0914h	CTSU	CTSU Sensor Offset Register 0	CTSUSUSO0	16	16	2 or 3 PCLKB	2 ICLK
000A 0916h	CTSU	CTSU Sensor Offset Register 1	CTSUSUSO1	16	16	2 or 3 PCLKB	2 ICLK
000A 0918h	CTSU	CTSU Sensor Counter	CTSUSUSC	16	16	2 or 3 PCLKB	2 ICLK

Table 4.1 List of I/O Registers (Address Order) (32 / 42)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles	
						ICLK ≥ PCLK	ICLK < PCLK
000A 091Ah	CTSU	CTSU Reference Counter	CTSURC	16	16	2 or 3 PCLKB	2 ICLK
000A 091Ch	CTSU	CTSU Error Status Register	CTSUERRS	16	16	2 or 3 PCLKB	2 ICLK
000A 8300h	CAN0	Bit Configuration Register L	CFGL	16	16	2 or 3 PCLKB	2 ICLK
000A 8302h	CAN0	Bit Configuration Register H	CFGH	16	16	2 or 3 PCLKB	2 ICLK
000A 8304h	CAN0	Control Register L	CTRL	16	16	2 or 3 PCLKB	2 ICLK
000A 8306h	CAN0	Control Register H	CTRH	16	16	2 or 3 PCLKB	2 ICLK
000A 8308h	CAN0	Status Register L	STSL	16	16	2 or 3 PCLKB	2 ICLK
000A 830Ah	CAN0	Status Register H	STSH	16	16	2 or 3 PCLKB	2 ICLK
000A 830Ch	CAN0	Error Flag Register L	ERFLL	16	16	2 or 3 PCLKB	2 ICLK
000A 830Eh	CAN0	Error Flag Register H	ERFLH	16	16	2 or 3 PCLKB	2 ICLK
000A 8322h	CAN	Global Configuration Register L	GCFGL	16	16	2 or 3 PCLKB	2 ICLK
000A 8324h	CAN	Global Configuration Register H	GCFGH	16	16	2 or 3 PCLKB	2 ICLK
000A 8326h	CAN	Global Control Register L	GCTRL	16	16	2 or 3 PCLKB	2 ICLK
000A 8328h	CAN	Global Control Register H	GCTRH	16	16	2 or 3 PCLKB	2 ICLK
000A 832Ah	CAN	Global Status Register	GSTS	16	16	2 or 3 PCLKB	2 ICLK
000A 832Ch	CAN	Global Error Flag Register	GERFLL	8	8	2 or 3 PCLKB	2 ICLK
000A 832Eh	CAN	Timestamp Register	GTSC	16	16	2 or 3 PCLKB	2 ICLK
000A 8330h	CAN	Receive Rule Number Configuration Register	GAFLCFG	16	16	2 or 3 PCLKB	2 ICLK
000A 8332h	CAN	Receive Buffer Number Configuration Register	RMNB	16	16	2 or 3 PCLKB	2 ICLK
000A 8334h	CAN	Receive Buffer Receive Complete Flag Register	RMND0	16	16	2 or 3 PCLKB	2 ICLK
000A 8338h	CAN	Receive FIFO Control Register 0	RFCC0	16	16	2 or 3 PCLKB	2 ICLK
000A 833Ah	CAN	Receive FIFO Control Register 1	RFCC1	16	16	2 or 3 PCLKB	2 ICLK
000A 8340h	CAN	Receive FIFO Status Register 0	RFSTS0	16	16	2 or 3 PCLKB	2 ICLK
000A 8342h	CAN	Receive FIFO Status Register 1	RFSTS1	16	16	2 or 3 PCLKB	2 ICLK
000A 8348h	CAN	Receive FIFO Pointer Control Register 0	RFPCTR0	16	16	2 or 3 PCLKB	2 ICLK
000A 834Ah	CAN	Receive FIFO Pointer Control Register 1	RFPCTR1	16	16	2 or 3 PCLKB	2 ICLK
000A 8350h	CAN0	Transmit/Receive FIFO Control Register 0L	CFCC0L	16	16	2 or 3 PCLKB	2 ICLK
000A 8352h	CAN0	Transmit/Receive FIFO Control Register 0H	CFCC0H	16	16	2 or 3 PCLKB	2 ICLK
000A 8358h	CAN0	Transmit/Receive FIFO Status Register 0	CFSTS0	16	16	2 or 3 PCLKB	2 ICLK
000A 835Ch	CAN0	Transmit/Receive FIFO Pointer Control Register 0	CFPCTR0	16	16	2 or 3 PCLKB	2 ICLK
000A 8360h	CAN	Receive FIFO Message Lost Status Register	RFMSTS	8	8	2 or 3 PCLKB	2 ICLK
000A 8361h	CAN0	Transmit/Receive FIFO Message Lost Status Register	CFMSTS	8	8	2 or 3 PCLKB	2 ICLK
000A 8362h	CAN	Receive FIFO Interrupt Status Register	RFISTS	8	8	2 or 3 PCLKB	2 ICLK
000A 8363h	CAN	Transmit/Receive FIFO Receive Interrupt Status Register	CFISTS	8	8	2 or 3 PCLKB	2 ICLK
000A 8364h	CAN0	Transmit Buffer Control Register 0	TMC0	8	8	2 or 3 PCLKB	2 ICLK
000A 8365h	CAN0	Transmit Buffer Control Register 1	TMC1	8	8	2 or 3 PCLKB	2 ICLK
000A 8366h	CAN0	Transmit Buffer Control Register 2	TMC2	8	8	2 or 3 PCLKB	2 ICLK
000A 8367h	CAN0	Transmit Buffer Control Register 3	TMC3	8	8	2 or 3 PCLKB	2 ICLK
000A 836Ch	CAN0	Transmit Buffer Status Register 0	TMSTS0	8	8	2 or 3 PCLKB	2 ICLK
000A 836Dh	CAN0	Transmit Buffer Status Register 1	TMSTS1	8	8	2 or 3 PCLKB	2 ICLK
000A 836Eh	CAN0	Transmit Buffer Status Register 2	TMSTS2	8	8	2 or 3 PCLKB	2 ICLK
000A 836Fh	CAN0	Transmit Buffer Status Register 3	TMSTS3	8	8	2 or 3 PCLKB	2 ICLK
000A 8374h	CAN0	Transmit Buffer Transmit Request Status Register	TMTRSTS	16	16	2 or 3 PCLKB	2 ICLK
000A 8376h	CAN0	Transmit Buffer Transmit Complete Status Register	TMTCSSTS	16	16	2 or 3 PCLKB	2 ICLK
000A 8378h	CAN0	Transmit Buffer Transmit Abort Status Register	TMTASTS	16	16	2 or 3 PCLKB	2 ICLK
000A 837Ah	CAN0	Transmit Buffer Interrupt Enable Register	TMIEC	16	16	2 or 3 PCLKB	2 ICLK
000A 837Ch	CAN0	Transmit History Buffer Control Register	THLCC0	16	16	2 or 3 PCLKB	2 ICLK
000A 8380h	CAN0	Transmit History Buffer Status Register	THLSTS0	16	16	2 or 3 PCLKB	2 ICLK
000A 8384h	CAN0	Transmit History Buffer Pointer Control Register	THLPCTR0	16	16	2 or 3 PCLKB	2 ICLK
000A 8388h	CAN	Global Transmit Interrupt Status Register	GTINTSTS	16	16	2 or 3 PCLKB	2 ICLK
000A 838Ah	CAN	Global RAM Window Control Register	GRWCR	16	16	2 or 3 PCLKB	2 ICLK
000A 838Ch	CAN	Global Test Configuration Register	GTSTCFG	16	16	2 or 3 PCLKB	2 ICLK

Table 4.1 List of I/O Registers (Address Order) (33 / 42)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles	
						ICLK ≥ PCLK	ICLK < PCLK
000A 838Eh	CAN	Global Test Control Register	GTSTCTRL	16	16	2 or 3 PCLKB	2 ICLK
000A 8394h	CAN	Global Test Protection Unlock Register	GLOCKK	16	16	2 or 3 PCLKB	2 ICLK
000A 83A0h	CAN	Receive Rule Entry Register 0AL	GAFLIDL0	16	16	2 or 3 PCLKB	2 ICLK
000A 83A0h	CAN	Receive Buffer Register 0AL	RMIDL0	16	16	2 or 3 PCLKB	2 ICLK
000A 83A2h	CAN	Receive Rule Entry Register 0AH	GAFLIDH0	16	16	2 or 3 PCLKB	2 ICLK
000A 83A2h	CAN	Receive Buffer Register 0AH	RMIDH0	16	16	2 or 3 PCLKB	2 ICLK
000A 83A4h	CAN	Receive Rule Entry Register 0BL	GAFLML0	16	16	2 or 3 PCLKB	2 ICLK
000A 83A4h	CAN	Receive Buffer Register 0BL	RMTS0	16	16	2 or 3 PCLKB	2 ICLK
000A 83A6h	CAN	Receive Rule Entry Register 0BH	GAFLMH0	16	16	2 or 3 PCLKB	2 ICLK
000A 83A6h	CAN	Receive Buffer Register 0BH	RMPTR0	16	16	2 or 3 PCLKB	2 ICLK
000A 83A8h	CAN	Receive Rule Entry Register 0CL	GAFLPL0	16	16	2 or 3 PCLKB	2 ICLK
000A 83A8h	CAN	Receive Buffer Register 0CL	RMDF00	16	16	2 or 3 PCLKB	2 ICLK
000A 83AAh	CAN	Receive Rule Entry Register 0CH	GAFLPH0	16	16	2 or 3 PCLKB	2 ICLK
000A 83AAh	CAN	Receive Buffer Register 0CH	RMDF10	16	16	2 or 3 PCLKB	2 ICLK
000A 83ACh	CAN	Receive Rule Entry Register 1AL	GAFLIDL1	16	16	2 or 3 PCLKB	2 ICLK
000A 83ACh	CAN	Receive Buffer Register 0DL	RMDF20	16	16	2 or 3 PCLKB	2 ICLK
000A 83AEh	CAN	Receive Rule Entry Register 1AH	GAFLIDH1	16	16	2 or 3 PCLKB	2 ICLK
000A 83AEh	CAN	Receive Buffer Register 0DH	RMDF30	16	16	2 or 3 PCLKB	2 ICLK
000A 83B0h	CAN	Receive Rule Entry Register 1BL	GAFLML1	16	16	2 or 3 PCLKB	2 ICLK
000A 83B0h	CAN	Receive Buffer Register 1AL	RMIDL1	16	16	2 or 3 PCLKB	2 ICLK
000A 83B2h	CAN	Receive Rule Entry Register 1BH	GAFLMH1	16	16	2 or 3 PCLKB	2 ICLK
000A 83B2h	CAN	Receive Buffer Register 1AH	RMIDH1	16	16	2 or 3 PCLKB	2 ICLK
000A 83B4h	CAN	Receive Rule Entry Register 1CL	GAFLPL1	16	16	2 or 3 PCLKB	2 ICLK
000A 83B4h	CAN	Receive Buffer Register 1BL	RMTS1	16	16	2 or 3 PCLKB	2 ICLK
000A 83B6h	CAN	Receive Rule Entry Register 1CH	GAFLPH1	16	16	2 or 3 PCLKB	2 ICLK
000A 83B6h	CAN	Receive Buffer Register 1BH	RMPTR1	16	16	2 or 3 PCLKB	2 ICLK
000A 83B8h	CAN	Receive Rule Entry Register 2AL	GAFLIDL2	16	16	2 or 3 PCLKB	2 ICLK
000A 83B8h	CAN	Receive Buffer Register 1CL	RMDF01	16	16	2 or 3 PCLKB	2 ICLK
000A 83BAh	CAN	Receive Rule Entry Register 2AH	GAFLIDH2	16	16	2 or 3 PCLKB	2 ICLK
000A 83BAh	CAN	Receive Buffer Register 1CH	RMDF11	16	16	2 or 3 PCLKB	2 ICLK
000A 83BCh	CAN	Receive Rule Entry Register 2BL	GAFLML2	16	16	2 or 3 PCLKB	2 ICLK
000A 83BCh	CAN	Receive Buffer Register 1DL	RMDF21	16	16	2 or 3 PCLKB	2 ICLK
000A 83BEh	CAN	Receive Rule Entry Register 2BH	GAFLMH2	16	16	2 or 3 PCLKB	2 ICLK
000A 83BEh	CAN	Receive Buffer Register 1DH	RMDF31	16	16	2 or 3 PCLKB	2 ICLK
000A 83C0h	CAN	Receive Rule Entry Register 2CL	GAFLPL2	16	16	2 or 3 PCLKB	2 ICLK
000A 83C0h	CAN	Receive Buffer Register 2AL	RMIDL2	16	16	2 or 3 PCLKB	2 ICLK
000A 83C2h	CAN	Receive Rule Entry Register 2CH	GAFLPH2	16	16	2 or 3 PCLKB	2 ICLK
000A 83C2h	CAN	Receive Buffer Register 2AH	RMIDH2	16	16	2 or 3 PCLKB	2 ICLK
000A 83C4h	CAN	Receive Rule Entry Register 3AL	GAFLIDL3	16	16	2 or 3 PCLKB	2 ICLK
000A 83C4h	CAN	Receive Buffer Register 2BL	RMTS2	16	16	2 or 3 PCLKB	2 ICLK
000A 83C6h	CAN	Receive Rule Entry Register 3AH	GAFLIDH3	16	16	2 or 3 PCLKB	2 ICLK
000A 83C6h	CAN	Receive Buffer Register 2BH	RMPTR2	16	16	2 or 3 PCLKB	2 ICLK
000A 83C8h	CAN	Receive Rule Entry Register 3BL	GAFLML3	16	16	2 or 3 PCLKB	2 ICLK
000A 83C8h	CAN	Receive Buffer Register 2CL	RMDF02	16	16	2 or 3 PCLKB	2 ICLK
000A 83CAh	CAN	Receive Rule Entry Register 3BH	GAFLMH3	16	16	2 or 3 PCLKB	2 ICLK
000A 83CAh	CAN	Receive Buffer Register 2CH	RMDF12	16	16	2 or 3 PCLKB	2 ICLK
000A 83CCh	CAN	Receive Rule Entry Register 3CL	GAFLPL3	16	16	2 or 3 PCLKB	2 ICLK
000A 83CCh	CAN	Receive Buffer Register 2DL	RMDF22	16	16	2 or 3 PCLKB	2 ICLK
000A 83CEh	CAN	Receive Rule Entry Register 3CH	GAFLPH3	16	16	2 or 3 PCLKB	2 ICLK
000A 83CEh	CAN	Receive Buffer Register 2DH	RMDF32	16	16	2 or 3 PCLKB	2 ICLK
000A 83D0h	CAN	Receive Rule Entry Register 4AL	GAFLIDL4	16	16	2 or 3 PCLKB	2 ICLK
000A 83D0h	CAN	Receive Buffer Register 3AL	RMIDL3	16	16	2 or 3 PCLKB	2 ICLK

Table 4.1 List of I/O Registers (Address Order) (34 / 42)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles	
						ICLK ≥ PCLK	ICLK < PCLK
000A 83D2h	CAN	Receive Rule Entry Register 4AH	GAFLIDH4	16	16	2 or 3 PCLKB	2 ICLK
000A 83D2h	CAN	Receive Buffer Register 3AH	RMIDH3	16	16	2 or 3 PCLKB	2 ICLK
000A 83D4h	CAN	Receive Rule Entry Register 4BL	GAFLML4	16	16	2 or 3 PCLKB	2 ICLK
000A 83D4h	CAN	Receive Buffer Register 3BL	RMTS3	16	16	2 or 3 PCLKB	2 ICLK
000A 83D6h	CAN	Receive Rule Entry Register 4BH	GAFLMH4	16	16	2 or 3 PCLKB	2 ICLK
000A 83D6h	CAN	Receive Buffer Register 3BH	RMPTR3	16	16	2 or 3 PCLKB	2 ICLK
000A 83D8h	CAN	Receive Rule Entry Register 4CL	GAFLPL4	16	16	2 or 3 PCLKB	2 ICLK
000A 83D8h	CAN	Receive Buffer Register 3CL	RMDFO3	16	16	2 or 3 PCLKB	2 ICLK
000A 83DAh	CAN	Receive Rule Entry Register 4CH	GAFLPH4	16	16	2 or 3 PCLKB	2 ICLK
000A 83DAh	CAN	Receive Buffer Register 3CH	RMDF13	16	16	2 or 3 PCLKB	2 ICLK
000A 83DCh	CAN	Receive Rule Entry Register 5AL	GAFLIDL5	16	16	2 or 3 PCLKB	2 ICLK
000A 83DCh	CAN	Receive Buffer Register 3DL	RMDF23	16	16	2 or 3 PCLKB	2 ICLK
000A 83DEh	CAN	Receive Rule Entry Register 5AH	GAFLIDH5	16	16	2 or 3 PCLKB	2 ICLK
000A 83DEh	CAN	Receive Buffer Register 3DH	RMDF33	16	16	2 or 3 PCLKB	2 ICLK
000A 83E0h	CAN	Receive Rule Entry Register 5BL	GAFLML5	16	16	2 or 3 PCLKB	2 ICLK
000A 83E0h	CAN	Receive Buffer Register 4AL	RMIDL4	16	16	2 or 3 PCLKB	2 ICLK
000A 83E2h	CAN	Receive Rule Entry Register 5BH	GAFLMH5	16	16	2 or 3 PCLKB	2 ICLK
000A 83E2h	CAN	Receive Buffer Register 4AH	RMIDH4	16	16	2 or 3 PCLKB	2 ICLK
000A 83E4h	CAN	Receive Rule Entry Register 5CL	GAFLPL5	16	16	2 or 3 PCLKB	2 ICLK
000A 83E4h	CAN	Receive Buffer Register 4BL	RMTS4	16	16	2 or 3 PCLKB	2 ICLK
000A 83E6h	CAN	Receive Rule Entry Register 5CH	GAFLPH5	16	16	2 or 3 PCLKB	2 ICLK
000A 83E6h	CAN	Receive Buffer Register 4BH	RMPTR4	16	16	2 or 3 PCLKB	2 ICLK
000A 83E8h	CAN	Receive Rule Entry Register 6AL	GAFLIDL6	16	16	2 or 3 PCLKB	2 ICLK
000A 83E8h	CAN	Receive Buffer Register 4CL	RMDFO4	16	16	2 or 3 PCLKB	2 ICLK
000A 83EAh	CAN	Receive Rule Entry Register 6AH	GAFLIDH6	16	16	2 or 3 PCLKB	2 ICLK
000A 83EAh	CAN	Receive Buffer Register 4CH	RMDF14	16	16	2 or 3 PCLKB	2 ICLK
000A 83ECh	CAN	Receive Rule Entry Register 6BL	GAFLML6	16	16	2 or 3 PCLKB	2 ICLK
000A 83ECh	CAN	Receive Buffer Register 4DL	RMDF24	16	16	2 or 3 PCLKB	2 ICLK
000A 83EEh	CAN	Receive Rule Entry Register 6BH	GAFLMH6	16	16	2 or 3 PCLKB	2 ICLK
000A 83EEh	CAN	Receive Buffer Register 4DH	RMDF34	16	16	2 or 3 PCLKB	2 ICLK
000A 83F0h	CAN	Receive Rule Entry Register 6CL	GAFLPL6	16	16	2 or 3 PCLKB	2 ICLK
000A 83F0h	CAN	Receive Buffer Register 5AL	RMIDL5	16	16	2 or 3 PCLKB	2 ICLK
000A 83F2h	CAN	Receive Rule Entry Register 6CH	GAFLPH6	16	16	2 or 3 PCLKB	2 ICLK
000A 83F2h	CAN	Receive Buffer Register 5AH	RMIDH5	16	16	2 or 3 PCLKB	2 ICLK
000A 83F4h	CAN	Receive Rule Entry Register 7AL	GAFLIDL7	16	16	2 or 3 PCLKB	2 ICLK
000A 83F4h	CAN	Receive Buffer Register 5BL	RMTS5	16	16	2 or 3 PCLKB	2 ICLK
000A 83F6h	CAN	Receive Rule Entry Register 7AH	GAFLIDH7	16	16	2 or 3 PCLKB	2 ICLK
000A 83F6h	CAN	Receive Buffer Register 5BH	RMPTR5	16	16	2 or 3 PCLKB	2 ICLK
000A 83F8h	CAN	Receive Rule Entry Register 7BL	GAFLML7	16	16	2 or 3 PCLKB	2 ICLK
000A 83F8h	CAN	Receive Buffer Register 5CL	RMDFO5	16	16	2 or 3 PCLKB	2 ICLK
000A 83FAh	CAN	Receive Rule Entry Register 7BH	GAFLMH7	16	16	2 or 3 PCLKB	2 ICLK
000A 83FAh	CAN	Receive Buffer Register 5CH	RMDF15	16	16	2 or 3 PCLKB	2 ICLK
000A 83FCh	CAN	Receive Rule Entry Register 7CL	GAFLPL7	16	16	2 or 3 PCLKB	2 ICLK
000A 83FCh	CAN	Receive Buffer Register 5DL	RMDF25	16	16	2 or 3 PCLKB	2 ICLK
000A 83FEh	CAN	Receive Rule Entry Register 7CH	GAFLPH7	16	16	2 or 3 PCLKB	2 ICLK
000A 83FEh	CAN	Receive Buffer Register 5DH	RMDF35	16	16	2 or 3 PCLKB	2 ICLK
000A 8400h	CAN	Receive Rule Entry Register 8AL	GAFLIDL8	16	16	2 or 3 PCLKB	2 ICLK
000A 8400h	CAN	Receive Buffer Register 6AL	RMIDL6	16	16	2 or 3 PCLKB	2 ICLK
000A 8402h	CAN	Receive Rule Entry Register 8AH	GAFLIDH8	16	16	2 or 3 PCLKB	2 ICLK
000A 8402h	CAN	Receive Buffer Register 6AH	RMIDH6	16	16	2 or 3 PCLKB	2 ICLK
000A 8404h	CAN	Receive Rule Entry Register 8BL	GAFLML8	16	16	2 or 3 PCLKB	2 ICLK
000A 8404h	CAN	Receive Buffer Register 6BL	RMTS6	16	16	2 or 3 PCLKB	2 ICLK

Table 4.1 List of I/O Registers (Address Order) (35 / 42)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles	
						ICLK ≥ PCLK	ICLK < PCLK
000A 8406h	CAN	Receive Rule Entry Register 8BH	GAFLMH8	16	16	2 or 3 PCLKB	2 ICLK
000A 8406h	CAN	Receive Buffer Register 6BH	RMPTR6	16	16	2 or 3 PCLKB	2 ICLK
000A 8408h	CAN	Receive Rule Entry Register 8CL	GAFLPL8	16	16	2 or 3 PCLKB	2 ICLK
000A 8408h	CAN	Receive Buffer Register 6CL	RMDf06	16	16	2 or 3 PCLKB	2 ICLK
000A 840Ah	CAN	Receive Rule Entry Register 8CH	GAFLPH8	16	16	2 or 3 PCLKB	2 ICLK
000A 840Ah	CAN	Receive Buffer Register 6CH	RMDf16	16	16	2 or 3 PCLKB	2 ICLK
000A 840Ch	CAN	Receive Rule Entry Register 9AL	GAFLIDL9	16	16	2 or 3 PCLKB	2 ICLK
000A 840Ch	CAN	Receive Buffer Register 6DL	RMDf26	16	16	2 or 3 PCLKB	2 ICLK
000A 840Eh	CAN	Receive Rule Entry Register 9AH	GAFLIDH9	16	16	2 or 3 PCLKB	2 ICLK
000A 840Eh	CAN	Receive Buffer Register 6DH	RMDf36	16	16	2 or 3 PCLKB	2 ICLK
000A 8410h	CAN	Receive Rule Entry Register 9BL	GAFLML9	16	16	2 or 3 PCLKB	2 ICLK
000A 8410h	CAN	Receive Buffer Register 7AL	RMIDL7	16	16	2 or 3 PCLKB	2 ICLK
000A 8412h	CAN	Receive Rule Entry Register 9BH	GAFLMH9	16	16	2 or 3 PCLKB	2 ICLK
000A 8412h	CAN	Receive Buffer Register 7AH	RMIDH7	16	16	2 or 3 PCLKB	2 ICLK
000A 8414h	CAN	Receive Rule Entry Register 9CL	GAFLPL9	16	16	2 or 3 PCLKB	2 ICLK
000A 8414h	CAN	Receive Buffer Register 7BL	RMTS7	16	16	2 or 3 PCLKB	2 ICLK
000A 8416h	CAN	Receive Rule Entry Register 9CH	GAFLPH9	16	16	2 or 3 PCLKB	2 ICLK
000A 8416h	CAN	Receive Buffer Register 7BH	RMPTR7	16	16	2 or 3 PCLKB	2 ICLK
000A 8418h	CAN	Receive Rule Entry Register 10AL	GAFLIDL10	16	16	2 or 3 PCLKB	2 ICLK
000A 8418h	CAN	Receive Buffer Register 7CL	RMDf07	16	16	2 or 3 PCLKB	2 ICLK
000A 841Ah	CAN	Receive Rule Entry Register 10AH	GAFLIDH10	16	16	2 or 3 PCLKB	2 ICLK
000A 841Ah	CAN	Receive Buffer Register 7CH	RMDf17	16	16	2 or 3 PCLKB	2 ICLK
000A 841Ch	CAN	Receive Rule Entry Register 10BL	GAFLML10	16	16	2 or 3 PCLKB	2 ICLK
000A 841Ch	CAN	Receive Buffer Register 7DL	RMDf27	16	16	2 or 3 PCLKB	2 ICLK
000A 841Eh	CAN	Receive Rule Entry Register 10BH	GAFLMH10	16	16	2 or 3 PCLKB	2 ICLK
000A 841Eh	CAN	Receive Buffer Register 7DH	RMDf37	16	16	2 or 3 PCLKB	2 ICLK
000A 8420h	CAN	Receive Rule Entry Register 10CL	GAFLPL10	16	16	2 or 3 PCLKB	2 ICLK
000A 8420h	CAN	Receive Buffer Register 8AL	RMIDL8	16	16	2 or 3 PCLKB	2 ICLK
000A 8422h	CAN	Receive Rule Entry Register 10CH	GAFLPH10	16	16	2 or 3 PCLKB	2 ICLK
000A 8422h	CAN	Receive Buffer Register 8AH	RMIDH8	16	16	2 or 3 PCLKB	2 ICLK
000A 8424h	CAN	Receive Rule Entry Register 11AL	GAFLIDL11	16	16	2 or 3 PCLKB	2 ICLK
000A 8424h	CAN	Receive Buffer Register 8BL	RMTS8	16	16	2 or 3 PCLKB	2 ICLK
000A 8426h	CAN	Receive Rule Entry Register 11AH	GAFLIDH11	16	16	2 or 3 PCLKB	2 ICLK
000A 8426h	CAN	Receive Buffer Register 8BH	RMPTR8	16	16	2 or 3 PCLKB	2 ICLK
000A 8428h	CAN	Receive Rule Entry Register 11BL	GAFLML11	16	16	2 or 3 PCLKB	2 ICLK
000A 8428h	CAN	Receive Buffer Register 8CL	RMDf08	16	16	2 or 3 PCLKB	2 ICLK
000A 842Ah	CAN	Receive Rule Entry Register 11BH	GAFLMH11	16	16	2 or 3 PCLKB	2 ICLK
000A 842Ah	CAN	Receive Buffer Register 8CH	RMDf18	16	16	2 or 3 PCLKB	2 ICLK
000A 842Ch	CAN	Receive Rule Entry Register 11CL	GAFLPL11	16	16	2 or 3 PCLKB	2 ICLK
000A 842Ch	CAN	Receive Buffer Register 8DL	RMDf28	16	16	2 or 3 PCLKB	2 ICLK
000A 842Eh	CAN	Receive Rule Entry Register 11CH	GAFLPH11	16	16	2 or 3 PCLKB	2 ICLK
000A 842Eh	CAN	Receive Buffer Register 8DH	RMDf38	16	16	2 or 3 PCLKB	2 ICLK
000A 8430h	CAN	Receive Rule Entry Register 12AL	GAFLIDL12	16	16	2 or 3 PCLKB	2 ICLK
000A 8430h	CAN	Receive Buffer Register 9AL	RMIDL9	16	16	2 or 3 PCLKB	2 ICLK
000A 8432h	CAN	Receive Rule Entry Register 12AH	GAFLIDH12	16	16	2 or 3 PCLKB	2 ICLK
000A 8432h	CAN	Receive Buffer Register 9AH	RMIDH9	16	16	2 or 3 PCLKB	2 ICLK
000A 8434h	CAN	Receive Rule Entry Register 12BL	GAFLML12	16	16	2 or 3 PCLKB	2 ICLK
000A 8434h	CAN	Receive Buffer Register 9BL	RMTS9	16	16	2 or 3 PCLKB	2 ICLK
000A 8436h	CAN	Receive Rule Entry Register 12BH	GAFLMH12	16	16	2 or 3 PCLKB	2 ICLK
000A 8436h	CAN	Receive Buffer Register 9BH	RMPTR9	16	16	2 or 3 PCLKB	2 ICLK
000A 8438h	CAN	Receive Rule Entry Register 12CL	GAFLPL12	16	16	2 or 3 PCLKB	2 ICLK
000A 8438h	CAN	Receive Buffer Register 9CL	RMDf09	16	16	2 or 3 PCLKB	2 ICLK

Table 4.1 List of I/O Registers (Address Order) (36 / 42)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles	
						ICLK ≥ PCLK	ICLK < PCLK
000A 843Ah	CAN	Receive Rule Entry Register 12CH	GAFLPH12	16	16	2 or 3 PCLKB	2 ICLK
000A 843Ah	CAN	Receive Buffer Register 9CH	RMDF19	16	16	2 or 3 PCLKB	2 ICLK
000A 843Ch	CAN	Receive Rule Entry Register 13AL	GAFLIDL13	16	16	2 or 3 PCLKB	2 ICLK
000A 843Ch	CAN	Receive Buffer Register 9DL	RMDF29	16	16	2 or 3 PCLKB	2 ICLK
000A 843Eh	CAN	Receive Rule Entry Register 13AH	GAFLIDH13	16	16	2 or 3 PCLKB	2 ICLK
000A 843Eh	CAN	Receive Buffer Register 9DH	RMDF39	16	16	2 or 3 PCLKB	2 ICLK
000A 8440h	CAN	Receive Rule Entry Register 13BL	GAFLML13	16	16	2 or 3 PCLKB	2 ICLK
000A 8440h	CAN	Receive Buffer Register 10AL	RMIDL10	16	16	2 or 3 PCLKB	2 ICLK
000A 8442h	CAN	Receive Rule Entry Register 13BH	GAFLMH13	16	16	2 or 3 PCLKB	2 ICLK
000A 8442h	CAN	Receive Buffer Register 10AH	RMIDH10	16	16	2 or 3 PCLKB	2 ICLK
000A 8444h	CAN	Receive Rule Entry Register 13CL	GAFLPL13	16	16	2 or 3 PCLKB	2 ICLK
000A 8444h	CAN	Receive Buffer Register 10BL	RMTS10	16	16	2 or 3 PCLKB	2 ICLK
000A 8446h	CAN	Receive Rule Entry Register 13CH	GAFLPH13	16	16	2 or 3 PCLKB	2 ICLK
000A 8446h	CAN	Receive Buffer Register 10BH	RMPTR10	16	16	2 or 3 PCLKB	2 ICLK
000A 8448h	CAN	Receive Rule Entry Register 14AL	GAFLIDL14	16	16	2 or 3 PCLKB	2 ICLK
000A 8448h	CAN	Receive Buffer Register 10CL	RMDF010	16	16	2 or 3 PCLKB	2 ICLK
000A 844Ah	CAN	Receive Rule Entry Register 14AH	GAFLIDH14	16	16	2 or 3 PCLKB	2 ICLK
000A 844Ah	CAN	Receive Buffer Register 10CH	RMDF110	16	16	2 or 3 PCLKB	2 ICLK
000A 844Ch	CAN	Receive Rule Entry Register 14BL	GAFLML14	16	16	2 or 3 PCLKB	2 ICLK
000A 844Ch	CAN	Receive Buffer Register 10DL	RMDF210	16	16	2 or 3 PCLKB	2 ICLK
000A 844Eh	CAN	Receive Rule Entry Register 14BH	GAFLMH14	16	16	2 or 3 PCLKB	2 ICLK
000A 844Eh	CAN	Receive Buffer Register 10DH	RMDF310	16	16	2 or 3 PCLKB	2 ICLK
000A 8450h	CAN	Receive Rule Entry Register 14CL	GAFLPL14	16	16	2 or 3 PCLKB	2 ICLK
000A 8450h	CAN	Receive Buffer Register 11AL	RMIDL11	16	16	2 or 3 PCLKB	2 ICLK
000A 8452h	CAN	Receive Rule Entry Register 14CH	GAFLPH14	16	16	2 or 3 PCLKB	2 ICLK
000A 8452h	CAN	Receive Buffer Register 11AH	RMIDH11	16	16	2 or 3 PCLKB	2 ICLK
000A 8454h	CAN	Receive Rule Entry Register 15AL	GAFLIDL15	16	16	2 or 3 PCLKB	2 ICLK
000A 8454h	CAN	Receive Buffer Register 11BL	RMTS11	16	16	2 or 3 PCLKB	2 ICLK
000A 8456h	CAN	Receive Rule Entry Register 15AH	GAFLIDH15	16	16	2 or 3 PCLKB	2 ICLK
000A 8456h	CAN	Receive Buffer Register 11BH	RMPTR11	16	16	2 or 3 PCLKB	2 ICLK
000A 8458h	CAN	Receive Rule Entry Register 15BL	GAFLML15	16	16	2 or 3 PCLKB	2 ICLK
000A 8458h	CAN	Receive Buffer Register 11CL	RMDF011	16	16	2 or 3 PCLKB	2 ICLK
000A 845Ah	CAN	Receive Rule Entry Register 15BH	GAFLMH15	16	16	2 or 3 PCLKB	2 ICLK
000A 845Ah	CAN	Receive Buffer Register 11CH	RMDF111	16	16	2 or 3 PCLKB	2 ICLK
000A 845Ch	CAN	Receive Rule Entry Register 15CL	GAFLPL15	16	16	2 or 3 PCLKB	2 ICLK
000A 845Ch	CAN	Receive Buffer Register 11DL	RMDF211	16	16	2 or 3 PCLKB	2 ICLK
000A 845Eh	CAN	Receive Rule Entry Register 15CH	GAFLPH15	16	16	2 or 3 PCLKB	2 ICLK
000A 845Eh	CAN	Receive Buffer Register 11DH	RMDF311	16	16	2 or 3 PCLKB	2 ICLK
000A 8460h	CAN	Receive Buffer Register 12AL	RMIDL12	16	16	2 or 3 PCLKB	2 ICLK
000A 8462h	CAN	Receive Buffer Register 12AH	RMIDH12	16	16	2 or 3 PCLKB	2 ICLK
000A 8464h	CAN	Receive Buffer Register 12BL	RMTS12	16	16	2 or 3 PCLKB	2 ICLK
000A 8466h	CAN	Receive Buffer Register 12BH	RMPTR12	16	16	2 or 3 PCLKB	2 ICLK
000A 8468h	CAN	Receive Buffer Register 12CL	RMDF012	16	16	2 or 3 PCLKB	2 ICLK
000A 846Ah	CAN	Receive Buffer Register 12CH	RMDF112	16	16	2 or 3 PCLKB	2 ICLK
000A 846Ch	CAN	Receive Buffer Register 12DL	RMDF212	16	16	2 or 3 PCLKB	2 ICLK
000A 846Eh	CAN	Receive Buffer Register 12DH	RMDF312	16	16	2 or 3 PCLKB	2 ICLK
000A 8470h	CAN	Receive Buffer Register 13AL	RMIDL13	16	16	2 or 3 PCLKB	2 ICLK
000A 8472h	CAN	Receive Buffer Register 13AH	RMIDH13	16	16	2 or 3 PCLKB	2 ICLK
000A 8474h	CAN	Receive Buffer Register 13BL	RMTS13	16	16	2 or 3 PCLKB	2 ICLK
000A 8476h	CAN	Receive Buffer Register 13BH	RMPTR13	16	16	2 or 3 PCLKB	2 ICLK
000A 8478h	CAN	Receive Buffer Register 13CL	RMDF013	16	16	2 or 3 PCLKB	2 ICLK
000A 847Ah	CAN	Receive Buffer Register 13CH	RMDF113	16	16	2 or 3 PCLKB	2 ICLK

Table 4.1 List of I/O Registers (Address Order) (37 / 42)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles	
						ICLK ≥ PCLK	ICLK < PCLK
000A 847Ch	CAN	Receive Buffer Register 13DL	RMDF213	16	16	2 or 3 PCLKB	2 ICLK
000A 847Eh	CAN	Receive Buffer Register 13DH	RMDF313	16	16	2 or 3 PCLKB	2 ICLK
000A 8480h	CAN	Receive Buffer Register 14AL	RMIDL14	16	16	2 or 3 PCLKB	2 ICLK
000A 8482h	CAN	Receive Buffer Register 14AH	RMIDH14	16	16	2 or 3 PCLKB	2 ICLK
000A 8484h	CAN	Receive Buffer Register 14BL	RMTS14	16	16	2 or 3 PCLKB	2 ICLK
000A 8486h	CAN	Receive Buffer Register 14BH	RMPTR14	16	16	2 or 3 PCLKB	2 ICLK
000A 8488h	CAN	Receive Buffer Register 14CL	RMDF014	16	16	2 or 3 PCLKB	2 ICLK
000A 848Ah	CAN	Receive Buffer Register 14CH	RMDF114	16	16	2 or 3 PCLKB	2 ICLK
000A 848Ch	CAN	Receive Buffer Register 14DL	RMDF214	16	16	2 or 3 PCLKB	2 ICLK
000A 848Eh	CAN	Receive Buffer Register 14DH	RMDF314	16	16	2 or 3 PCLKB	2 ICLK
000A 8490h	CAN	Receive Buffer Register 15AL	RMIDL15	16	16	2 or 3 PCLKB	2 ICLK
000A 8492h	CAN	Receive Buffer Register 15AH	RMIDH15	16	16	2 or 3 PCLKB	2 ICLK
000A 8494h	CAN	Receive Buffer Register 15BL	RMTS15	16	16	2 or 3 PCLKB	2 ICLK
000A 8496h	CAN	Receive Buffer Register 15BH	RMPTR15	16	16	2 or 3 PCLKB	2 ICLK
000A 8498h	CAN	Receive Buffer Register 15CL	RMDF015	16	16	2 or 3 PCLKB	2 ICLK
000A 849Ah	CAN	Receive Buffer Register 15CH	RMDF115	16	16	2 or 3 PCLKB	2 ICLK
000A 849Ch	CAN	Receive Buffer Register 15DL	RMDF215	16	16	2 or 3 PCLKB	2 ICLK
000A 849Eh	CAN	Receive Buffer Register 15DH	RMDF315	16	16	2 or 3 PCLKB	2 ICLK
000A 8580h to 000A 859Fh	CAN	RAM Test Register 0 to 15	RPGACC0 to 15	16	16	2 or 3 PCLKB	2 ICLK
000A 85A0h	CAN	Receive FIFO Access Register 0AL	RFIDL0	16	16	2 or 3 PCLKB	2 ICLK
000A 85A0h	CAN	RAM Test Register 16	RPGACC16	16	16	2 or 3 PCLKB	2 ICLK
000A 85A2h	CAN	Receive FIFO Access Register 0AH	RFIDH0	16	16	2 or 3 PCLKB	2 ICLK
000A 85A2h	CAN	RAM Test Register 17	RPGACC17	16	16	2 or 3 PCLKB	2 ICLK
000A 85A4h	CAN	Receive FIFO Access Register 0BL	RFTS0	16	16	2 or 3 PCLKB	2 ICLK
000A 85A4h	CAN	RAM Test Register 18	RPGACC18	16	16	2 or 3 PCLKB	2 ICLK
000A 85A6h	CAN	Receive FIFO Access Register 0BH	RFPTR0	16	16	2 or 3 PCLKB	2 ICLK
000A 85A6h	CAN	RAM Test Register 19	RPGACC19	16	16	2 or 3 PCLKB	2 ICLK
000A 85A8h	CAN	Receive FIFO Access Register 0CL	RFDF00	16	16	2 or 3 PCLKB	2 ICLK
000A 85A8h	CAN	RAM Test Register 20	RPGACC20	16	16	2 or 3 PCLKB	2 ICLK
000A 85AAh	CAN	Receive FIFO Access Register 0CH	RFDF10	16	16	2 or 3 PCLKB	2 ICLK
000A 85AAh	CAN	RAM Test Register 21	RPGACC21	16	16	2 or 3 PCLKB	2 ICLK
000A 85ACh	CAN	Receive FIFO Access Register 0DL	RFDF20	16	16	2 or 3 PCLKB	2 ICLK
000A 85ACh	CAN	RAM Test Register 22	RPGACC22	16	16	2 or 3 PCLKB	2 ICLK
000A 85AEh	CAN	Receive FIFO Access Register 0DH	RFDF30	16	16	2 or 3 PCLKB	2 ICLK
000A 85AEh	CAN	RAM Test Register 23	RPGACC23	16	16	2 or 3 PCLKB	2 ICLK
000A 85B0h	CAN	Receive FIFO Access Register 1AL	RFIDL1	16	16	2 or 3 PCLKB	2 ICLK
000A 85B0h	CAN	RAM Test Register 24	RPGACC24	16	16	2 or 3 PCLKB	2 ICLK
000A 85B2h	CAN	Receive FIFO Access Register 1AH	RFIDH1	16	16	2 or 3 PCLKB	2 ICLK
000A 85B2h	CAN	RAM Test Register 25	RPGACC25	16	16	2 or 3 PCLKB	2 ICLK
000A 85B4h	CAN	Receive FIFO Access Register 1BL	RFTS1	16	16	2 or 3 PCLKB	2 ICLK
000A 85B4h	CAN	RAM Test Register 26	RPGACC26	16	16	2 or 3 PCLKB	2 ICLK
000A 85B6h	CAN	Receive FIFO Access Register 1BH	RFPTR1	16	16	2 or 3 PCLKB	2 ICLK
000A 85B6h	CAN	RAM Test Register 27	RPGACC27	16	16	2 or 3 PCLKB	2 ICLK
000A 85B8h	CAN	Receive FIFO Access Register 1CL	RFDF01	16	16	2 or 3 PCLKB	2 ICLK
000A 85B8h	CAN	RAM Test Register 28	RPGACC28	16	16	2 or 3 PCLKB	2 ICLK
000A 85BAh	CAN	Receive FIFO Access Register 1CH	RFDF11	16	16	2 or 3 PCLKB	2 ICLK
000A 85BAh	CAN	RAM Test Register 29	RPGACC29	16	16	2 or 3 PCLKB	2 ICLK
000A 85BCh	CAN	Receive FIFO Access Register 1DL	RFDF21	16	16	2 or 3 PCLKB	2 ICLK
000A 85BCh	CAN	RAM Test Register 30	RPGACC30	16	16	2 or 3 PCLKB	2 ICLK
000A 85BEh	CAN	Receive FIFO Access Register 1DH	RFDF31	16	16	2 or 3 PCLKB	2 ICLK
000A 85BEh	CAN	RAM Test Register 31	RPGACC31	16	16	2 or 3 PCLKB	2 ICLK

Table 4.1 List of I/O Registers (Address Order) (38 / 42)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles	
						ICLK ≥ PCLK	ICLK < PCLK
000A 85C0h to 000A 85DEh	CAN	RAM Test Register 32 to 47	RPGACC32 to 47	16	16	2 or 3 PCLKB	2 ICLK
000A 85E0h	CAN0	Transmit/Receive FIFO Access Register 0AL	CFIDL0	16	16	2 or 3 PCLKB	2 ICLK
000A 85E0h	CAN	RAM Test Register 48	RPGACC48	16	16	2 or 3 PCLKB	2 ICLK
000A 85E2h	CAN0	Transmit/Receive FIFO Access Register 0AH	CFIDH0	16	16	2 or 3 PCLKB	2 ICLK
000A 85E2h	CAN	RAM Test Register 49	RPGACC49	16	16	2 or 3 PCLKB	2 ICLK
000A 85E4h	CAN0	Transmit/Receive FIFO Access Register 0BL	CFTS0	16	16	2 or 3 PCLKB	2 ICLK
000A 85E4h	CAN	RAM Test Register 50	RPGACC50	16	16	2 or 3 PCLKB	2 ICLK
000A 85E6h	CAN0	Transmit/Receive FIFO Access Register 0BH	CFPTR0	16	16	2 or 3 PCLKB	2 ICLK
000A 85E6h	CAN	RAM Test Register 51	RPGACC51	16	16	2 or 3 PCLKB	2 ICLK
000A 85E8h	CAN0	Transmit/Receive FIFO Access Register 0CL	CFDF00	16	16	2 or 3 PCLKB	2 ICLK
000A 85E8h	CAN	RAM Test Register 52	RPGACC52	16	16	2 or 3 PCLKB	2 ICLK
000A 85EAh	CAN0	Transmit/Receive FIFO Access Register 0CH	CFDF10	16	16	2 or 3 PCLKB	2 ICLK
000A 85EAh	CAN	RAM Test Register 53	RPGACC53	16	16	2 or 3 PCLKB	2 ICLK
000A 85ECh	CAN0	Transmit/Receive FIFO Access Register 0DL	CFDF20	16	16	2 or 3 PCLKB	2 ICLK
000A 85ECh	CAN	RAM Test Register 54	RPGACC54	16	16	2 or 3 PCLKB	2 ICLK
000A 85EEh	CAN0	Transmit/Receive FIFO Access Register 0DH	CFDF30	16	16	2 or 3 PCLKB	2 ICLK
000A 85EEh	CAN	RAM Test Register 55	RPGACC55	16	16	2 or 3 PCLKB	2 ICLK
000A 85F0h to 000A 85FEh	CAN	RAM Test Register 56 to 63	RPGACC56 to 63	16	16	2 or 3 PCLKB	2 ICLK
000A 8600h	CAN0	Transmit Buffer Register 0AL	TMIDL0	16	16	2 or 3 PCLKB	2 ICLK
000A 8600h	CAN	RAM Test Register 64	RPGACC64	16	16	2 or 3 PCLKB	2 ICLK
000A 8602h	CAN0	Transmit Buffer Register 0AH	TMIDH0	16	16	2 or 3 PCLKB	2 ICLK
000A 8602h	CAN	RAM Test Register 65	RPGACC65	16	16	2 or 3 PCLKB	2 ICLK
000A 8604h	CAN	RAM Test Register 66	RPGACC66	16	16	2 or 3 PCLKB	2 ICLK
000A 8606h	CAN0	Transmit Buffer Register 0BH	TMPTR0	16	16	2 or 3 PCLKB	2 ICLK
000A 8606h	CAN	RAM Test Register 67	RPGACC67	16	16	2 or 3 PCLKB	2 ICLK
000A 8608h	CAN0	Transmit Buffer Register 0CL	TMDF00	16	16	2 or 3 PCLKB	2 ICLK
000A 8608h	CAN	RAM Test Register 68	RPGACC68	16	16	2 or 3 PCLKB	2 ICLK
000A 860Ah	CAN0	Transmit Buffer Register 0CH	TMDF10	16	16	2 or 3 PCLKB	2 ICLK
000A 860Ah	CAN	RAM Test Register 69	RPGACC69	16	16	2 or 3 PCLKB	2 ICLK
000A 860Ch	CAN0	Transmit Buffer Register 0DL	TMDF20	16	16	2 or 3 PCLKB	2 ICLK
000A 860Ch	CAN	RAM Test Register 70	RPGACC70	16	16	2 or 3 PCLKB	2 ICLK
000A 860Eh	CAN0	Transmit Buffer Register 0DH	TMDF30	16	16	2 or 3 PCLKB	2 ICLK
000A 860Eh	CAN	RAM Test Register 71	RPGACC71	16	16	2 or 3 PCLKB	2 ICLK
000A 8610h	CAN0	Transmit Buffer Register 1AL	TMIDL1	16	16	2 or 3 PCLKB	2 ICLK
000A 8610h	CAN	RAM Test Register 72	RPGACC72	16	16	2 or 3 PCLKB	2 ICLK
000A 8612h	CAN0	Transmit Buffer Register 1AH	TMIDH1	16	16	2 or 3 PCLKB	2 ICLK
000A 8612h	CAN	RAM Test Register 73	RPGACC73	16	16	2 or 3 PCLKB	2 ICLK
000A 8614h	CAN	RAM Test Register 74	RPGACC74	16	16	2 or 3 PCLKB	2 ICLK
000A 8616h	CAN0	Transmit Buffer Register 1BH	TMPTR1	16	16	2 or 3 PCLKB	2 ICLK
000A 8616h	CAN	RAM Test Register 75	RPGACC75	16	16	2 or 3 PCLKB	2 ICLK
000A 8618h	CAN0	Transmit Buffer Register 1CL	TMDF01	16	16	2 or 3 PCLKB	2 ICLK
000A 8618h	CAN	RAM Test Register 76	RPGACC76	16	16	2 or 3 PCLKB	2 ICLK
000A 861Ah	CAN0	Transmit Buffer Register 1CH	TMDF11	16	16	2 or 3 PCLKB	2 ICLK
000A 861Ah	CAN	RAM Test Register 77	RPGACC77	16	16	2 or 3 PCLKB	2 ICLK
000A 861Ch	CAN0	Transmit Buffer Register 1DL	TMDF21	16	16	2 or 3 PCLKB	2 ICLK
000A 861Ch	CAN	RAM Test Register 78	RPGACC78	16	16	2 or 3 PCLKB	2 ICLK
000A 861Eh	CAN0	Transmit Buffer Register 1DH	TMDF31	16	16	2 or 3 PCLKB	2 ICLK
000A 861Eh	CAN	RAM Test Register 79	RPGACC79	16	16	2 or 3 PCLKB	2 ICLK
000A 8620h	CAN0	Transmit Buffer Register 2AL	TMIDL2	16	16	2 or 3 PCLKB	2 ICLK
000A 8620h	CAN	RAM Test Register 80	RPGACC80	16	16	2 or 3 PCLKB	2 ICLK

Table 4.1 List of I/O Registers (Address Order) (39 / 42)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles	
						ICLK ≥ PCLK	ICLK < PCLK
000A 8622h	CAN0	Transmit Buffer Register 2AH	TMIDH2	16	16	2 or 3 PCLKB	2 ICLK
000A 8622h	CAN	RAM Test Register 81	RPGACC81	16	16	2 or 3 PCLKB	2 ICLK
000A 8624h	CAN	RAM Test Register 82	RPGACC82	16	16	2 or 3 PCLKB	2 ICLK
000A 8626h	CAN0	Transmit Buffer Register 2BH	TMPTR2	16	16	2 or 3 PCLKB	2 ICLK
000A 8626h	CAN	RAM Test Register 83	RPGACC83	16	16	2 or 3 PCLKB	2 ICLK
000A 8628h	CAN0	Transmit Buffer Register 2CL	TMDFO2	16	16	2 or 3 PCLKB	2 ICLK
000A 8628h	CAN	RAM Test Register 84	RPGACC84	16	16	2 or 3 PCLKB	2 ICLK
000A 862Ah	CAN0	Transmit Buffer Register 2CH	TMDF12	16	16	2 or 3 PCLKB	2 ICLK
000A 862Ah	CAN	RAM Test Register 85	RPGACC85	16	16	2 or 3 PCLKB	2 ICLK
000A 862Ch	CAN0	Transmit Buffer Register 2DL	TMDF22	16	16	2 or 3 PCLKB	2 ICLK
000A 862Ch	CAN	RAM Test Register 86	RPGACC86	16	16	2 or 3 PCLKB	2 ICLK
000A 862Eh	CAN0	Transmit Buffer Register 2DH	TMDF32	16	16	2 or 3 PCLKB	2 ICLK
000A 862Eh	CAN	RAM Test Register 87	RPGACC87	16	16	2 or 3 PCLKB	2 ICLK
000A 8630h	CAN0	Transmit Buffer Register 3AL	TMIDL3	16	16	2 or 3 PCLKB	2 ICLK
000A 8630h	CAN	RAM Test Register 88	RPGACC88	16	16	2 or 3 PCLKB	2 ICLK
000A 8632h	CAN0	Transmit Buffer Register 3AH	TMIDH3	16	16	2 or 3 PCLKB	2 ICLK
000A 8632h	CAN	RAM Test Register 89	RPGACC89	16	16	2 or 3 PCLKB	2 ICLK
000A 8634h	CAN	RAM Test Register 90	RPGACC90	16	16	2 or 3 PCLKB	2 ICLK
000A 8636h	CAN0	Transmit Buffer Register 3BH	TMPTR3	16	16	2 or 3 PCLKB	2 ICLK
000A 8636h	CAN	RAM Test Register 91	RPGACC91	16	16	2 or 3 PCLKB	2 ICLK
000A 8638h	CAN0	Transmit Buffer Register 3CL	TMDFO3	16	16	2 or 3 PCLKB	2 ICLK
000A 8638h	CAN	RAM Test Register 92	RPGACC92	16	16	2 or 3 PCLKB	2 ICLK
000A 863Ah	CAN0	Transmit Buffer Register 3CH	TMDF13	16	16	2 or 3 PCLKB	2 ICLK
000A 863Ah	CAN	RAM Test Register 93	RPGACC93	16	16	2 or 3 PCLKB	2 ICLK
000A 863Ch	CAN0	Transmit Buffer Register 3DL	TMDF23	16	16	2 or 3 PCLKB	2 ICLK
000A 863Ch	CAN	RAM Test Register 94	RPGACC94	16	16	2 or 3 PCLKB	2 ICLK
000A 863Eh	CAN0	Transmit Buffer Register 3DH	TMDF33	16	16	2 or 3 PCLKB	2 ICLK
000A 863Eh	CAN	RAM Test Register 95	RPGACC95	16	16	2 or 3 PCLKB	2 ICLK
000A 8640h to 000A 867Eh	CAN	RAM Test Register 96 to 127	RPGACC96 to 127	16	16	2 or 3 PCLKB	2 ICLK
000A 8680h	CAN0	Transmit History Buffer Access Register	THLACC0	16	16	2 or 3 PCLKB	2 ICLK
000D 0A00h	MTU3	Timer Control Register	TCR	8	8	2 or 3 PCLKB	2 ICLK
000D 0A01h	MTU4	Timer Control Register	TCR	8	8	2 or 3 PCLKB	2 ICLK
000D 0A02h	MTU3	Timer Mode Register	TMDR	8	8	2 or 3 PCLKB	2 ICLK
000D 0A03h	MTU4	Timer Mode Register	TMDR	8	8	2 or 3 PCLKB	2 ICLK
000D 0A04h	MTU3	Timer I/O Control Register H	TIORH	8	8	2 or 3 PCLKB	2 ICLK
000D 0A05h	MTU3	Timer I/O Control Register L	TIORL	8	8	2 or 3 PCLKB	2 ICLK
000D 0A06h	MTU4	Timer I/O Control Register H	TIORH	8	8	2 or 3 PCLKB	2 ICLK
000D 0A07h	MTU4	Timer I/O Control Register L	TIORL	8	8	2 or 3 PCLKB	2 ICLK
000D 0A08h	MTU3	Timer Interrupt Enable Register	TIER	8	8	2 or 3 PCLKB	2 ICLK
000D 0A09h	MTU4	Timer Interrupt Enable Register	TIER	8	8	2 or 3 PCLKB	2 ICLK
000D 0A0Ah	MTU	Timer Output Master Enable Register	TOER	8	8	2 or 3 PCLKB	2 ICLK
000D 0A0Dh	MTU	Timer Gate Control Register	TGCR	8	8	2 or 3 PCLKB	2 ICLK
000D 0A0Eh	MTU	Timer Output Control Register 1	TOCR1	8	8	2 or 3 PCLKB	2 ICLK
000D 0A0Fh	MTU	Timer Output Control Register 2	TOCR2	8	8	2 or 3 PCLKB	2 ICLK
000D 0A10h	MTU3	Timer Counter	TCNT	16	16	2 or 3 PCLKB	2 ICLK
000D 0A12h	MTU4	Timer Counter	TCNT	16	16	2 or 3 PCLKB	2 ICLK
000D 0A14h	MTU	Timer Cycle Data Register	TCDR	16	16	2 or 3 PCLKB	2 ICLK
000D 0A16h	MTU	Timer Dead Time Data Register	TDDR	16	16	2 or 3 PCLKB	2 ICLK
000D 0A18h	MTU3	Timer General Register A	TGRA	16	16	2 or 3 PCLKB	2 ICLK
000D 0A1Ah	MTU3	Timer General Register B	TGRB	16	16	2 or 3 PCLKB	2 ICLK
000D 0A1Ch	MTU4	Timer General Register A	TGRA	16	16	2 or 3 PCLKB	2 ICLK

Table 4.1 List of I/O Registers (Address Order) (40 / 42)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles	
						ICLK ≥ PCLK	ICLK < PCLK
000D 0A1Eh	MTU4	Timer General Register B	TGRB	16	16	2 or 3 PCLKB	2 ICLK
000D 0A20h	MTU	Timer Subcounters	TCNTS	16	16	2 or 3 PCLKB	2 ICLK
000D 0A22h	MTU	Timer Cycle Buffer Register	TCBR	16	16	2 or 3 PCLKB	2 ICLK
000D 0A24h	MTU3	Timer General Register C	TGRC	16	16	2 or 3 PCLKB	2 ICLK
000D 0A26h	MTU3	Timer General Register D	TGRD	16	16	2 or 3 PCLKB	2 ICLK
000D 0A28h	MTU4	Timer General Register C	TGRC	16	16	2 or 3 PCLKB	2 ICLK
000D 0A2Ah	MTU4	Timer General Register D	TGRD	16	16	2 or 3 PCLKB	2 ICLK
000D 0A2Ch	MTU3	Timer Status Register	TSR	8	8	2 or 3 PCLKB	2 ICLK
000D 0A2Dh	MTU4	Timer Status Register	TSR	8	8	2 or 3 PCLKB	2 ICLK
000D 0A30h	MTU	Timer Interrupt Skipping Set Register	TITCR	8	8	2 or 3 PCLKB	2 ICLK
000D 0A31h	MTU	Timer Interrupt Skipping Counters	TITCNT	8	8	2 or 3 PCLKB	2 ICLK
000D 0A32h	MTU	Timer Buffer Transfer Set Register	TBTER	8	8	2 or 3 PCLKB	2 ICLK
000D 0A34h	MTU	Timer Dead Time Enable Register	TDER	8	8	2 or 3 PCLKB	2 ICLK
000D 0A36h	MTU	Timer Output Level Buffer Register	TOLBR	8	8	2 or 3 PCLKB	2 ICLK
000D 0A38h	MTU3	Timer Buffer Operation Transfer Mode Register	TBTM	8	8	2 or 3 PCLKB	2 ICLK
000D 0A39h	MTU4	Timer Buffer Operation Transfer Mode Register	TBTM	8	8	2 or 3 PCLKB	2 ICLK
000D 0A40h	MTU4	Timer A/D Converter Start Request Control Register	TADCR	16	16	2 or 3 PCLKB	2 ICLK
000D 0A44h	MTU4	Timer A/D Converter Start Request Cycle Set Register A	TADCORA	16	16	2 or 3 PCLKB	2 ICLK
000D 0A46h	MTU4	Timer A/D Converter Start Request Cycle Set Register B	TADCORB	16	16	2 or 3 PCLKB	2 ICLK
000D 0A48h	MTU4	Timer A/D Converter Start Request Cycle Set Buffer Register A	TADCOBRA	16	16	2 or 3 PCLKB	2 ICLK
000D 0A4Ah	MTU4	Timer A/D Converter Start Request Cycle Set Buffer Register B	TADCOBRB	16	16	2 or 3 PCLKB	2 ICLK
000D 0A60h	MTU	Timer Waveform Control Register	TWCR	8	8, 16	2 or 3 PCLKB	2 ICLK
000D 0A80h	MTU	Timer Start Register	TSTR	8	8, 16	2 or 3 PCLKB	2 ICLK
000D 0A81h	MTU	Timer Synchronous Register	TSYR	8	8, 16	2 or 3 PCLKB	2 ICLK
000D 0A84h	MTU	Timer Read/Write Enable Register	TRWER	8	8, 16	2 or 3 PCLKB	2 ICLK
000D 0A90h	MTU0	Noise Filter Control Register	NFCR	8	8, 16	2 or 3 PCLKB	2 ICLK
000D 0A91h	MTU1	Noise Filter Control Register	NFCR	8	8, 16	2 or 3 PCLKB	2 ICLK
000D 0A92h	MTU2	Noise Filter Control Register	NFCR	8	8, 16	2 or 3 PCLKB	2 ICLK
000D 0A93h	MTU3	Noise Filter Control Register	NFCR	8	8, 16	2 or 3 PCLKB	2 ICLK
000D 0A94h	MTU4	Noise Filter Control Register	NFCR	8	8, 16	2 or 3 PCLKB	2 ICLK
000D 0A95h	MTU5	Noise Filter Control Register	NFCR	8	8, 16	2 or 3 PCLKB	2 ICLK
000D 0B00h	MTU0	Timer Control Register	TCR	8	8	2 or 3 PCLKB	2 ICLK
000D 0B01h	MTU0	Timer Mode Register	TMDR	8	8	2 or 3 PCLKB	2 ICLK
000D 0B02h	MTU0	Timer I/O Control Register H	TIORH	8	8	2 or 3 PCLKB	2 ICLK
000D 0B03h	MTU0	Timer I/O Control Register L	TIORL	8	8	2 or 3 PCLKB	2 ICLK
000D 0B04h	MTU0	Timer Interrupt Enable Register	TIER	8	8	2 or 3 PCLKB	2 ICLK
000D 0B05h	MTU0	Timer Status Register	TSR	8	8	2 or 3 PCLKB	2 ICLK
000D 0B06h	MTU0	Timer Counter	TCNT	16	16	2 or 3 PCLKB	2 ICLK
000D 0B08h	MTU0	Timer General Register A	TGRA	16	16	2 or 3 PCLKB	2 ICLK
000D 0B0Ah	MTU0	Timer General Register B	TGRB	16	16	2 or 3 PCLKB	2 ICLK
000D 0B0Ch	MTU0	Timer General Register C	TGRC	16	16	2 or 3 PCLKB	2 ICLK
000D 0B0Eh	MTU0	Timer General Register D	TGRD	16	16	2 or 3 PCLKB	2 ICLK
000D 0B20h	MTU0	Timer General Register E	TGRE	16	16	2 or 3 PCLKB	2 ICLK
000D 0B22h	MTU0	Timer General Register F	TGRF	16	16	2 or 3 PCLKB	2 ICLK
000D 0B24h	MTU0	Timer Interrupt Enable Register 2	TIER2	8	8	2 or 3 PCLKB	2 ICLK
000D 0B26h	MTU0	Timer Buffer Operation Transfer Mode Register	TBTM	8	8	2 or 3 PCLKB	2 ICLK
000D 0B80h	MTU1	Timer Control Register	TCR	8	8	2 or 3 PCLKB	2 ICLK
000D 0B81h	MTU1	Timer Mode Register	TMDR	8	8	2 or 3 PCLKB	2 ICLK
000D 0B82h	MTU1	Timer I/O Control Register	TIOR	8	8	2 or 3 PCLKB	2 ICLK
000D 0B84h	MTU1	Timer Interrupt Enable Register	TIER	8	8	2 or 3 PCLKB	2 ICLK
000D 0B85h	MTU1	Timer Status Register	TSR	8	8	2 or 3 PCLKB	2 ICLK

Table 4.1 List of I/O Registers (Address Order) (41 / 42)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles	
						ICLK ≥ PCLK	ICLK < PCLK
000D 0B86h	MTU1	Timer Counter	TCNT	16	16	2 or 3 PCLKB	2 ICLK
000D 0B88h	MTU1	Timer General Register A	TGRA	16	16	2 or 3 PCLKB	2 ICLK
000D 0B8Ah	MTU1	Timer General Register B	TGRB	16	16	2 or 3 PCLKB	2 ICLK
000D 0B90h	MTU1	Timer Input Capture Control Register	TICCR	8	8	2 or 3 PCLKB	2 ICLK
000D 0C00h	MTU2	Timer Control Register	TCR	8	8	2 or 3 PCLKB	2 ICLK
000D 0C01h	MTU2	Timer Mode Register	TMDR	8	8	2 or 3 PCLKB	2 ICLK
000D 0C02h	MTU2	Timer I/O Control Register	TIOR	8	8	2 or 3 PCLKB	2 ICLK
000D 0C04h	MTU2	Timer Interrupt Enable Register	TIER	8	8	2 or 3 PCLKB	2 ICLK
000D 0C05h	MTU2	Timer Status Register	TSR	8	8	2 or 3 PCLKB	2 ICLK
000D 0C06h	MTU2	Timer Counter	TCNT	16	16	2 or 3 PCLKB	2 ICLK
000D 0C08h	MTU2	Timer General Register A	TGRA	16	16	2 or 3 PCLKB	2 ICLK
000D 0C0Ah	MTU2	Timer General Register B	TGRB	16	16	2 or 3 PCLKB	2 ICLK
000D 0C80h	MTU5	Timer Counter U	TCNTU	16	16	2 or 3 PCLKB	2 ICLK
000D 0C82h	MTU5	Timer General Register U	TGRU	16	16	2 or 3 PCLKB	2 ICLK
000D 0C84h	MTU5	Timer Control Register U	TCRU	8	8	2 or 3 PCLKB	2 ICLK
000D 0C86h	MTU5	Timer I/O Control Register U	TIORU	8	8	2 or 3 PCLKB	2 ICLK
000D 0C90h	MTU5	Timer Counter V	TCNTV	16	16	2 or 3 PCLKB	2 ICLK
000D 0C92h	MTU5	Timer General Register V	TGRV	16	16	2 or 3 PCLKB	2 ICLK
000D 0C94h	MTU5	Timer Control Register V	TCRV	8	8	2 or 3 PCLKB	2 ICLK
000D 0C96h	MTU5	Timer I/O Control Register V	TIORV	8	8	2 or 3 PCLKB	2 ICLK
000D 0CA0h	MTU5	Timer Counter W	TCNTW	16	16	2 or 3 PCLKB	2 ICLK
000D 0CA2h	MTU5	Timer General Register W	TGRW	16	16	2 or 3 PCLKB	2 ICLK
000D 0CA4h	MTU5	Timer Control Register W	TCRW	8	8	2 or 3 PCLKB	2 ICLK
000D 0CA6h	MTU5	Timer I/O Control Register W	TIORW	8	8	2 or 3 PCLKB	2 ICLK
000D 0CB2h	MTU5	Timer Interrupt Enable Register	TIER	8	8	2 or 3 PCLKB	2 ICLK
000D 0CB4h	MTU5	Timer Start Register	TSTR	8	8	2 or 3 PCLKB	2 ICLK
000D 0CB6h	MTU5	Timer Compare Match Clear Register	TCNTCMPCLR	8	8	2 or 3 PCLKB	2 ICLK
007F C090h	FLASH	E2 DataFlash Control Register	DFCTL	8	8	2 or 3 PCLKB	2 ICLK
007F C0ACh	TEMPSPA	Temperature Sensor Calibration Data Register L	TSCDRL	8	8	2 or 3 PCLKB	2 ICLK
007F C0ADh	TEMPSPA	Temperature Sensor Calibration Data Register H	TSCDRH	8	8	2 or 3 PCLKB	2 ICLK
007F C100h	FLASH	Flash P/E Mode Control Register	FPMCR	8	8	2 or 3 PCLKB	2 ICLK
007F C104h	FLASH	Flash Area Select Register	FASR	8	8	2 or 3 PCLKB	2 ICLK
007F C108h	FLASH	Flash Processing Start Address Register L	FSARL	16	16	2 or 3 PCLKB	2 ICLK
007F C110h	FLASH	Flash Processing Start Address Register H	FSARH	16	16	2 or 3 PCLKB	2 ICLK
007F C114h	FLASH	Flash Control Register	FCR	8	8	2 or 3 PCLKB	2 ICLK
007F C118h	FLASH	Flash Processing End Address Register L	FEARL	16	16	2 or 3 PCLKB	2 ICLK
007F C120h	FLASH	Flash Processing End Address Register H	FEARH	16	16	2 or 3 PCLKB	2 ICLK
007F C124h	FLASH	Flash Reset Register	FRESETR	8	8	2 or 3 PCLKB	2 ICLK
007F C12Ch	FLASH	Flash Status Register 1	FSTATR1	8	8	2 or 3 PCLKB	2 ICLK
007F C130h	FLASH	Flash Write Buffer Register 0	FWB0	16	16	2 or 3 PCLKB	2 ICLK
007F C138h	FLASH	Flash Write Buffer Register 1	FWB1	16	16	2 or 3 PCLKB	2 ICLK
007F C140h	FLASH	Flash Write Buffer Register 2	FWB2	16	16	2 or 3 PCLKB	2 ICLK
007F C144h	FLASH	Flash Write Buffer Register 3	FWB3	16	16	2 or 3 PCLKB	2 ICLK
007F C180h	FLASH	Protection Unlock Register	FPR	8	8	2 or 3 PCLKB	2 ICLK
007F C184h	FLASH	Protection Unlock Status Register	FPSR	8	8	2 or 3 PCLKB	2 ICLK
007F C1C0h	FLASH	Flash Start-Up Setting Monitor Register	FSCMR	16	16	2 or 3 PCLKB	2 ICLK
007F C1C8h	FLASH	Flash Access Window Start Address Monitor Register	FAWSMR	16	16	2 or 3 PCLKB	2 ICLK
007F C1D0h	FLASH	Flash Access Window End Address Monitor Register	FAWEMR	16	16	2 or 3 PCLKB	2 ICLK
007F C1D8h	FLASH	Flash Initial Setting Register	FISR	8	8	2 or 3 PCLKB	2 ICLK
007F C1DCh	FLASH	Flash Extra Area Control Register	FEXCR	8	8	2 or 3 PCLKB	2 ICLK
007F C1E0h	FLASH	Flash Error Address Monitor Register L	FEAML	16	16	2 or 3 PCLKB	2 ICLK
007F C1E8h	FLASH	Flash Error Address Monitor Register H	FEAMH	8	8	2 or 3 PCLKB	2 ICLK

Table 4.1 List of I/O Registers (Address Order) (42 / 42)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles	
						ICLK \geq PCLK	ICLK $<$ PCLK
007F C1F0h	FLASH	Flash Status Register 0	FSTATR0	8	8	2 or 3 PCLKB	2 ICLK
007F C350h	FLASHCON ST	Unique ID Register 0	UIDR0	32	32	2 or 3 PCLKB	2 ICLK
007F C354h	FLASHCON ST	Unique ID Register 1	UIDR1	32	32	2 or 3 PCLKB	2 ICLK
007F C358h	FLASHCON ST	Unique ID Register 2	UIDR2	32	32	2 or 3 PCLKB	2 ICLK
007F C35Ch	FLASHCON ST	Unique ID Register 3	UIDR3	32	32	2 or 3 PCLKB	2 ICLK
007F FFB2h	FLASH	Flash P/E Mode Entry Register	FENTRYR	16	16	2 or 3 PCLKB	2 ICLK

Note 1. Odd addresses cannot be accessed in 16-bit units. Table 26.4 lists register allocation for 16-bit access in the User's Manual: Hardware.

Note 2. When the register is accessed while the USB is operating, a delay may be generated in accessing.

5. Electrical Characteristics

5.1 Absolute Maximum Ratings

Table 5.1 Absolute Maximum Ratings

Conditions: VSS = AVSS0 = VREFL0 = VREFL = VSS_USB = 0 V

Item	Symbol	Value	Unit	
Power supply voltage	VCC, VCC_USB	-0.3 to +6.5	V	
VBATT power supply voltage	Vbatt	-0.3 to +6.5	V	
Input voltage	Ports for 5 V tolerant*1	V _{in}	V	
	P03, P05, P40 to P47			-0.3 to AVCC0 +0.3
	Ports other than above			-0.3 to VCC +0.3
Reference power supply voltage	VREFH0	-0.3 to AVCC0 +0.3	V	
	VREFH			
Analog power supply voltage	AVCC0	-0.3 to +6.5	V	
Analog input voltage	When AN000 to AN007 are used	V _{AN}	V	
	When AN016 to AN031 are used			-0.3 to VCC +0.3
Operating temperature*2	T _{opr}	-40 to +85 -40 to +105	°C	
Storage temperature	T _{stg}	-55 to +125	°C	

Caution: Permanent damage to the MCU may be caused if absolute maximum ratings are exceeded.

To preclude any malfunctions due to noise interference, insert capacitors with high frequency characteristics between the VCC and VSS pins, between the AVCC0 and AVSS0 pins, between the VCC_USB and VSS_USB pins, between the VREFH0 and VREFL0 pins, and between the VREFH and VREFL pins. Place capacitors of about 0.1 μF as close as possible to every power supply pin and use the shortest and heaviest possible traces.

Connect the VCL pin to a VSS pin via a 4.7 μF capacitor. The capacitor must be placed close to the pin. For details, refer to section 5.15.1, Connecting VCL Capacitor and Bypass Capacitors.

Do not input signals or an I/O pull-up power supply to ports other than 5-V tolerant ports while the device is not powered.

The current injection that results from input of such a signal or I/O pull-up may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Even if -0.3 to +6.5 V is input to 5-V tolerant ports, it will not cause problems such as damage to the MCU.

Note 1. Ports 12, 13, 16, 17, 30, 31, 32, and B5 are 5 V tolerant.

Note 2. The upper limit of operating temperature is 85°C or 105°C, depending on the product. For details, refer to section 1.2, List of Products.

Table 5.2 Recommended Operating Voltage Conditions

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Power supply voltages	VCC*1, *2	When USB is not used	1.8	—	5.5	V
		When USB is used When USB regulator is not used	3.0	—	3.6	
		When USB is used When USB regulator is used	4.0	—	5.5	
	VSS	—	0	—		
USB power supply voltages	VCC_USB	When USB regulator is not used	—	VCC	—	V
	VSS_USB		—	0	—	
VBATT power supply voltage	VBATT		1.8	—	5.5	V
Analog power supply voltages	AVCC0*1, *2		1.8	—	5.5	V
	AVSS0		—	0	—	
	VREFH0		1.8	—	AVCC0	
	VREFL0		—	0	—	
	VREFH		1.8	—	AVCC0	
	VREFL		—	0	—	

Note 1. Use AVCC0 and VCC under the following conditions:

AVCC0 and VCC can be set individually within the operating range when $VCC \geq 2.0$ V

AVCC0 = VCC when $VCC < 2.0$ V

Note 2. When powering on the VCC and AVCC0 pins, power them on at the same time or the VCC pin first and then the AVCC0 pin.

5.2 DC Characteristics

Table 5.3 DC Characteristics (1)Conditions: $2.7\text{ V} \leq \text{VCC} = \text{VCC_USB} \leq 5.5\text{ V}$, $2.7\text{ V} \leq \text{AVCC0} \leq 5.5\text{ V}$, $\text{VSS} = \text{AVSS0} = \text{VSS_USB} = 0\text{ V}$, $T_a = -40\text{ to }+105^\circ\text{C}$

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions	
Schmitt trigger input voltage	RIIC input pin (except for SMBus, 5 V tolerant)	V_{IH}	$\text{VCC} \times 0.7$	—	5.8	V		
	Ports 12, 13, 16, 17, port B5 (5 V tolerant)		$\text{VCC} \times 0.8$	—	5.8			
	Ports 14 to 15, ports 20 to 27, ports 33 to 37, ports 50 to 55, ports A0 to A7, ports B0 to B4, B6, B7, ports C0 to C7, ports D0 to D7, ports E0 to E7, port J3, Ports 30 to 32 (when time capture event input is not selected), RES		$\text{VCC} \times 0.8$	—	$\text{VCC} + 0.3$			
	Ports 03, 05, 07, ports 40 to 47		$\text{AVCC0} \times 0.8$	—	$\text{AVCC0} + 0.3$			
	Ports 30 to 32 (when time capture event input is selected)		When VCC is supplied	$\text{VCC} \times 0.8$	—			$\text{VCC} + 0.3$
			When VBATT is supplied	$\text{VBATT} \times 0.8$	—			$\text{VBATT} + 0.3$
	Ports 03, 05, 07, ports 40 to 47	V_{IL}	-0.3	—	$\text{AVCC0} \times 0.2$			
	RIIC input pin (except for SMBus)		-0.3	—	$\text{VCC} \times 0.3$			
	Other than RIIC input pin or ports 30 to 32		-0.3	—	$\text{VCC} \times 0.2$			
	Ports 30 to 32 (when time capture event input is selected)		When VCC is supplied	-0.3	—	$\text{VCC} \times 0.3$		
			When VBATT is supplied	-0.3	—	$\text{VBATT} \times 0.3$		
	Ports 03, 05, 07, ports 40 to 47		ΔV_T	$\text{AVCC0} \times 0.1$	—	—		
RIIC input pin (except for SMBus)	$\text{VCC} \times 0.05$	—		—				
Ports 12, 13, 16, 17, Port B5	$\text{VCC} \times 0.05$	—		—				
Other than RIIC input pin	$\text{VCC} \times 0.1$	—		—				
Input level voltage (except for Schmitt trigger input pins)	MD	V_{IH}	$\text{VCC} \times 0.9$	—	$\text{VCC} + 0.3$	V		
	EXTAL (external clock input)		$\text{VCC} \times 0.8$	—	$\text{VCC} + 0.3$			
	RIIC input pin (SMBus)		2.1	—	$\text{VCC} + 0.3$			
	MD	V_{IL}	-0.3	—	$\text{VCC} \times 0.1$			
	EXTAL (external clock input)		-0.3	—	$\text{VCC} \times 0.2$			
	RIIC input pin (SMBus)		-0.3	—	0.8			

Table 5.4 DC Characteristics (2)Conditions: $1.8\text{ V} \leq V_{CC} = V_{CC_USB} < 2.7\text{ V}$, $1.8\text{ V} \leq AV_{CC0} < 2.7\text{ V}$, $V_{SS} = AV_{SS0} = V_{SS_USB} = 0\text{ V}$, $T_a = -40$ to $+105^\circ\text{C}$

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Schmitt trigger input voltage	Ports 12, 13, 16, 17, port B5 (5 V tolerant)	V_{IH}	$V_{CC} \times 0.8$	—	5.8	V	
	Ports 14 to 15, ports 20 to 27, ports 30 to 37, ports 50 to 55, ports A0 to A7, ports B0 to B4, B6, B7, ports C0 to C7, ports D0 to D7, ports E0 to E7, port J3, RES		$V_{CC} \times 0.8$	—	$V_{CC} + 0.3$		
	Ports 03, 05, 07, ports 40 to 47		$AV_{CC0} \times 0.8$	—	$AV_{CC0} + 0.3$		
	Ports 03, 05, 07, ports 40 to 47	V_{IL}	-0.3	—	$AV_{CC0} \times 0.2$		
	Ports other than above		-0.3	—	$V_{CC} \times 0.2$		
	Ports 03, 05, 07, ports 40 to 47	ΔV_T	$AV_{CC0} \times 0.01$	—	—		
	Ports other than above		$V_{CC} \times 0.01$	—	—		
Input level voltage (except for Schmitt trigger input pins)	MD	V_{IH}	$V_{CC} \times 0.9$	—	$V_{CC} + 0.3$	V	
	EXTAL (external clock input)		$V_{CC} \times 0.8$	—	$V_{CC} + 0.3$		
	MD	V_{IL}	-0.3	—	$V_{CC} \times 0.1$		
	EXTAL (external clock input)		-0.3	—	$V_{CC} \times 0.2$		

Table 5.5 DC Characteristics (3)Conditions: $1.8\text{ V} \leq V_{CC} = V_{CC_USB} = AV_{CC0} \leq 5.5\text{ V}$, $V_{SS} = AV_{SS0} = V_{SS_USB} = 0\text{ V}$, $T_a = -40$ to $+105^\circ\text{C}$

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Input leakage current	RES#, MD, port 35	$ I_{in} $	—	—	1.0	μA	$V_{in} = 0\text{ V}$, VCC
Three-state leakage current (off-state)	Ports for 5 V tolerant	$ I_{TSI} $	—	—	1.0	μA	$V_{in} = 0\text{ V}$, 5.8V
	Ports except for 5 V tolerant		—	—	0.2	μA	$V_{in} = 0\text{ V}$, VCC
Input capacitance	All input pins (except for port 35, USB0_DM, USB0_DP)	C_{in}	—	—	15	pF	$V_{in} = 0\text{ mV}$, $f = 1\text{ MHz}$, $T_a = 25^\circ\text{C}$
	Port 35, USB0_DM, USB0_DP		—	—	30		

Table 5.6 DC Characteristics (4)Conditions: $1.8\text{ V} \leq V_{CC} = V_{CC_USB} = AV_{CC0} \leq 5.5\text{ V}$, $V_{SS} = AV_{SS0} = V_{SS_USB} = 0\text{ V}$, $T_a = -40$ to $+105^\circ\text{C}$

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Input pull-up resistor	All ports (except for port 35)	R_U	10	20	50	k Ω	$V_{in} = 0\text{ V}$

Table 5.7 DC Characteristics (5)

Conditions: 1.8 V ≤ VCC = VCC_USB = AVCC0 ≤ 5.5 V, VSS = AVSS0 = VSS_USB = 0 V, T_a = -40 to +105°C

Item					Symbol	Typ. *4	Max.	Unit	Test Conditions
Supply current *1	High-speed operating mode	Normal operating mode	No peripheral operation*2	ICLK = 54 MHz	I _{CC}	6.5	—	mA	
				ICLK = 32 MHz		4.1	—		
				ICLK = 16 MHz		2.9	—		
				ICLK = 8 MHz		2.2	—		
				ICLK = 4 MHz		1.9	—		
			All peripheral operation: Normal	ICLK = 54 MHz*11		26.5	—		
				ICLK = 32 MHz*3		21.0	—		
				ICLK = 16 MHz*3		11.8	—		
				ICLK = 8 MHz*3		6.6	—		
				ICLK = 4 MHz*3		4.2	—		
		All peripheral operation: Max.	ICLK = 54 MHz*11	—	53.3				
			ICLK = 32 MHz*3	—	40.8				
		Increase during security function operation	PCLKB = 32 MHz	—	2				
		Sleep mode	No peripheral operation*2	ICLK = 54 MHz	3.5	—			
				ICLK = 32 MHz	2.4	—			
				ICLK = 16 MHz	1.9	—			
				ICLK = 8 MHz	1.6	—			
				ICLK = 4 MHz	1.5	—			
			All peripheral operation: Normal	ICLK = 54 MHz*11	13.4	—			
				ICLK = 32 MHz*3	12.5	—			
	ICLK = 16 MHz*3			7.3	—				
	ICLK = 8 MHz*3			4.6	—				
	ICLK = 4 MHz*3			3.3	—				
	Deep sleep mode	No peripheral operation*2	ICLK = 54 MHz	2.3	—				
			ICLK = 32 MHz	1.5	—				
			ICLK = 16 MHz	1.3	—				
			ICLK = 8 MHz	1.2	—				
			ICLK = 4 MHz	1.1	—				
		All peripheral operation: Normal	ICLK = 54 MHz*11	10.6	—				
			ICLK = 32 MHz*3	9.9	—				
			ICLK = 16 MHz*3	5.9	—				
			ICLK = 8 MHz*3	3.8	—				
ICLK = 4 MHz*3			2.7	—					
Increase during BGO operation*5		2.5	—						
Middle-speed operating mode	Normal operating mode	No peripheral operation*6	ICLK = 12 MHz	I _{CC}	2.7	—	mA		
			ICLK = 8 MHz		1.8	—			
			ICLK = 4 MHz		1.4	—			
			ICLK = 1 MHz		1.1	—			
			ICLK = 1 MHz		1.1	—			
		All peripheral operation: Normal*7	ICLK = 12 MHz		9.6	—			
			ICLK = 8 MHz		6.2	—			
			ICLK = 4 MHz		3.8	—			
			ICLK = 4 MHz		3.8	—			
			ICLK = 1 MHz		2.3	—			

Item					Symbol	Typ. *4	Max.	Unit	Test Conditions		
Supply current	Middle-speed operating mode	Normal operating mode	All peripheral operation: Max.*7	ICLK = 12 MHz	I _{CC}	—	16.7	mA			
				Sleep mode		No peripheral operation*6	ICLK = 12 MHz			1.9	—
							ICLK = 8 MHz			1.2	—
							ICLK = 4 MHz			1.1	—
		ICLK = 1 MHz	1.0				—				
		All peripheral operation: Normal*7		ICLK = 12 MHz		6.1	—				
				ICLK = 8 MHz		4.4	—				
				ICLK = 4 MHz		3.0	—				
				ICLK = 1 MHz		2.0	—				
		Deep sleep mode	No peripheral operation*6			ICLK = 12 MHz	1.6			—	
						ICLK = 8 MHz	1.0			—	
						ICLK = 4 MHz	0.9			—	
						ICLK = 1 MHz	0.8			—	
			All peripheral operation: Normal*7			ICLK = 12 MHz	5.1			—	
						ICLK = 8 MHz	3.7			—	
						ICLK = 4 MHz	2.6			—	
	ICLK = 1 MHz				1.8	—					
	Increase during BGO operation*5					2.5	—				
	Low-speed operating mode	Normal operating mode	No peripheral operation*8	ICLK = 32 kHz	I _{CC}	5.2	—	μA			
						All peripheral operation: Normal *9, *10	ICLK = 32 kHz			22.3	—
All peripheral operation: Max.*9, *10									ICLK = 32 kHz	—	74.4
		Sleep mode	No peripheral operation*8	ICLK = 32 kHz		3.0	—				
All peripheral operation: Normal*9						ICLK = 32 kHz	13.1		—		
		Deep sleep mode	No peripheral operation*8	ICLK = 32 kHz			2.4		—		
All peripheral operation: Normal*9						ICLK = 32 kHz	10.5		—		

- Note 1. Supply current values do not include the output charge/discharge current from all pins. The values apply when internal pull-up MOSs are in the off state.
- Note 2. Clock supply to the peripheral functions is stopped. This does not include BGO operation. The clock source is PLL. BCLK, FCLK, and PCLK are set to divided by 64.
- Note 3. Clocks are supplied to the peripheral functions. This does not include BGO operation. The clock source is PLL. BCLK, FCLK, and PCLK are the same frequency as that of ICLK.
- Note 4. Values when VCC is 3.3 V.
- Note 5. This is the increase when data is programmed to or erased from the ROM or E2 DataFlash during program execution.
- Note 6. Clock supply to the peripheral functions is stopped. The clock source is PLL when ICLK is 12 MHz and HOCO for other cases. BCLK, FCLK, and PCLK are set to divided by 64.
- Note 7. Clocks are supplied to the peripheral functions. The clock source is PLL when ICLK is 12 MHz and HOCO for other cases. BCLK, FCLK, and PCLK are the same frequency of that of the ICLK.
- Note 8. Clock supply to the peripheral functions is stopped. The clock source is the sub oscillation circuit. BCLK, FCLK, and PCLK are set to divided by 64.
- Note 9. Clocks are supplied to the peripheral functions. The clock source is the sub oscillation circuit. BCLK, FCLK, and PCLK are the same frequency as that of ICLK.
- Note 10. This is the value when the MSTPCRA.MSTPA17 (12-bit A/D converter module stop bit) is in the module stop state.
- Note 11. Clocks are supplied to the peripheral functions. This does not include BGO operation. The clock source is PLL. BCLK, FCLK, and PCLKB are set to divided by 2 and PCLKA and PCLKD are the same frequency as that of ICLK.

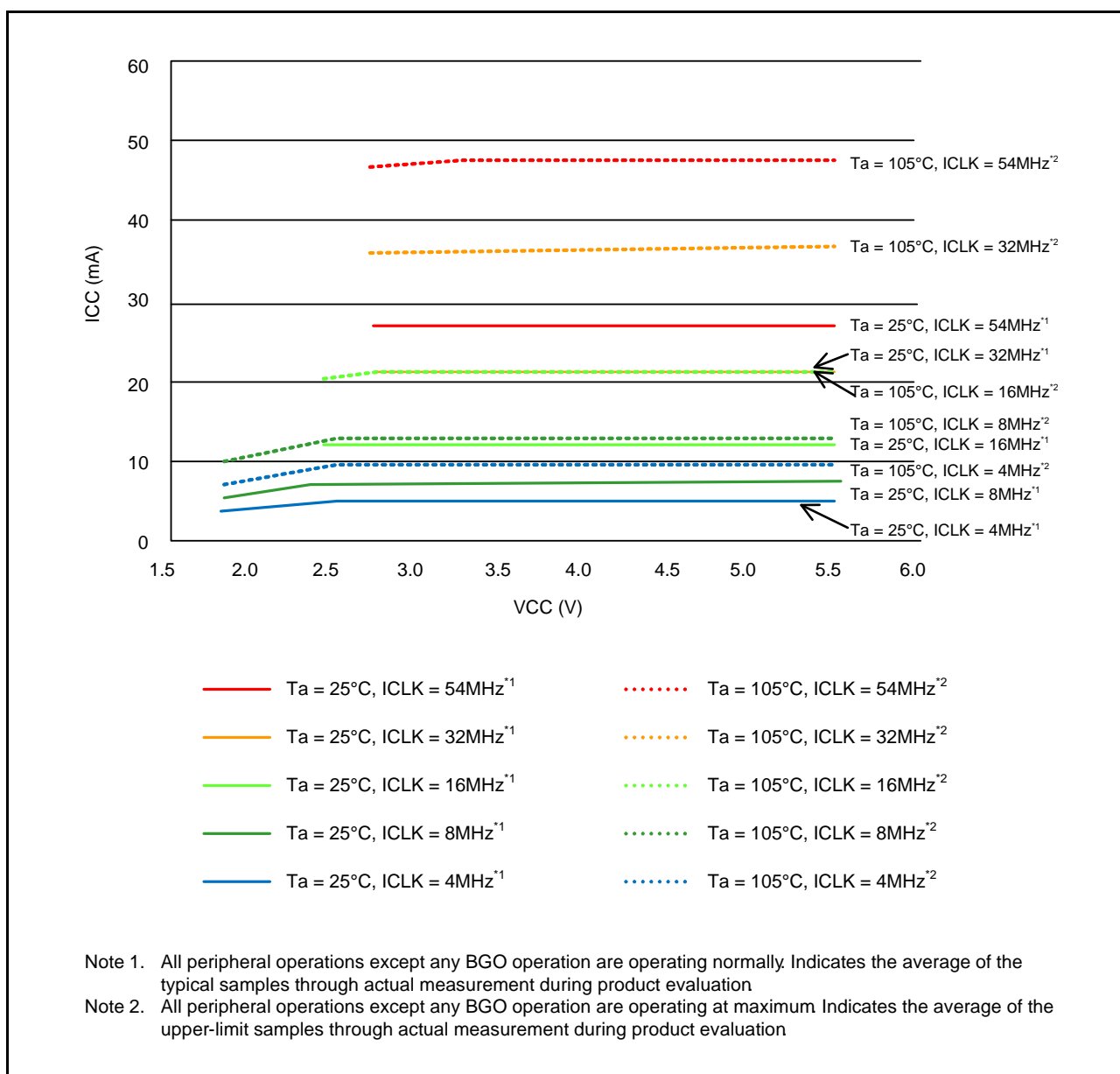


Figure 5.1 Voltage Dependency in High-Speed Operating Mode (Reference Data)

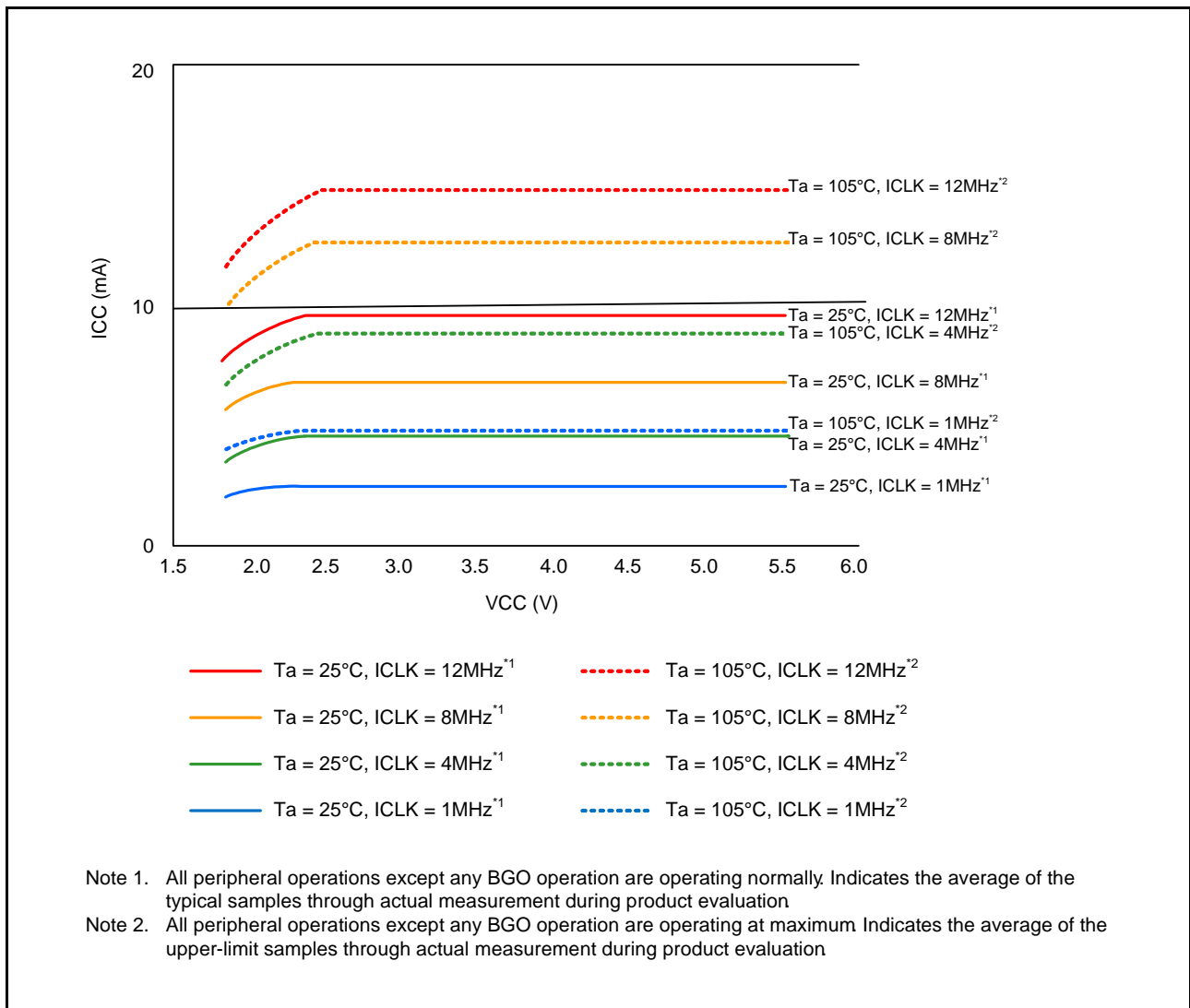


Figure 5.2 Voltage Dependency in Middle-Speed Operating Mode (Reference Data)

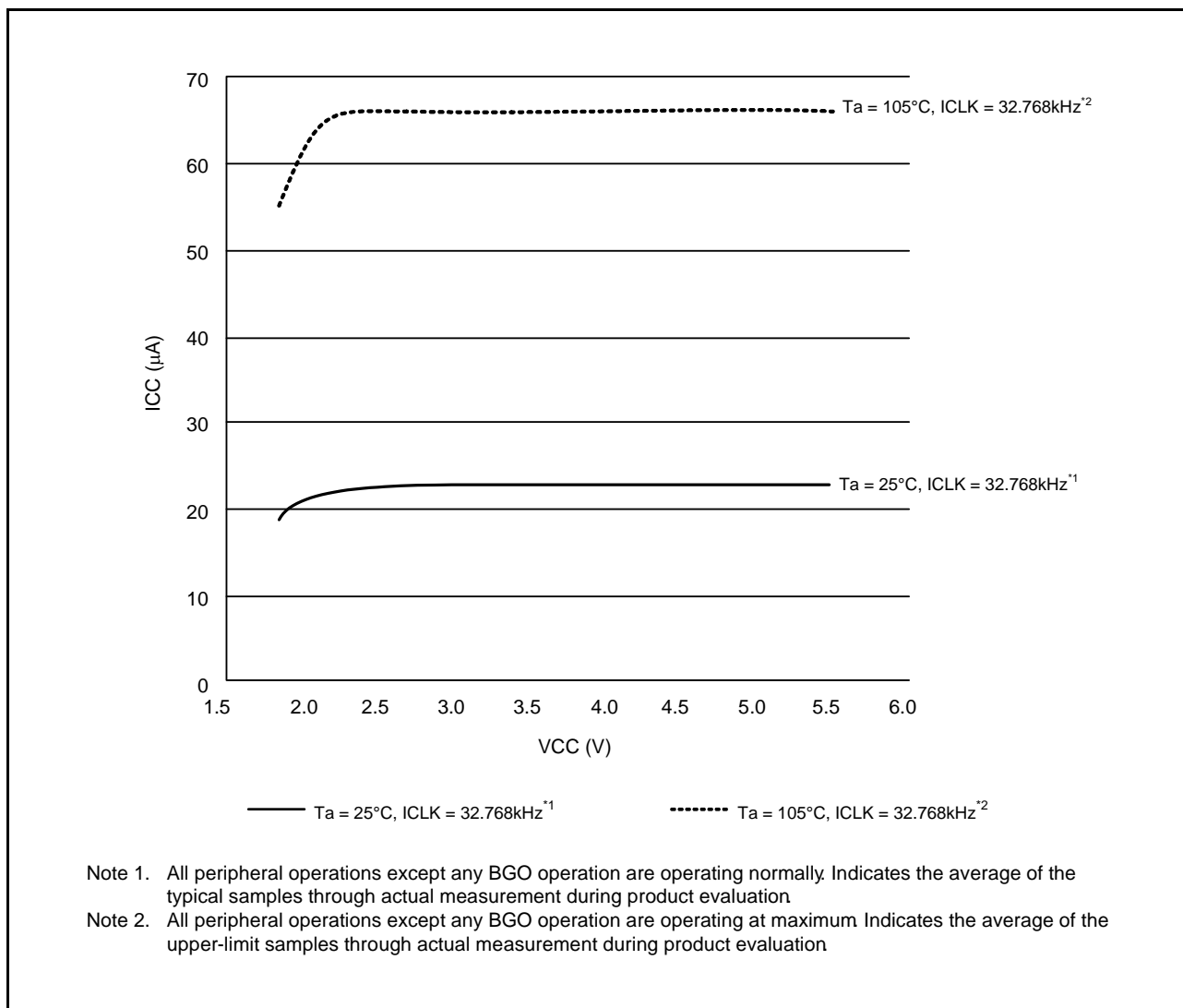


Figure 5.3 Voltage Dependency in Low-Speed Operating Mode (Reference Data)

Table 5.8 DC Characteristics (6)

Conditions: $1.8\text{ V} \leq VCC = VCC_USB = AVCC0 \leq 5.5\text{ V}$, $VSS = AVSS0 = VSS_USB = 0\text{ V}$, $T_a = -40\text{ to }+105^\circ\text{C}$

Item		Symbol	Typ.*3	Max.	Unit	Test Conditions		
Supply current*1	Software standby mode*2	I_{CC}	$T_a = 25^\circ\text{C}$	0.8	3.7	μA		
			$T_a = 55^\circ\text{C}$	1.2	4.3			
			$T_a = 85^\circ\text{C}$	3.5	18.6			
			$T_a = 105^\circ\text{C}$	7.9	45.2			
	Increment for IWDT operation			0.4	—			
	Increment for LPT operation			0.4	—			
	Increment for RTC operation*4			0.4	—			
						Use IWDT-Dedicated On-Chip Oscillator for clock source		
						RCR3.RTCDV[2:0] set to low drive capacity		
						RCR3.RTCDV[2:0] set to normal drive capacity		

Note 1. Supply current values are with all output pins unloaded and all input pull-up MOSs in the off state.

Note 2. The IWDT, LVD, and CMPB are stopped.

Note 3. When VCC is 3.3 V.

Note 4. This increment includes the oscillation circuit.

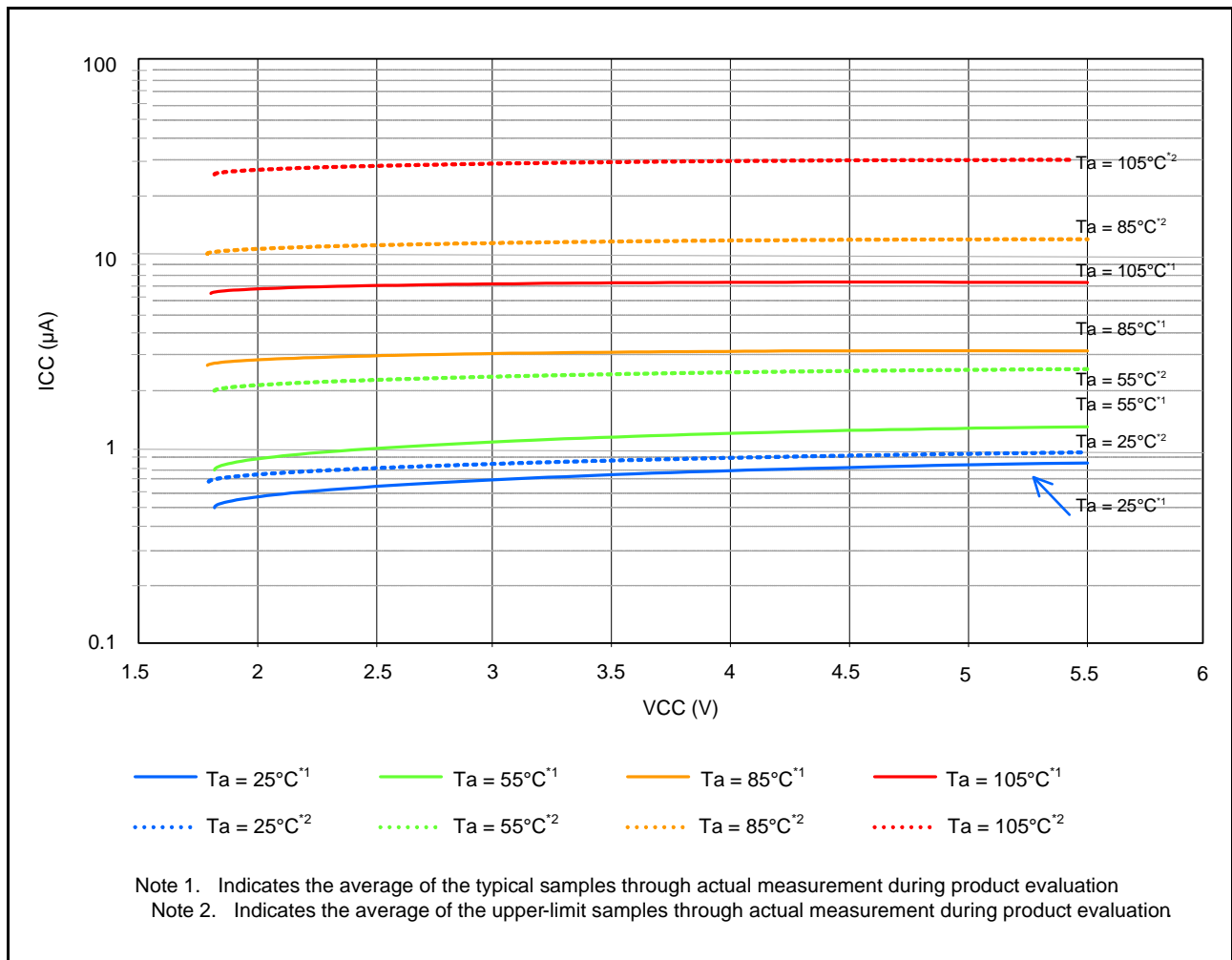


Figure 5.4 Voltage Dependency in Software Standby Mode (Reference Data)

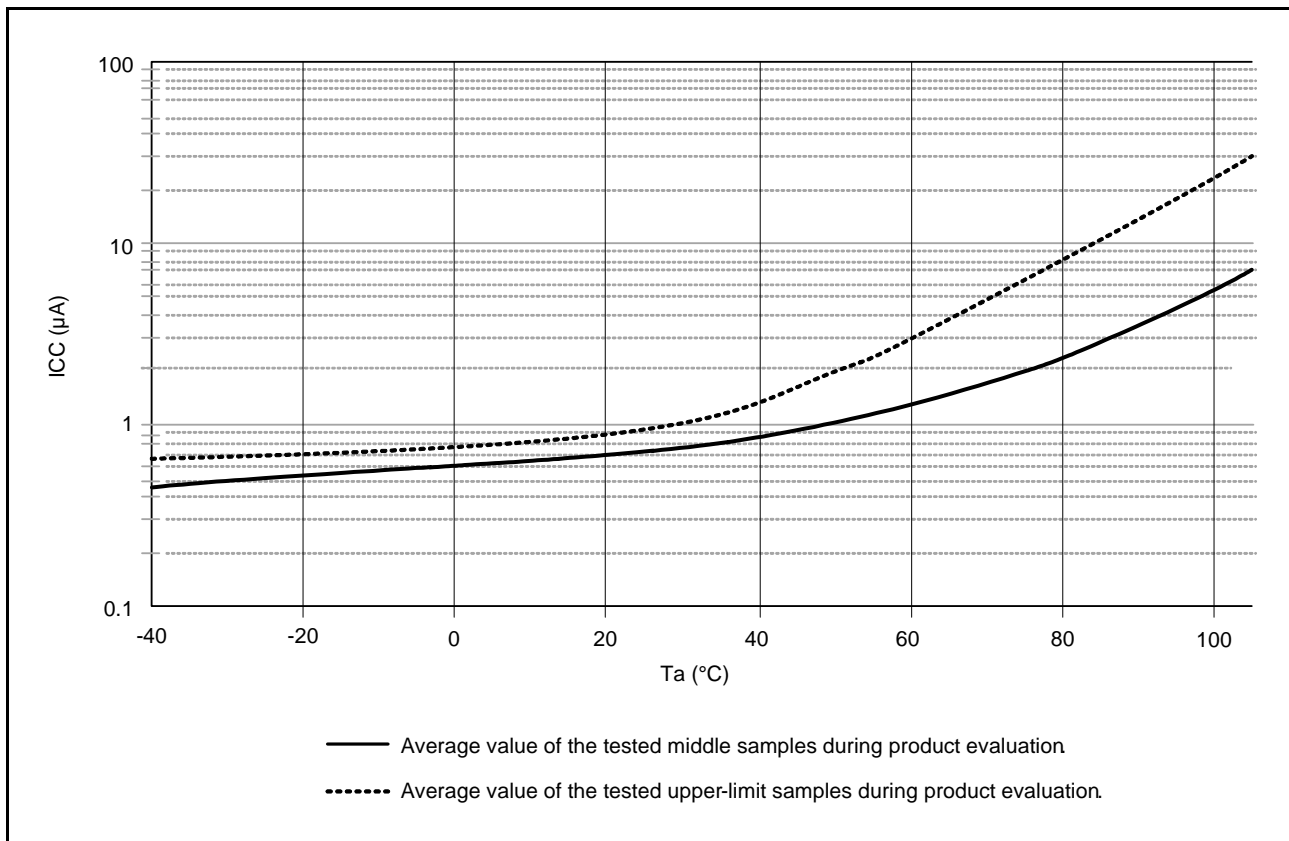


Figure 5.5 Temperature Dependency in Software Standby Mode (Reference Data)

Table 5.9 DC Characteristics (7)

Conditions: 1.8 V ≤ VCC = VCC_USB = AVCC0 ≤ 5.5 V, VSS = AVSS0 = VSS_USB = 0 V, Ta = -40 to +105°C

Item	Symbol	Typ.	Max.	Unit	Test Conditions	
Supply current*1 RTC operation when VCC is off	I _{CC}	T _a = 25°C	0.8	—	µA	VBATT = 2.0 V RCR3.RTCDV[2:0] set to low drive capacity
		T _a = 55°C	0.9	—		
		T _a = 85°C	1.0	—		
		T _a = 105°C	1.2	—		
		T _a = 25°C	0.9	—		VBATT = 3.3 V RCR3.RTCDV[2:0] set to low drive capacity
		T _a = 55°C	1.0	—		
		T _a = 85°C	1.1	—		
		T _a = 105°C	1.3	—		
		T _a = 25°C	1.5	—		VBATT = 2.0 V RCR3.RTCDV[2:0] set to normal drive capacity
		T _a = 55°C	1.8	—		
		T _a = 85°C	2.1	—		
		T _a = 105°C	2.4	—		
		T _a = 25°C	1.6	—		VBATT = 3.3 V RCR3.RTCDV[2:0] set to normal drive capacity
		T _a = 55°C	1.9	—		
		T _a = 85°C	2.2	—		
		T _a = 105°C	2.5	—		

Note 1. Supply current values do not include output charge/discharge current from all pins. The values apply when internal pull-up MOSs are in the off state.

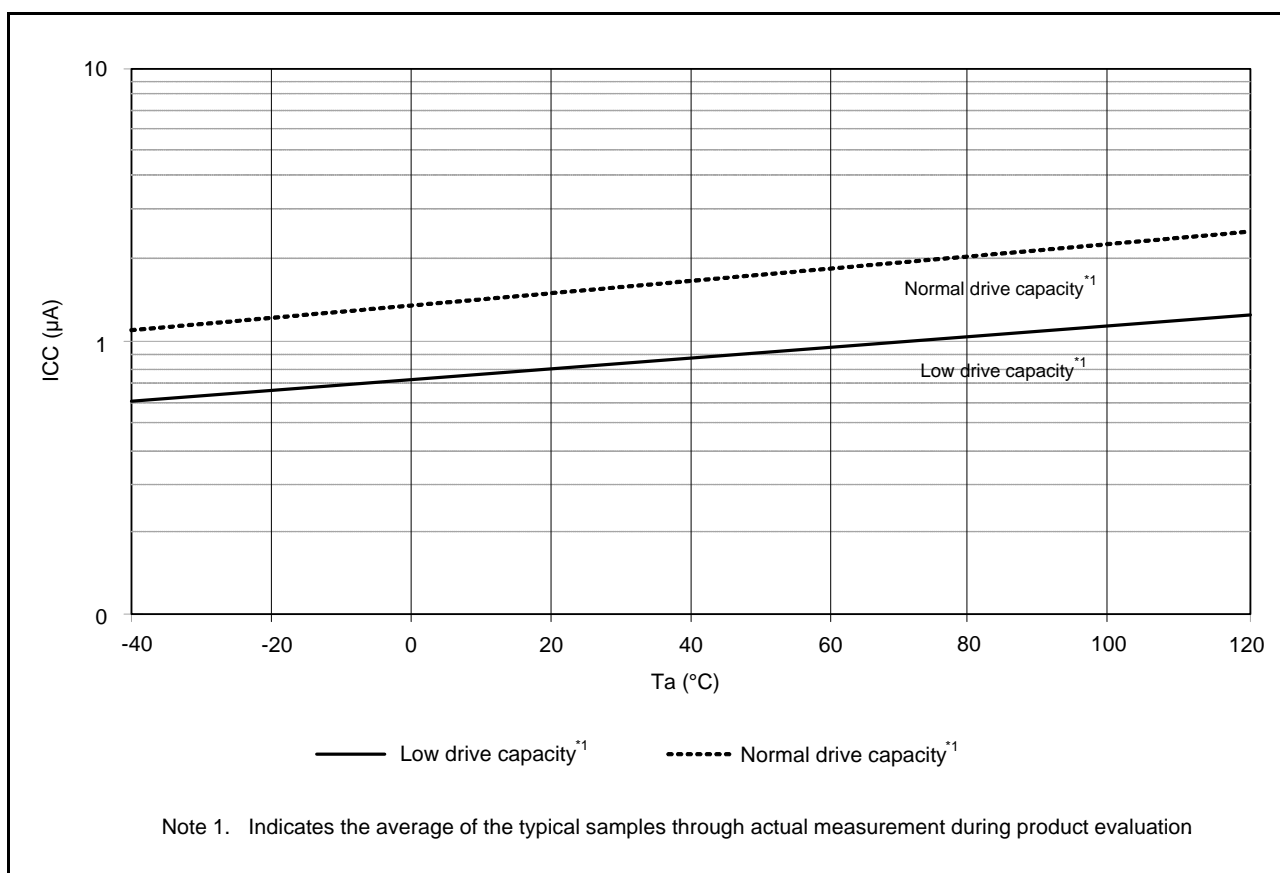


Figure 5.6 Temperature Dependency of RTC Operation with VCC Off (Reference Data)

Table 5.10 DC Characteristics (8)

Conditions: 1.8 V ≤ VCC = VCC_USB = AVCC0 ≤ 5.5 V, VSS = AVSS0 = VSS_USB = 0 V

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Permissible total power consumption ^{*1}	Pd	—	—	350	mW	D-version product
Permissible total power consumption ^{*1}	Pd	—	—	130	mW	G-version product

Note: Please contact a Renesas Electronics sales office for information on the derating of the G-version product. Derating is the systematic reduction of load to improve reliability.

Note 1. Total power dissipated by the entire chip (including output currents)

Table 5.11 DC Characteristics (9)Conditions: $1.8\text{ V} \leq VCC = VCC_USB = AVCC0 \leq 5.5\text{ V}$, $VSS = AVSS0 = VSS_USB = 0\text{ V}$, $T_a = -40\text{ to }+105^\circ\text{C}$

Item	Symbol	Min.	Typ.*7	Max.	Unit	Test Conditions
Analog power supply current	During A/D conversion (at high-speed conversion)	—	0.7	1.7	mA	
	During A/D conversion (in low-current mode)	—	0.6	1.0		
	During D/A conversion (per channel)*1	—	0.4	0.8		
	Waiting for A/D and D/A conversion (all units)	—	—	0.4	μA	
Reference power supply current	During A/D conversion (at high-speed conversion)	—	25	150	μA	
	Waiting for A/D conversion (all units)	—	—	60	nA	
	During D/A conversion (per channel)	—	50	100	μA	
	Waiting for D/A conversion (all units)	—	—	100	nA	
LVD1, 2	per channel	I_{LVD}	—	0.15	—	μA
Temperature sensor*6	—	I_{TEMP}	—	75	—	μA
Comparator B operating current*6	Window mode	I_{CMP}^{*5}	—	12.5	28.6	μA
	Comparator high-speed mode (per channel)		—	3.2	16.2	μA
	Comparator low-speed mode (per channel)		—	1.7	4.4	μA
CTSU operating current	When sleep mode Base clock frequency: 2MHz Pin capacitance: 50pF	I_{CTSU}	—	150	—	μA
USB operating current*4	During USB communication operation under the following settings and conditions <ul style="list-style-type: none"> Host controller operation is set to full-speed mode Bulk OUT transfer (64 bytes) \times 1, bulk IN transfer (64 bytes) \times 1 Connect peripheral devices via a 1-meter USB cable from the USB port. 	I_{USBH}^{*2}	—	4.3 (VCC) 0.9 (VCC_USB)	—	mA
	During USB communication operation under the following settings and conditions <ul style="list-style-type: none"> Function controller operation is set to full-speed mode Bulk OUT transfer (64 bytes) \times 1, bulk IN transfer (64 bytes) \times 1 Connect the host device via a 1-meter USB cable from the USB port. 	I_{USBF}^{*2}	—	3.6 (VCC) 1.1 (VCC_USB)	—	mA
	During suspended state under the following setting and conditions <ul style="list-style-type: none"> Function controller operation is set to full-speed mode (pull up the USB0_DP pin) Software standby mode Connect the host device via a 1-meter USB cable from the USB port. 	I_{SUSP}^{*3}	—	0.35 (VCC) 170 (VCC_USB)	—	μA

Note 1. The value of the D/A converter is the value of the power supply current including the reference current.

Note 2. Current consumed only by the USB module.

Note 3. Includes the current supplied from the pull-up resistor of the USB0_DP pin to the pull-down resistor of the host device, in addition to the current consumed by this MCU during the suspended state.

Note 4. Current consumed by the power supplies (VCC and VCC_USB).

Note 5. Current consumed only by the comparator B module.

Note 6. Current consumed by the power supply (VCC).

Note 7. When $VCC = AVCC0 = VCC_USB = 3.3\text{ V}$.**Table 5.12 DC Characteristics (10)**Conditions: $1.8\text{ V} \leq VCC = VCC_USB = AVCC0 \leq 5.5\text{ V}$, $VSS = AVSS0 = VSS_USB = 0\text{ V}$, $T_a = -40\text{ to }+105^\circ\text{C}$

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
RAM standby voltage	V_{RAM}	1.8	—	—	V	

Table 5.13 DC Characteristics (11)

Conditions: $0\text{ V} \leq \text{VCC} = \text{VCC_USB} = \text{AVCC0} \leq 5.5\text{ V}$, $\text{VSS} = \text{AVSS0} = \text{VSS_USB} = 0\text{ V}$, $T_a = -40\text{ to }+105^\circ\text{C}$

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Power-on VCC rising gradient	At normal startup*1	0.02	—	20	ms/V	
	During fast startup time*2	0.02	—	2		
	Voltage monitoring 0 reset enabled at startup*3, *4	0.02	—	—		

Note 1. When OFS1.(FASTSTUP, LVDAS) bits are 11b.

Note 2. When OFS1.(FASTSTUP, LVDAS) bits are 01b.

Note 3. When OFS1.LVDAS bit is 0.

Note 4. Turn on the power supply voltage according to the normal startup rising gradient because the settings in the OFS1 register are not read in boot mode.

Table 5.14 DC Characteristics (12)

Conditions: $1.8\text{ V} \leq \text{VCC} = \text{VCC_USB} = \text{AVCC0} \leq 5.5\text{ V}$, $\text{VSS} = \text{AVSS0} = \text{VSS_USB} = 0\text{ V}$, $T_a = -40\text{ to }+105^\circ\text{C}$

The ripple voltage must meet the allowable ripple frequency $f_r(\text{VCC})$ within the range between the VCC upper limit and lower limit. When VCC change exceeds $\text{VCC} \pm 10\%$, the allowable voltage change rising/falling gradient $dt/d\text{VCC}$ must be met.

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Allowable ripple frequency	$f_r(\text{VCC})$	—	—	10	kHz	Figure 5.7 $V_r(\text{VCC}) \leq \text{VCC} \times 0.2$
		—	—	1	MHz	Figure 5.7 $V_r(\text{VCC}) \leq \text{VCC} \times 0.08$
		—	—	10	MHz	Figure 5.7 $V_r(\text{VCC}) \leq \text{VCC} \times 0.06$
Allowable voltage change rising/falling gradient	$dt/d\text{VCC}$	1.0	—	—	ms/V	When VCC change exceeds $\text{VCC} \pm 10\%$

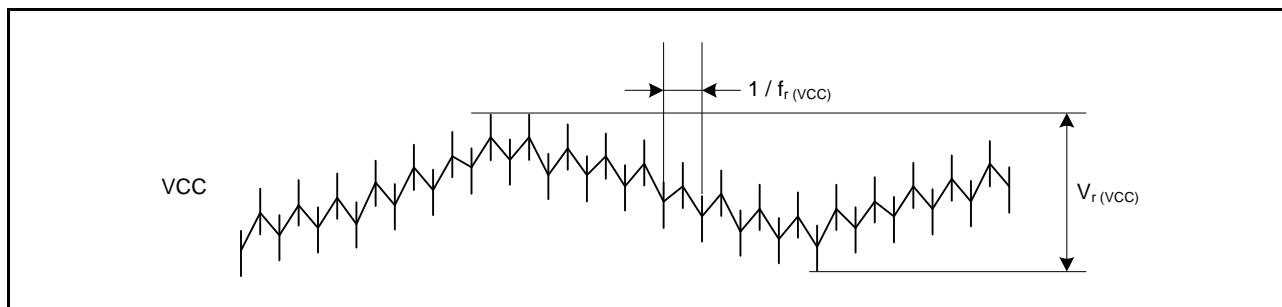


Figure 5.7 Ripple Waveform

Table 5.15 DC Characteristics (13)

Conditions: $1.8\text{ V} \leq \text{VCC} = \text{VCC_USB} = \text{AVCC0} \leq 5.5\text{ V}$, $\text{VSS} = \text{AVSS0} = \text{VSS_USB} = 0\text{ V}$, $T_a = -40\text{ to }+105^\circ\text{C}$

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Permissible error of VCL pin external capacitance	C_{VCL}	1.4	4.7	7.0	μF	

Note: The recommended capacitance is 4.7 μF . Variations in connected capacitors should be within the above range.

Table 5.16 Permissible Output Currents (1)Conditions: $1.8\text{ V} \leq VCC = VCC_USB = AVCC0 \leq 5.5\text{ V}$, $VSS = AVSS0 = VSS_USB = 0\text{ V}$, $T_a = -40\text{ to }+85^\circ\text{C}$

Item		Symbol	Max.	Unit	
Permissible output low current (average value per pin)	Ports 40 to 47, ports 03, 05, 07, port 36, 37	I_{OL}	4.0	mA	
	Ports other than above		Normal output mode		4.0
			High-drive output mode		8.0
Permissible output low current (maximum value per pin)	Ports 40 to 47, ports 03, 05, 07, ports 36, 37	I_{OL}	4.0		
	Ports other than above		Normal output mode		4.0
			High-drive output mode		8.0
Permissible output low current	Total of ports 40 to 47, ports 03, 05, 07	ΣI_{OL}	40		
	Total of ports 12 to 17, ports 20 to 27, ports 30 to 37, port PJ3		40		
	Total of ports 50 to 55, ports C0 to C7, ports B0 to B7		40		
	Total of ports E0 to E7, ports A0 to A7, ports D0 to D4		40		
	Total of all output pins		80		
Permissible output high current (average value per pin)	Ports 40 to 47, ports 03, 05, 07, ports 36, 37	I_{OH}	-4.0		
	Ports other than above		Normal output mode		-4.0
			High-drive output mode		-8.0
Permissible output high current (maximum value per pin)	Ports 40 to 47, ports 03, 05, 07, ports 36, 37	I_{OH}	-4.0		
	Ports other than above		Normal output mode		-4.0
			High-drive output mode		-8.0
Permissible output high current	Total of ports 40 to 47, ports 03, 05, 07	ΣI_{OH}	-40		
	Total of ports 12 to 17, ports 20 to 27, ports 30 to 37, port PJ3		-40		
	Total of ports 50 to 55, ports C0 to C7, ports B0 to B7		-40		
	Total of ports E0 to E7, ports A0 to A7, ports D0 to D4		-40		
	Total of all output pins		-80		

Note: Do not exceed the permissible total supply current.

Table 5.17 Permissible Output Currents (2)Conditions: $1.8\text{ V} \leq V_{CC} = V_{CC_USB} = AV_{CC0} \leq 5.5\text{ V}$, $V_{SS} = AV_{SS0} = V_{SS_USB} = 0\text{ V}$, $T_a = -40\text{ to }+105^\circ\text{C}$

Item		Symbol	Max.	Unit	
Permissible output low current (average value per pin)	Ports 40 to 47, ports 03, 05, 07, port 36, 37	I_{OL}	4.0	mA	
	Ports other than above		Normal output mode		4.0
			High-drive output mode		8.0
Permissible output low current (maximum value per pin)	Ports 40 to 47, ports 03, 05, 07, ports 36, 37		4.0		
	Ports other than above		Normal output mode		4.0
			High-drive output mode		8.0
Permissible output low current	Total of ports 40 to 47, ports 03, 05, 07	ΣI_{OL}	30		
	Total of ports 12 to 17, ports 20 to 27, ports 30 to 37, port PJ3		30		
	Total of ports 50 to 55, ports C0 to C7, ports B0 to B7		30		
	Total of ports E0 to E7, ports A0 to A7, ports D0 to D4		30		
	Total of all output pins		60		
Permissible output high current (average value per pin)	Ports 40 to 47, ports 03, 05, 07, ports 36, 37	I_{OH}	-4.0		
	Ports other than above		Normal output mode		-4.0
			High-drive output mode		-8.0
Permissible output high current (maximum value per pin)	Ports 40 to 47, ports 03, 05, 07, ports 36, 37		-4.0		
	Ports other than above		Normal output mode		-4.0
			High-drive output mode		-8.0
Permissible output high current	Total of ports 40 to 47, ports 03, 05, 07	ΣI_{OH}	-30		
	Total of ports 12 to 17, ports 20 to 27, ports 30 to 37, port PJ3		-30		
	Total of ports 50 to 55, ports C0 to C7, ports B0 to B7		-30		
	Total of ports E0 to E7, ports A0 to A7, ports D0 to D4		-30		
	Total of all output pins		-60		

Note: Do not exceed the permissible total supply current.

Table 5.18 Output Values of Voltage (1)

Conditions: $1.8\text{ V} \leq VCC = VCC_USB = AVCC0 < 2.7\text{ V}$, $VSS = AVSS0 = VSS_USB = 0\text{ V}$, $T_a = -40\text{ to }+105^\circ\text{C}$

Item		Symbol	Min.	Max.	Unit	Test Conditions	
Output low	All output ports	Normal output mode	—	0.8	V	$I_{OL} = 0.5\text{ mA}$	
		High-drive output mode		0.8		$I_{OL} = 1.0\text{ mA}$	
Output high	All output ports	Normal output mode	Ports 03, 05, 07, Ports 40 to 47	$AVCC0 - 0.5$	—	V	$I_{OH} = -0.5\text{ mA}$
				$VCC - 0.5$			
		High-drive output mode	$VCC - 0.5$	—	$I_{OH} = -1.0\text{ mA}$		

Table 5.19 Output Values of Voltage (2)

Conditions: $2.7\text{ V} \leq VCC = VCC_USB = AVCC0 < 4.0\text{ V}$, $VSS = AVSS0 = VSS_USB = 0\text{ V}$, $T_a = -40\text{ to }+105^\circ\text{C}$

Item		Symbol	Min.	Max.	Unit	Test Conditions	
Output low	All output ports (except for RIIC)	Normal output mode	—	0.8	V	$I_{OL} = 1.0\text{ mA}$	
		High-drive output mode		0.8		$I_{OL} = 2.0\text{ mA}$	
	RIIC pins	Standard mode (Normal output mode)		0.4		$I_{OL} = 3.0\text{ mA}$	
		Fast mode (High-drive output mode)		0.6		$I_{OL} = 6.0\text{ mA}$	
Output high	All output ports	Normal output mode	Ports 03, 05, 07, Ports 40 to 47	$AVCC0 - 0.8$	—	V	$I_{OH} = -1.0\text{ mA}$
				$VCC - 0.8$			
		High-drive output mode	$VCC - 0.8$	—	$I_{OH} = -2.0\text{ mA}$		

Table 5.20 Output Values of Voltage (3)

Conditions: $4.0\text{ V} \leq VCC = VCC_USB = AVCC0 \leq 5.5\text{ V}$, $VSS = AVSS0 = VSS_USB = 0\text{ V}$, $T_a = -40\text{ to }+105^\circ\text{C}$

Item		Symbol	Min.	Max.	Unit	Test Conditions	
Output low	All output ports (except for RIIC)	Normal output mode	—	0.8	V	$I_{OL} = 2.0\text{ mA}$	
		High-drive output mode		0.8		$I_{OL} = 4.0\text{ mA}$	
	RIIC pins	Standard mode (Normal output mode)		0.4		$I_{OL} = 3.0\text{ mA}$	
		Fast mode (High-drive output mode)		0.6		$I_{OL} = 6.0\text{ mA}$	
Output high	All output ports	Normal output mode	Ports 03, 05, 07, Ports 40 to 47	$AVCC0 - 0.8$	—	V	$I_{OH} = -2.0\text{ mA}$
				$VCC - 0.8$			
		High-drive output mode	$VCC - 0.8$	—	$I_{OH} = -4.0\text{ mA}$		

5.2.1 Normal I/O Pin Output Characteristics (1)

Figure 5.8 to Figure 5.12 show the characteristics when normal output is selected by the drive capacity control register.

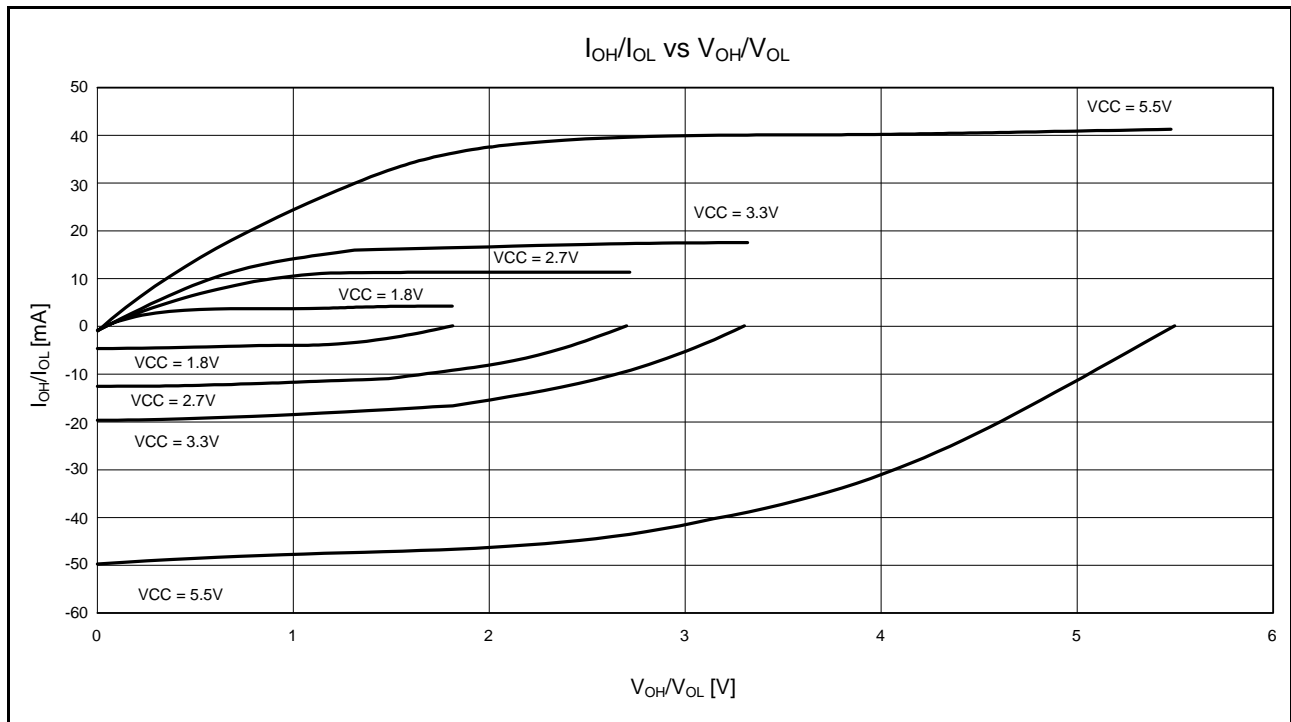


Figure 5.8 V_{OH}/V_{OL} and I_{OH}/I_{OL} Voltage Characteristics at $T_a = 25^\circ\text{C}$ When Normal Output is Selected (Reference Data)

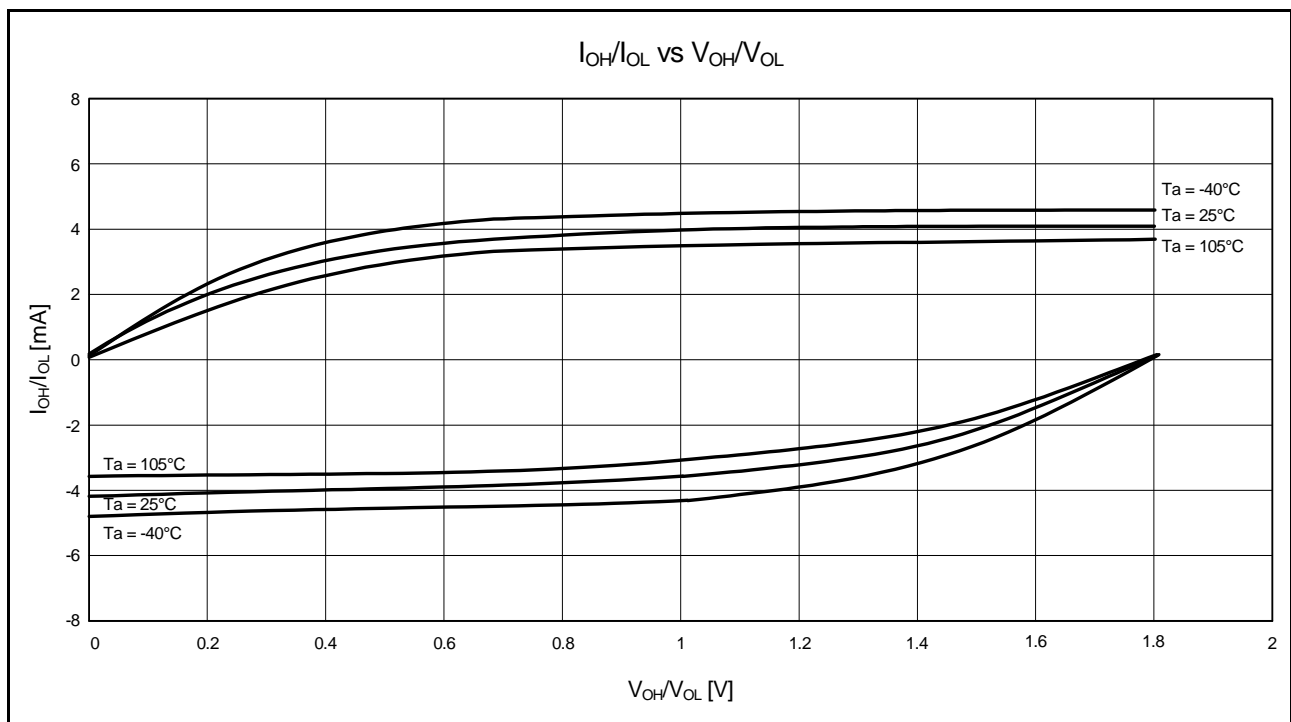


Figure 5.9 V_{OH}/V_{OL} and I_{OH}/I_{OL} Temperature Characteristics at $V_{CC} = 1.8\text{ V}$ When Normal Output is Selected (Reference Data)

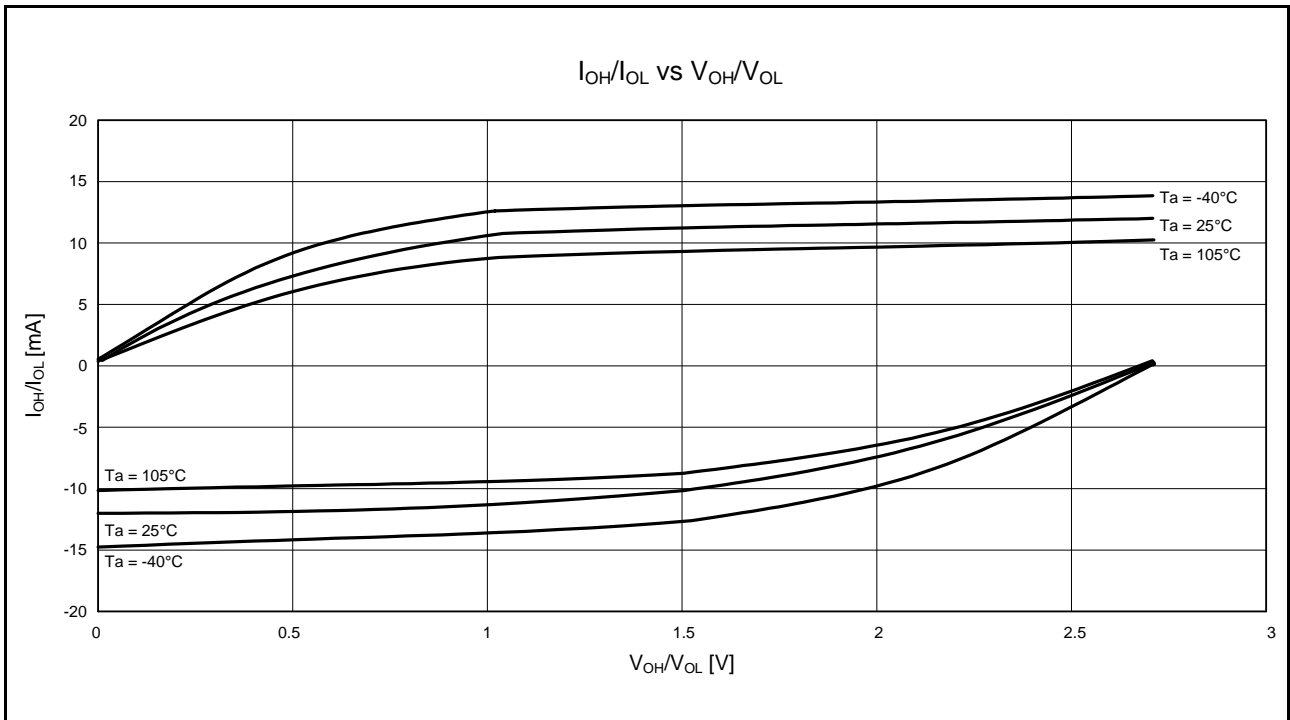


Figure 5.10 VOH/VOL and IOH/IOL Temperature Characteristics at VCC = 2.7 V When Normal Output is Selected (Reference Data)

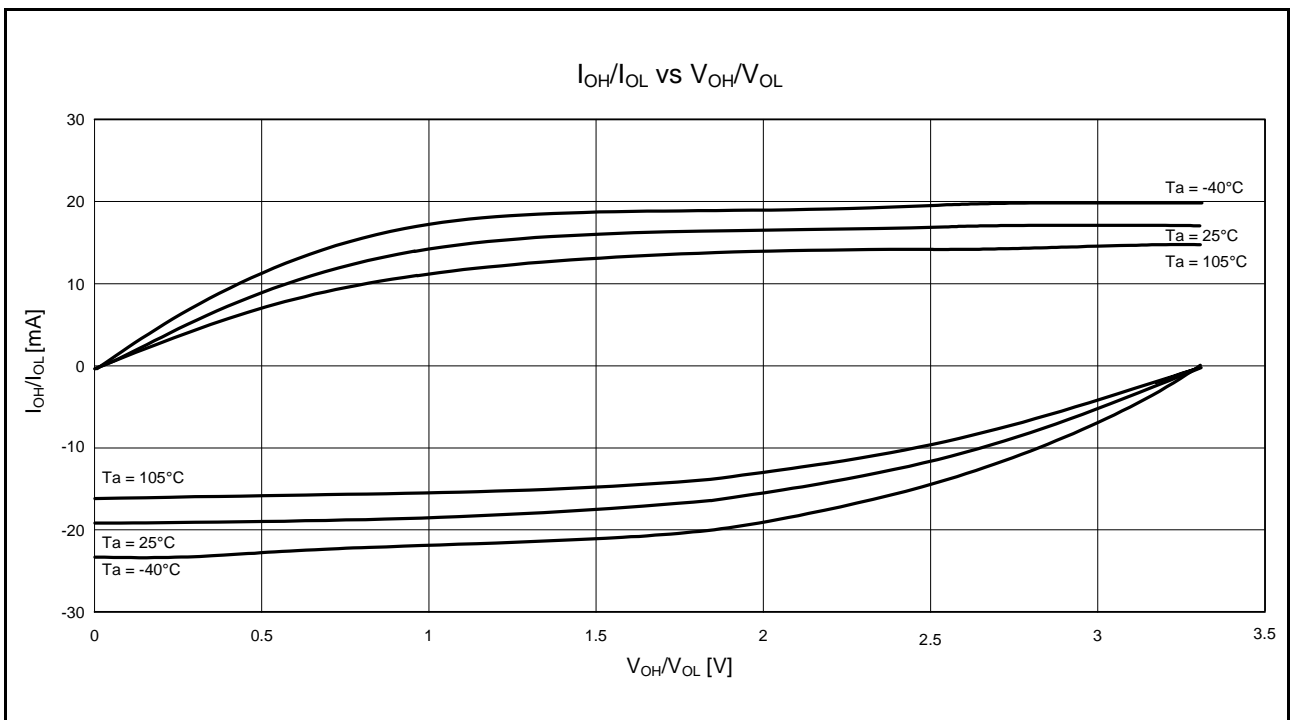


Figure 5.11 VOH/VOL and IOH/IOL Temperature Characteristics at VCC = 3.3 V When Normal Output is Selected (Reference Data)

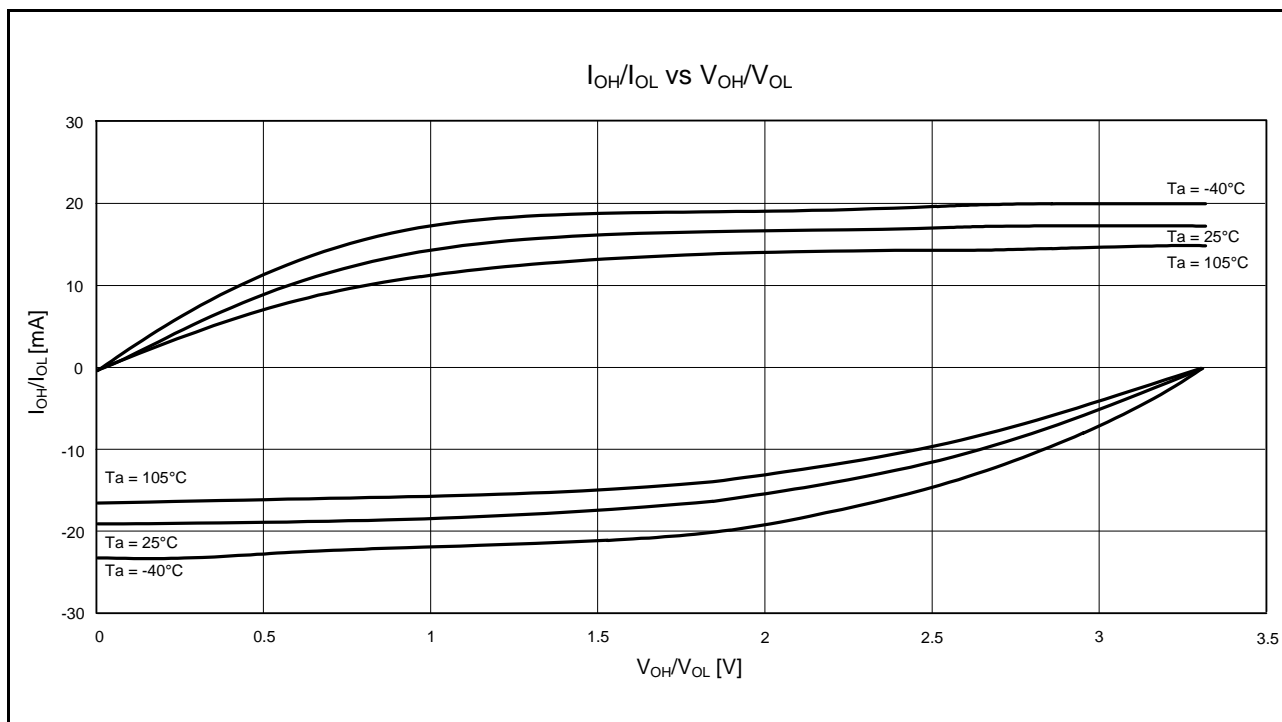


Figure 5.12 VOH/VOL and IOH/IOL Temperature Characteristics at VCC = 5.5 V When Normal Output is Selected (Reference Data)

5.2.2 Normal I/O Pin Output Characteristics (2)

Figure 5.13 to Figure 5.17 show the characteristics when high-drive output is selected by the drive capacity control register.

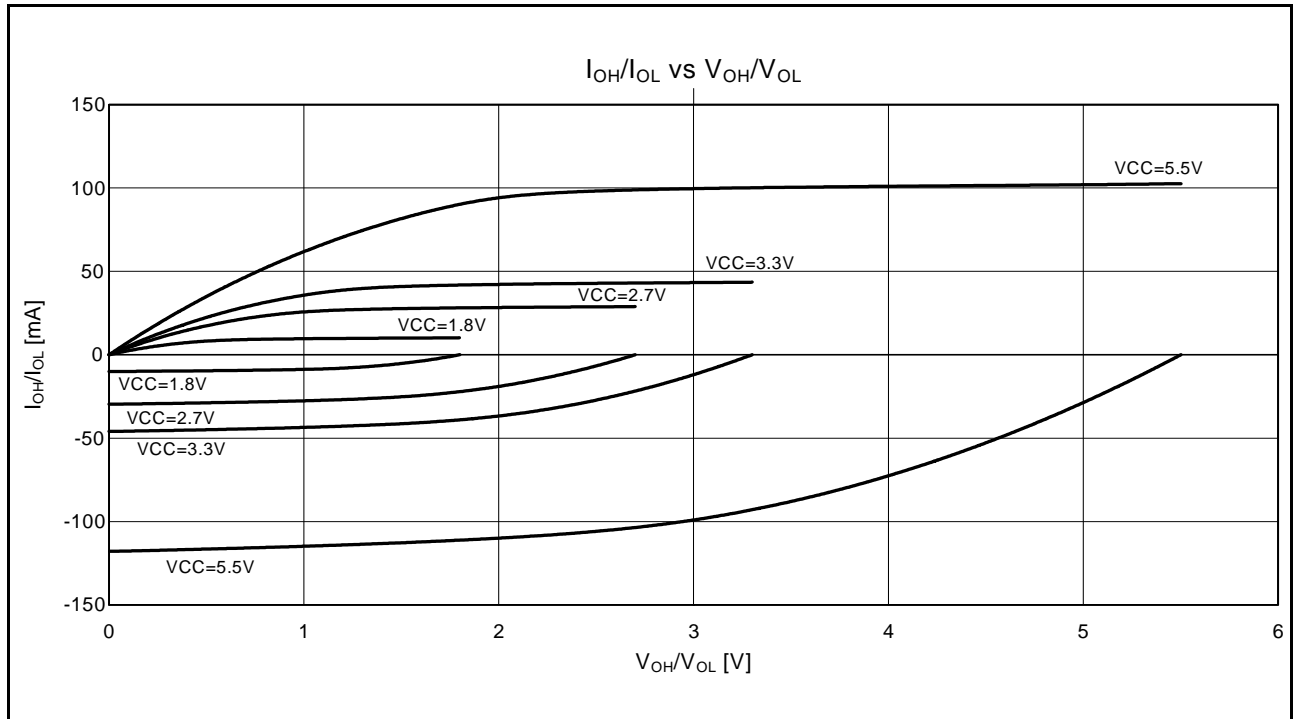


Figure 5.13 V_{OH}/V_{OL} and I_{OH}/I_{OL} Voltage Characteristics at $T_a = 25^\circ\text{C}$ When High-Drive Output is Selected (Reference Data)

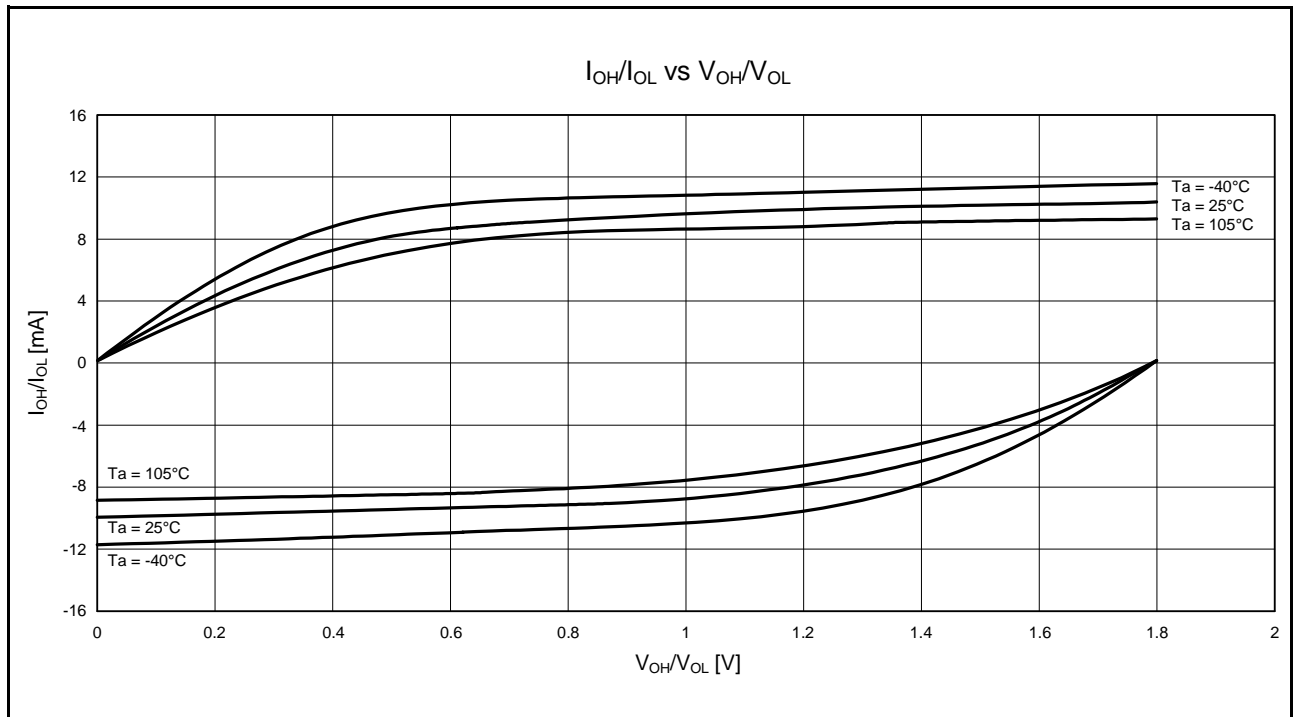


Figure 5.14 V_{OH}/V_{OL} and I_{OH}/I_{OL} Temperature Characteristics at $V_{CC} = 1.8\text{ V}$ When High-Drive Output is Selected (Reference Data)

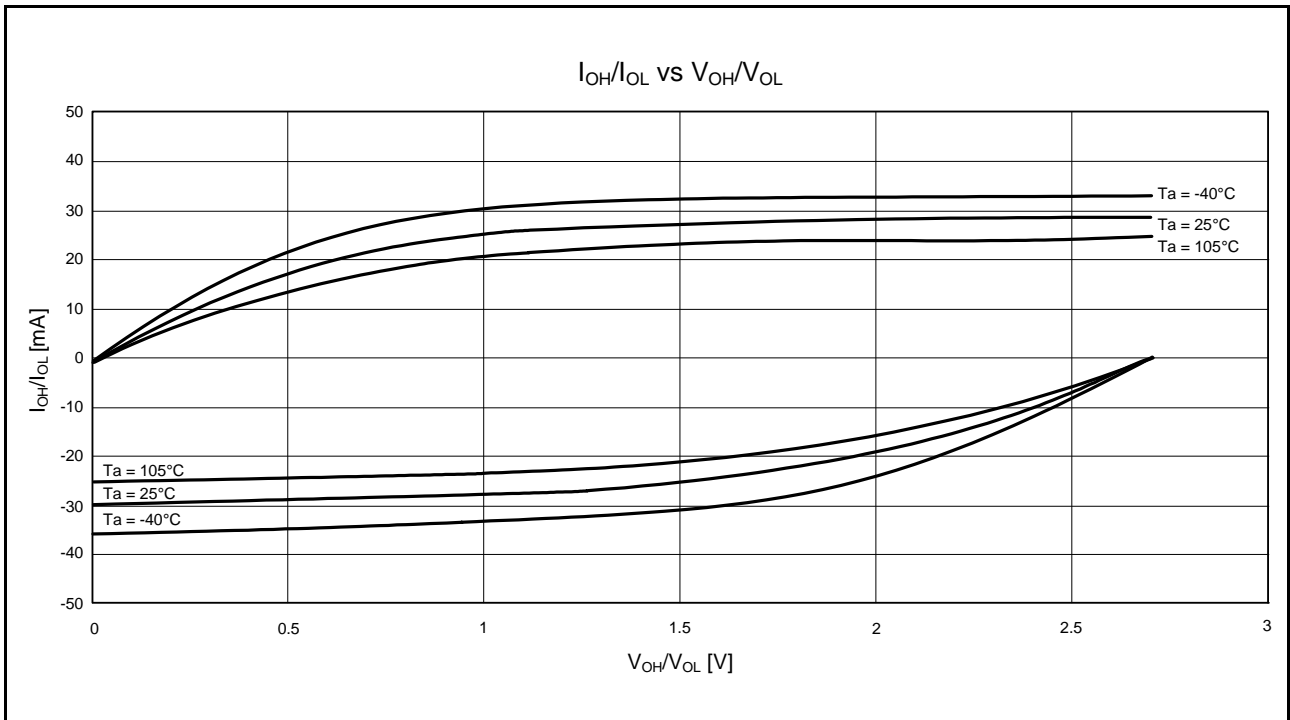


Figure 5.15 V_{OH}/V_{OL} and I_{OH}/I_{OL} Temperature Characteristics at $V_{CC} = 2.7$ V When High-Drive Output is Selected (Reference Data)

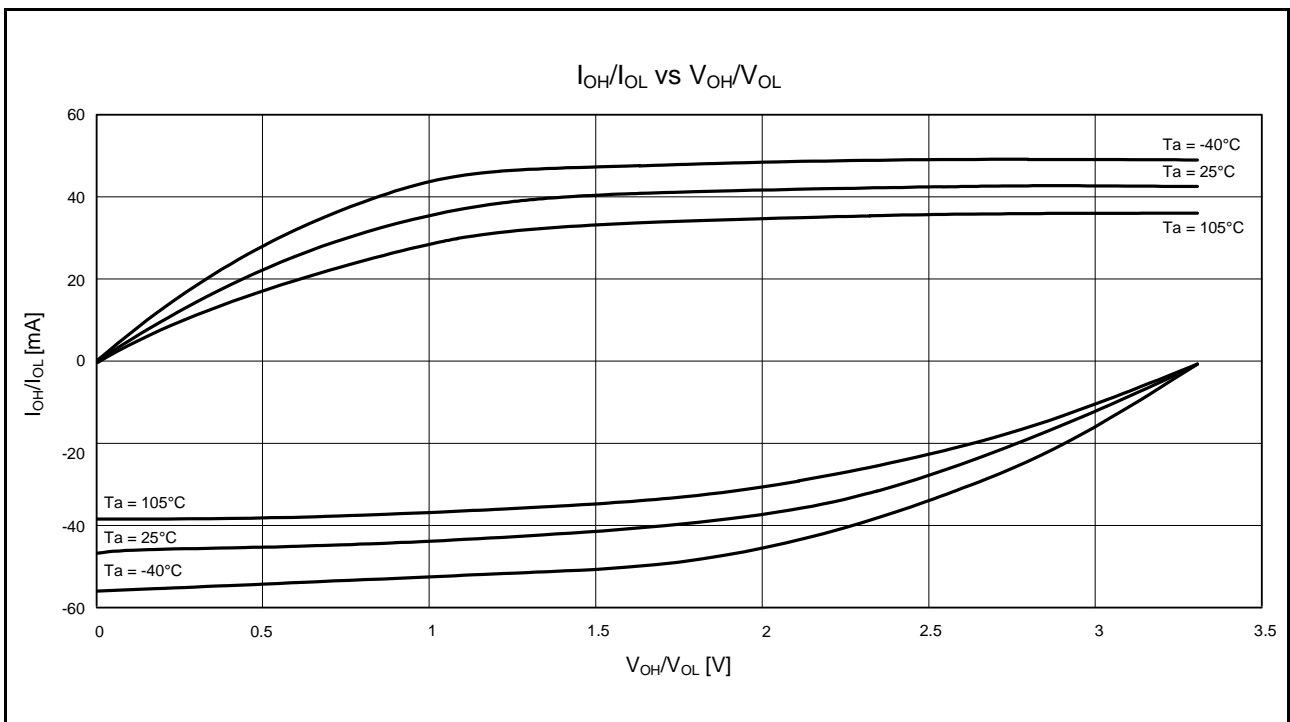


Figure 5.16 V_{OH}/V_{OL} and I_{OH}/I_{OL} Temperature Characteristics at $V_{CC} = 3.3$ V When High-Drive Output is Selected (Reference Data)

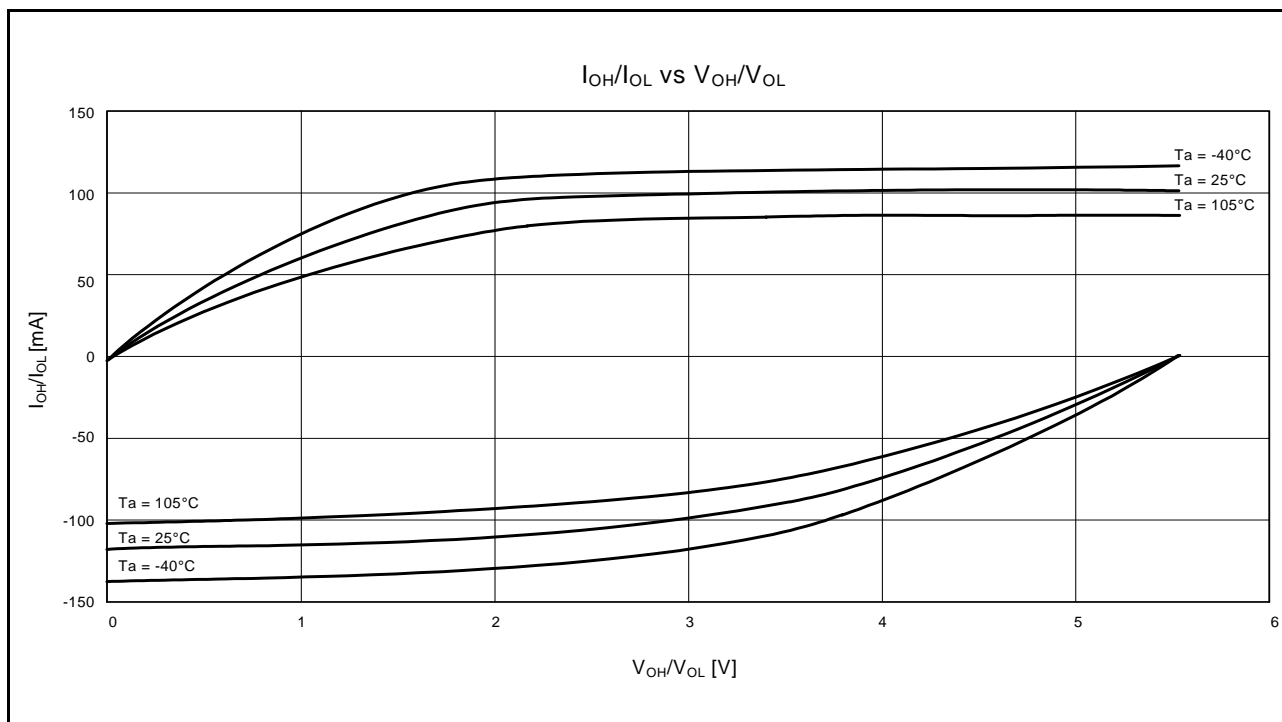


Figure 5.17 VOH/VOL and IOH/IOL Temperature Characteristics at VCC = 5.5 V When High-Drive Output is Selected (Reference Data)

5.2.3 Normal I/O Pin Output Characteristics (3)

Figure 5.18 to Figure 5.21 show the characteristics of the RIIC output pin.

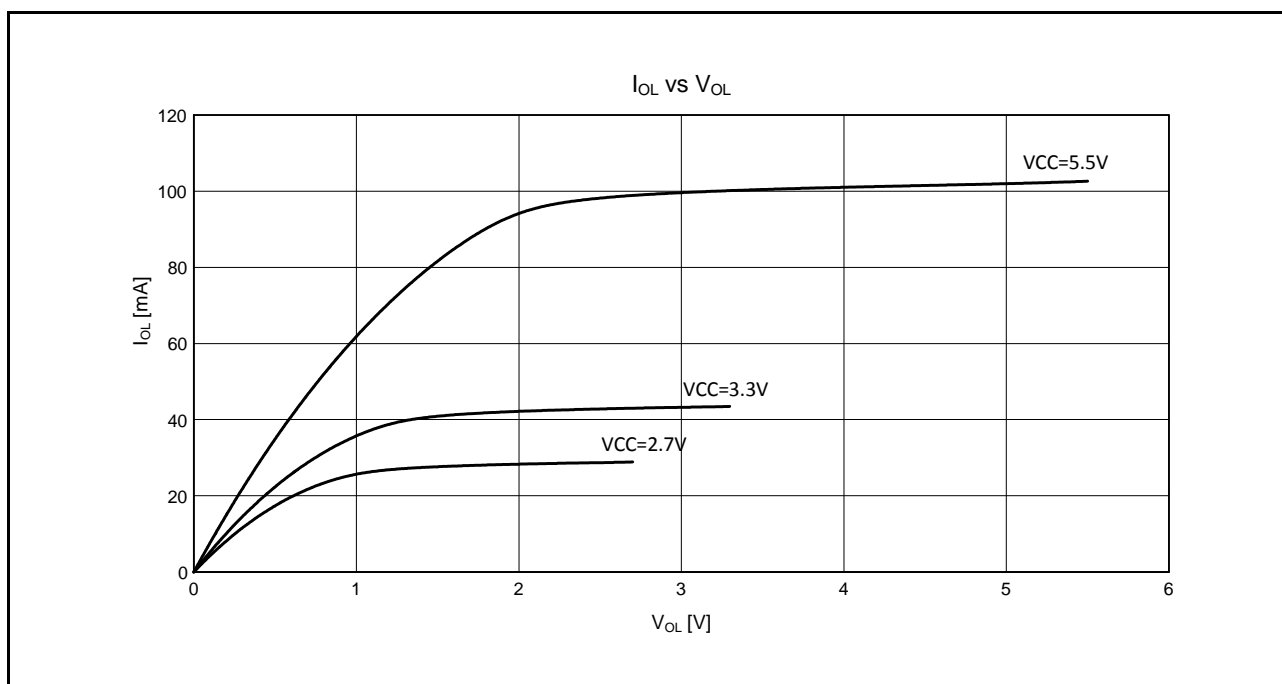


Figure 5.18 V_{OL} and I_{OL} Voltage Characteristics of RIIC Output Pin at T_a = 25°C (Reference Data)

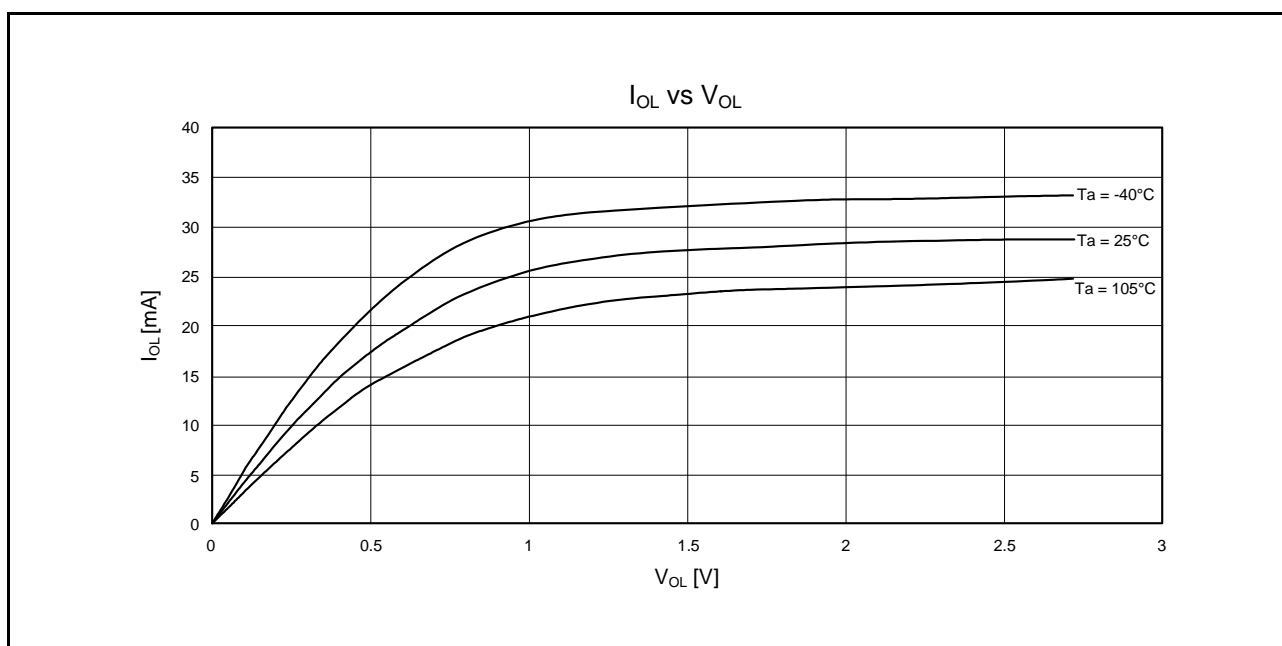


Figure 5.19 V_{OL} and I_{OL} Temperature Characteristics of RIIC Output Pin at VCC = 2.7 V (Reference Data)

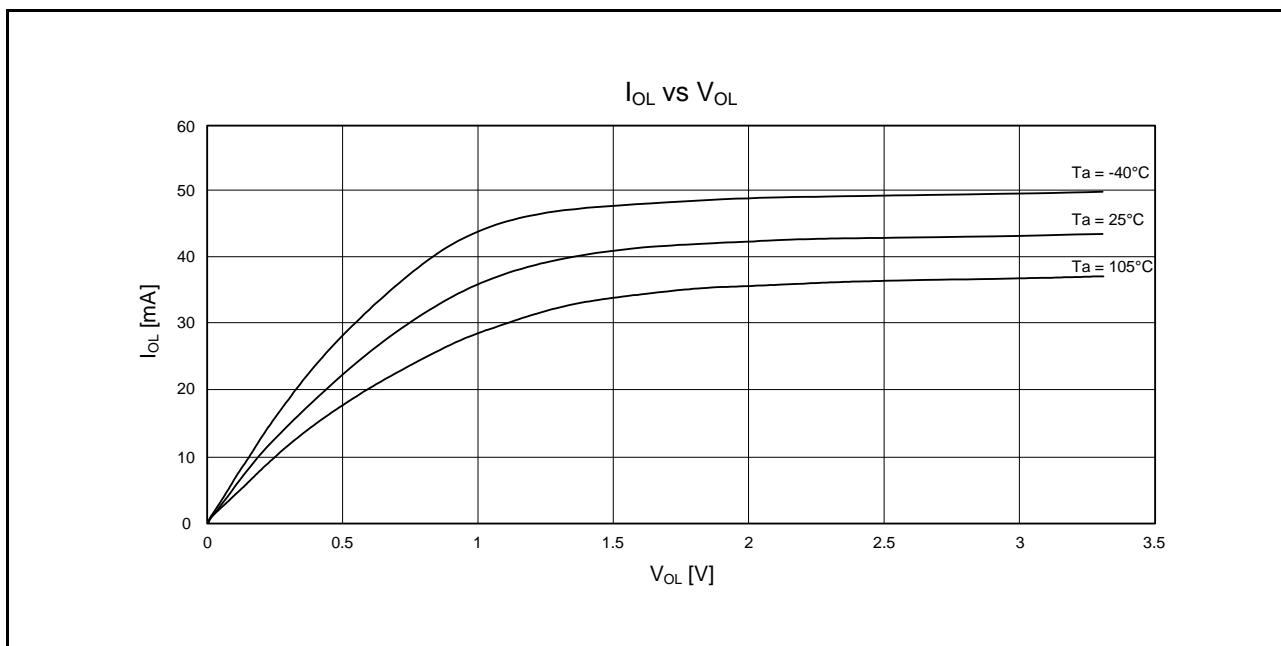


Figure 5.20 V_{OL} and I_{OL} Temperature Characteristics of RIIC Output Pin at VCC = 3.3 V (Reference Data)

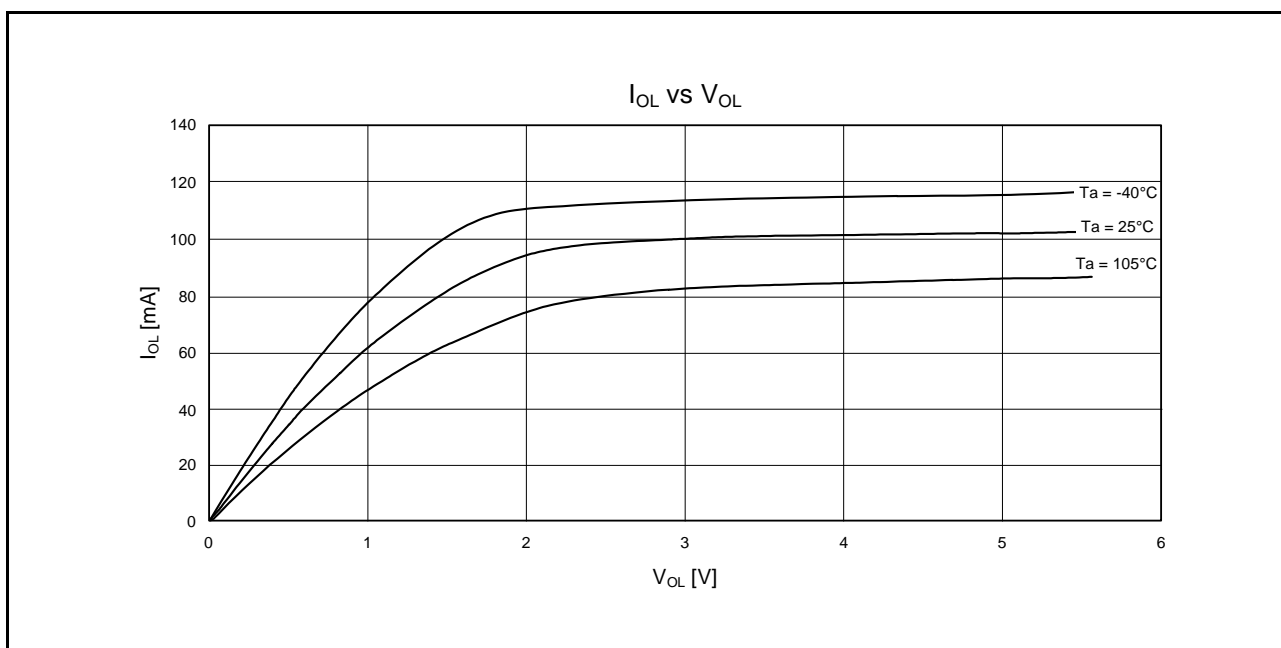


Figure 5.21 V_{OL} and I_{OL} Temperature Characteristics of RIIC Output Pin at VCC = 5.5 V (Reference Data)

5.3 AC Characteristics

5.3.1 Clock Timing

Table 5.21 Operating Frequency Value (High-Speed Operating Mode)

Conditions: $1.8\text{ V} \leq \text{VCC} = \text{VCC_USB} = \text{AVCC0} \leq 5.5\text{ V}$, $\text{VSS} = \text{AVSS0} = \text{VREFL0} = \text{VSS_USB} = 0\text{ V}$, $T_a = -40$ to $+105^\circ\text{C}$

Item	Symbol	VCC				Unit	
		$1.8\text{ V} \leq \text{VCC} < 2.4\text{ V}$	$2.4\text{ V} \leq \text{VCC} < 2.7\text{ V}$	$2.7\text{ V} \leq \text{VCC} \leq 5.5\text{ V}$	When USB is in Use*3		
Maximum operating frequency*4	System clock (ICLK)	f_{max}	8	16	54	54	MHz
	FlashIF clock (FCLK)*1, *2		8	16	32	32	
	Peripheral module clock (PCLKA)		8	16	54	54	
	Peripheral module clock (PCLKB)		8	16	32	32	
	Peripheral module clock (PCLKD)		8	32	54	54	
	External bus clock (BCLK)		8	16	32	32	
	BCLK pin output		8	8	16	16	
USB clock (UCLK)	f_{usb}	—	—	—	48		

Note 1. The lower-limit frequency of FCLK is 1 MHz during programming or erasing of the flash memory. When FCLK is in use at below 4 MHz, the frequency can be set to 1 MHz, 2 MHz, or 3 MHz. A non-integer frequency such as 1.5 MHz cannot be set.

Note 2. The frequency accuracy of FCLK must be within $\pm 3.5\%$.

Note 3. The VCC_USB range is 3.0 to 5.5 V when the USB clock is in use.

Note 4. The maximum operating frequency listed above does not include errors of the external oscillator and internal oscillator. For details on the range for the guaranteed operation, see Table 5.26, Clock Timing.

Table 5.22 Operating Frequency Value (Middle-Speed Operating Mode)

Conditions: $1.8\text{ V} \leq \text{VCC} = \text{VCC_USB} = \text{AVCC0} \leq 5.5\text{ V}$, $\text{VSS} = \text{AVSS0} = \text{VREFL0} = \text{VSS_USB} = 0\text{ V}$, $T_a = -40$ to $+105^\circ\text{C}$

Item	Symbol	VCC				Unit	
		$1.8\text{ V} \leq \text{VCC} < 2.4\text{ V}$	$2.4\text{ V} \leq \text{VCC} < 2.7\text{ V}$	$2.7\text{ V} \leq \text{VCC} \leq 5.5\text{ V}$	When USB is in Use*3		
Maximum operating frequency*4	System clock (ICLK)	f_{max}	8	12	12	12	MHz
	FlashIF clock (FCLK)*1, *2		8	12	12	12	
	Peripheral module clock (PCLKA)		8	12	12	12	
	Peripheral module clock (PCLKB)		8	12	12	12	
	Peripheral module clock (PCLKD)		8	12	12	12	
	External bus clock (BCLK)		8	12	12	12	
	BCLK pin output		8	8	12	12	
USB clock (UCLK)	f_{usb}	—	—	—	48		

Note 1. The lower-limit frequency of FCLK is 1 MHz during programming or erasing of the flash memory. When using FCLK at below 4 MHz, the frequency can be set to 1 MHz, 2 MHz, or 3 MHz. A non-integer frequency such as 1.5 MHz cannot be set.

Note 2. The frequency accuracy of FCLK must be within $\pm 3.5\%$.

Note 3. The VCC_USB range is 3.0 to 5.5 V when the USB clock is in use.

Note 4. The maximum operating frequency listed above does not include errors of the external oscillator and internal oscillator. For details on the range for the guaranteed operation, see Table 5.26, Clock Timing.

Table 5.23 Operating Frequency Value (Low-Speed Operating Mode)Conditions: $1.8\text{ V} \leq VCC = VCC_USB = AVCC0 \leq 5.5\text{ V}$, $VSS = AVSS0 = VREFL0 = VSS_USB = 0\text{ V}$, $T_a = -40\text{ to }+105^\circ\text{C}$

Item	Symbol	VCC			Unit	
		$1.8\text{ V} \leq VCC < 2.4\text{ V}$	$2.4\text{ V} \leq VCC < 2.7\text{ V}$	$2.7\text{ V} \leq VCC \leq 5.5\text{ V}$		
Maximum operating frequency*3	System clock (ICLK)	f_{\max}	32.768			kHz
	FlashIF clock (FCLK)*1		32.768			
	Peripheral module clock (PCLKA)		32.768			
	Peripheral module clock (PCLKB)		32.768			
	Peripheral module clock (PCLKD)*2		32.768			
	External bus clock (BCLK)		32.768			
	BCLK pin output		32.768			

Note 1. Programming and erasing the flash memory is impossible.

Note 2. The A/D converter cannot be used.

Note 3. The maximum operating frequency listed above does not include errors of the external oscillator. For details on the range for the guaranteed operation, see Table 5.26, Clock Timing.

Table 5.24 BCLK Clock Timing (1)Conditions: $2.7\text{ V} \leq VCC = VCC_USB = AVCC0 \leq 5.5\text{ V}$, $VSS = AVSS0 = VREFL0 = VSS_USB = 0\text{ V}$, $f_{\text{BCLK}} \leq 32\text{ MHz}$ (BCLK pin output frequency $\leq 16\text{ MHz}$), $T_a = -40\text{ to }+105^\circ\text{C}$

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
BCLK pin output cycle time	t_{Bcyc}	62.5	—	—	ns	Figure 5.22
BCLK pin output high pulse width	t_{CH}	15	—	—	ns	
BCLK pin output low pulse width	t_{CL}	15	—	—	ns	
BCLK pin output rise time	t_{Cr}	—	—	12	ns	
BCLK pin output fall time	t_{Cf}	—	—	12	ns	

Table 5.25 BCLK Clock Timing (2)Conditions: $1.8\text{ V} \leq VCC = VCC_USB = AVCC0 < 2.7\text{ V}$, $VSS = AVSS0 = VREFL0 = VSS_USB = 0\text{ V}$, $f_{\text{BCLK}} \leq 16\text{ MHz}$ (BCLK pin output frequency $\leq 8\text{ MHz}$), $T_a = -40\text{ to }+105^\circ\text{C}$

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
BCLK pin output cycle time	t_{Bcyc}	125	—	—	ns	Figure 5.22
BCLK pin output high pulse width	t_{CH}	30	—	—	ns	
BCLK pin output low pulse width	t_{CL}	30	—	—	ns	
BCLK pin output rise time	t_{Cr}	—	—	25	ns	
BCLK pin output fall time	t_{Cf}	—	—	25	ns	

Table 5.26 Clock TimingConditions: $1.8\text{ V} \leq \text{VCC} = \text{VCC_USB} = \text{AVCC0} \leq 5.5\text{ V}$, $\text{VSS} = \text{AVSS0} = \text{VREFL0} = \text{VSS_USB} = 0\text{ V}$, $T_a = -40\text{ to }+105^\circ\text{C}$

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions	
EXTAL external clock input cycle time	t_{Xcyc}	50	—	—	ns	Figure 5.23	
EXTAL external clock input high pulse width	t_{XH}	20	—	—	ns		
EXTAL external clock input low pulse width	t_{XL}	20	—	—	ns		
EXTAL external clock rise time	t_{Xr}	—	—	5	ns		
EXTAL external clock fall time	t_{Xf}	—	—	5	ns		
EXTAL external clock input wait time*1	t_{XWT}	0.5	—	—	μs		
Main clock oscillator oscillation frequency*2	f_{MAIN}	$2.4 \leq \text{VCC} \leq 5.5$	1	—	20		MHz
		$1.8 \leq \text{VCC} < 2.4$	1	—	8		
Main clock oscillator stabilization time (crystal)*2	t_{MAINOSC}	—	3	—	ms	Figure 5.24	
Main clock oscillator stabilization time (ceramic resonator)*2	t_{MAINOSC}	—	50	—	μs		
LOCO clock oscillation frequency	f_{LOCO}	3.44	4.0	4.56	MHz		
LOCO clock oscillation stabilization time	t_{LOCO}	—	—	0.5	μs	Figure 5.25	
IWDT-dedicated clock oscillation frequency	f_{ILOCO}	12.75	15	17.25	kHz		
IWDT-dedicated clock oscillation stabilization time	t_{ILOCO}	—	—	50	μs	Figure 5.26	
HOCO clock oscillation frequency	f_{HOCO} (32 MHz)	31.52	32	32.48	MHz	$T_a = -40\text{ to }+85^\circ\text{C}$	
		31.68	32	32.32		$T_a = 0\text{ to }+55^\circ\text{C}$	
		31.36	32	32.64		$T_a = -40\text{ to }+105^\circ\text{C}$	
	f_{HOCO} (54 MHz)	53.19	54	54.81	MHz	$T_a = -40\text{ to }+85^\circ\text{C}$	
		53.46	54	54.54		$T_a = 0\text{ to }+55^\circ\text{C}$	
		52.92	54	55.08		$T_a = -40\text{ to }+105^\circ\text{C}$	
HOCO clock oscillation stabilization time	t_{HOCO}	—	—	30	μs	Figure 5.28	
PLL input frequency*3	f_{PLLIN}	4	—	12.5	MHz		
PLL circuit oscillation frequency*3	f_{PLL}	24	—	54	MHz		
PLL clock oscillation stabilization time	t_{PLL}	—	—	50	μs	Figure 5.29	
PLL free-running oscillation frequency	f_{PLLFR}	—	8	—	MHz		
USBPLL input frequency*5	f_{PLLIN}	—	6, 8*6	—	MHz		
USBPLL circuit oscillation frequency*5	f_{PLL}	—	48*6	—	MHz		
USBPLL clock oscillation stabilization time	t_{PLL}	—	—	50	μs	Figure 5.29	
Sub-clock oscillator oscillation frequency*7	f_{SUB}	—	32.768	—	kHz		
Sub-clock oscillator stabilization time*4	t_{SUBOSC}	—	0.5	—	s	Figure 5.30	

Note 1. Time until the clock can be used after the main clock oscillator stop bit (MOSCCR.MOSTP) is set to 0 (operating).

Note 2. Reference values when an 8-MHz resonator is used.

When specifying the main clock oscillator stabilization time, set the MOSCWTCR register with a stabilization time value that is equal to or greater than the resonator-manufacturer-recommended value.

After the MOSCCR.MOSTP bit is changed to enable the main clock oscillator, confirm that the OSCOVFSR.MOOVF flag has become 1, and then start using the main clock.

Note 3. The VCC range should be 2.4 to 5.5 V when the PLL is used.

Note 4. Reference values when a 32.768-kHz resonator is used.

After the setting of the SOSCCR.SOSTP bit or RCR3.RTCEN bit is changed to operate the sub-clock oscillator, only start using the sub-clock after the sub-clock oscillation stabilization wait time that is equal to or greater than the oscillator-manufacturer-recommended value has elapsed.

Note 5. The VCC range should be 3.0 to 5.5 V when the USBPLL is used.

Note 6. The input frequency can be set to 6 or 8 MHz and the oscillation frequency can be set to 48 MHz only.

Note 7. Only 32.768 kHz can be used.

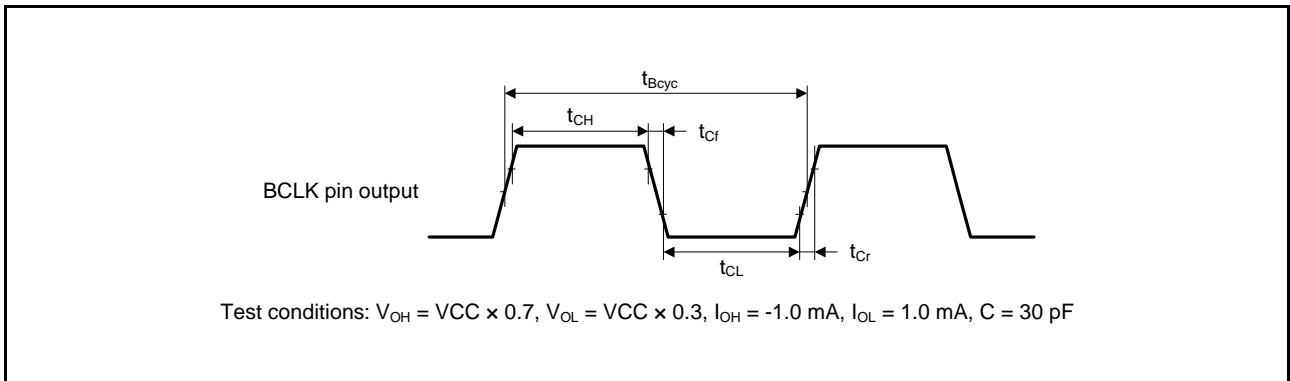


Figure 5.22 BCLK Pin Output Timing

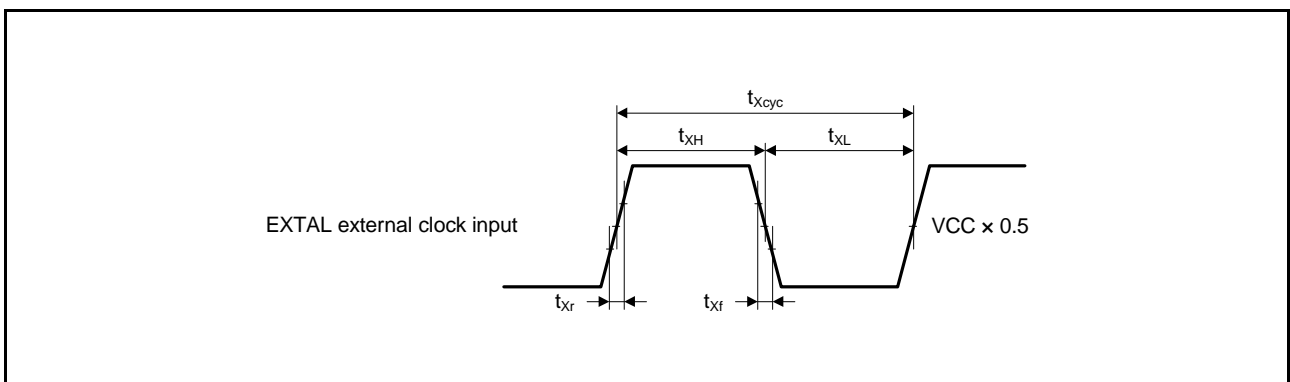


Figure 5.23 EXTAL External Clock Input Timing

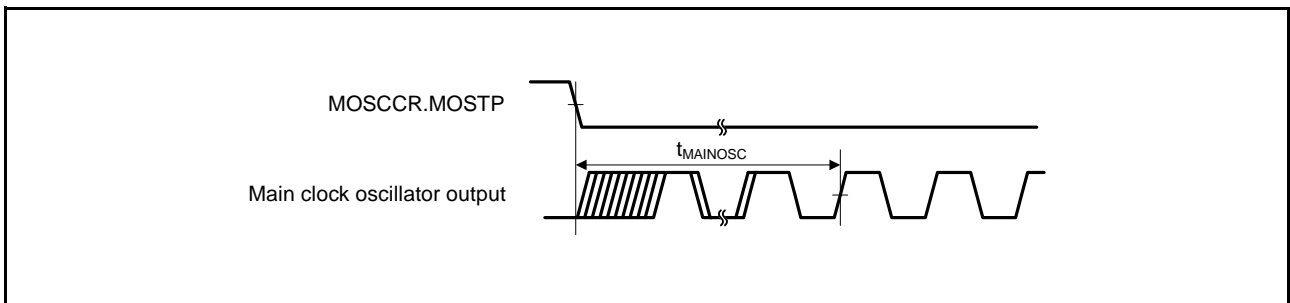


Figure 5.24 Main Clock Oscillation Start Timing

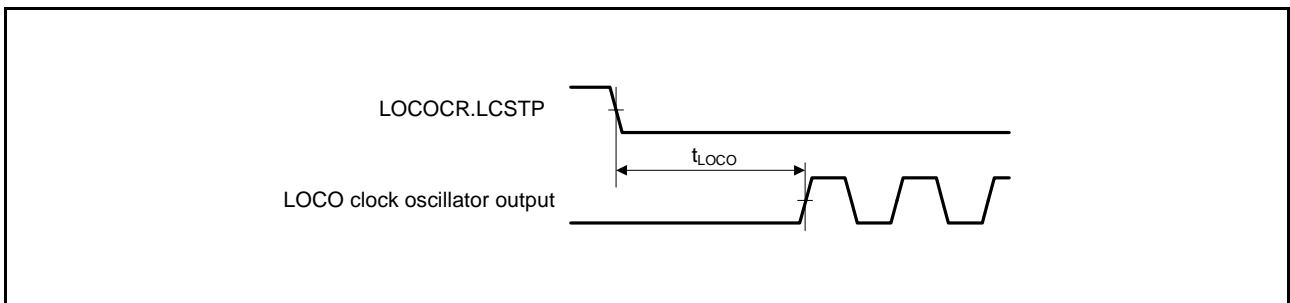


Figure 5.25 LOCO Clock Oscillation Start Timing

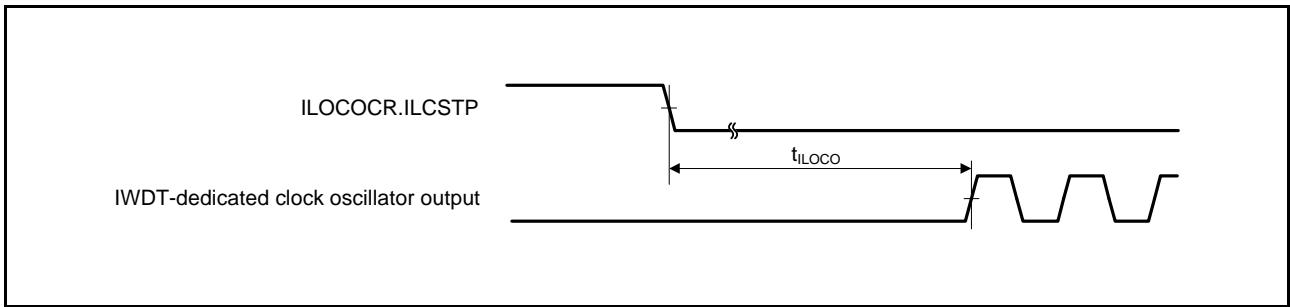


Figure 5.26 IWDT-Dedicated Clock Oscillation Start Timing

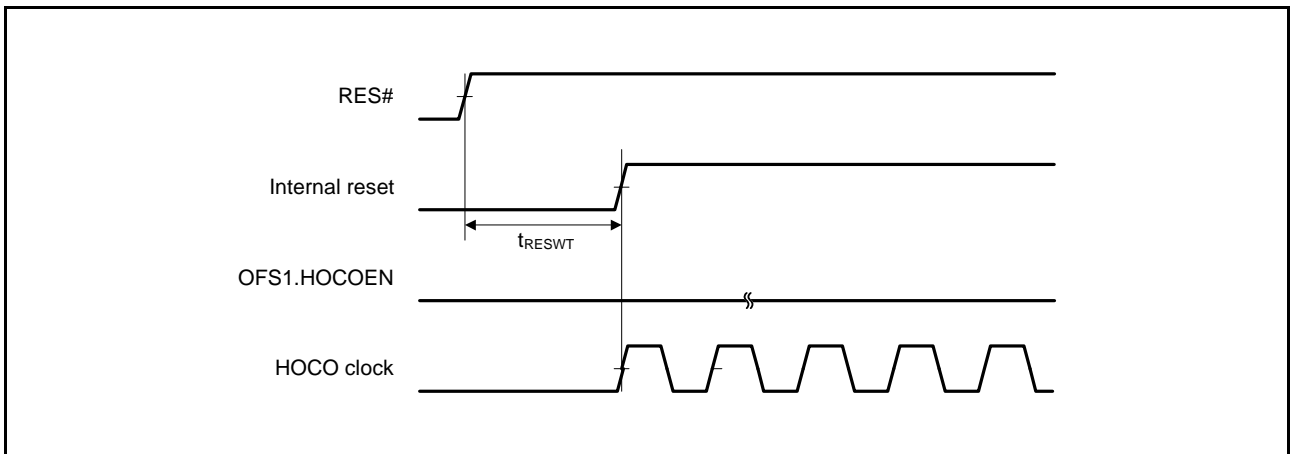


Figure 5.27 HOCO Clock Oscillation Start Timing (After Reset is Canceled by Setting OFS1.HOCOEN Bit to 0)

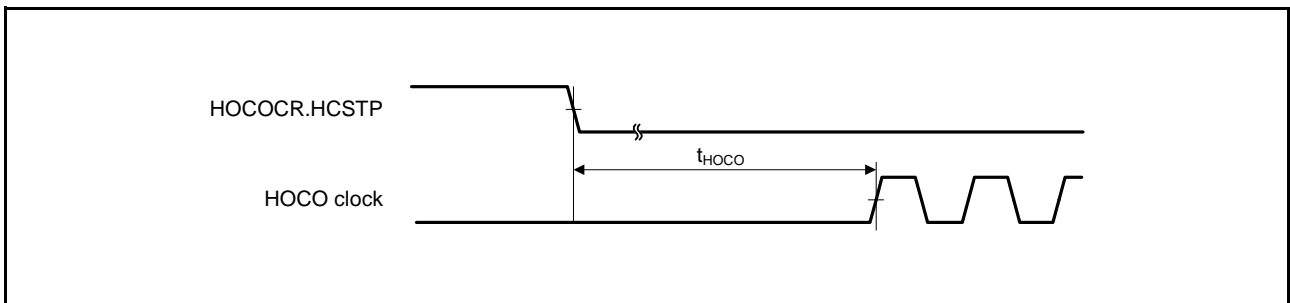


Figure 5.28 HOCO Clock Oscillation Start Timing (Oscillation is Started by Setting HOCOCR.HCSTP Bit)

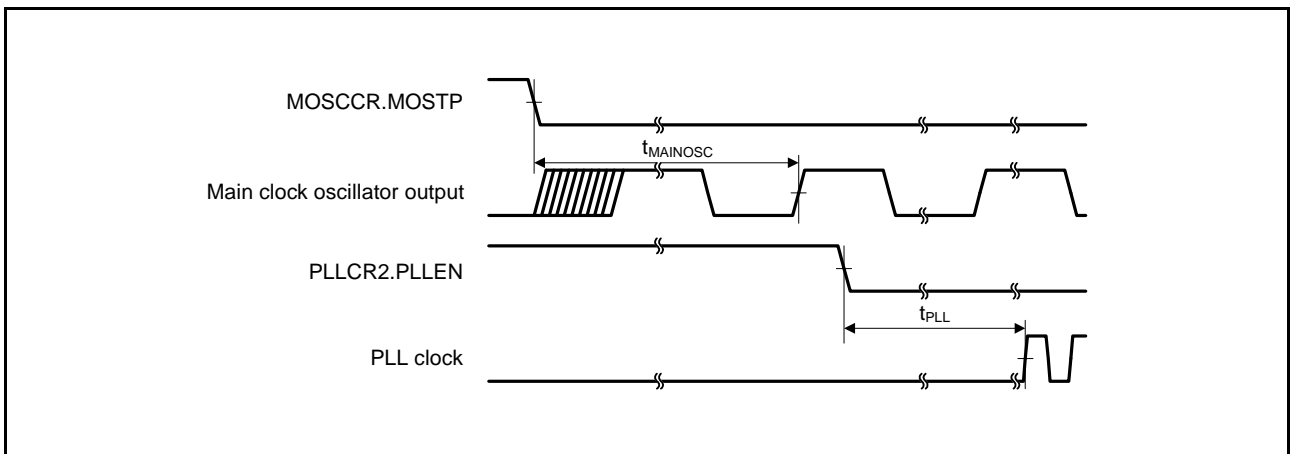


Figure 5.29 PLL Clock Oscillation Start Timing (PLL is Operated after Main Clock Oscillation Has Been Stabled)

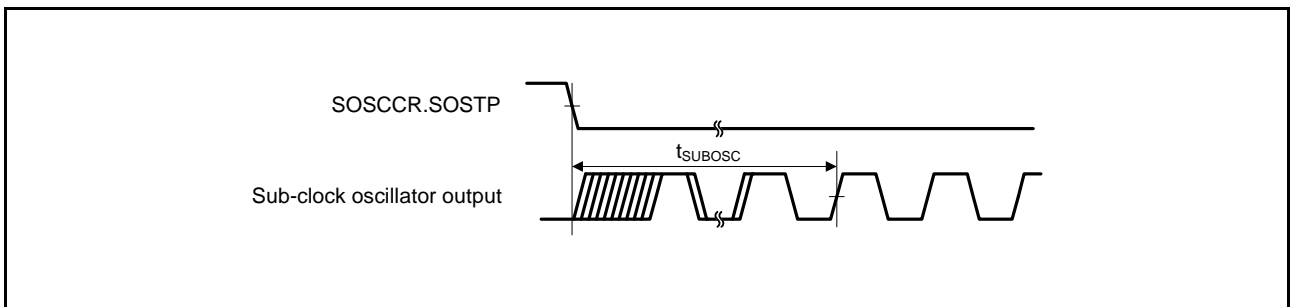


Figure 5.30 Sub-Clock Oscillation Start Timing

5.3.2 Reset Timing

Table 5.27 Reset Timing

Conditions: $1.8\text{ V} \leq VCC = VCC_USB = AVCC0 \leq 5.5\text{ V}$, $VSS = AVSS0 = VREFL0 = VSS_USB = 0\text{ V}$, $T_a = -40\text{ to }+105^\circ\text{C}$

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions	
RES# pulse width	At power-on	t_{RESWP}	3	—	—	ms	Figure 5.31
	Other than above	t_{RESW}	30	—	—	μs	Figure 5.32
Wait time after RES# cancellation (at power-on)	At normal startup*1	t_{RESWT}	—	8.5	—	ms	Figure 5.31
	During fast startup time*2	t_{RESWT}	—	560	—	μs	
Wait time after RES# cancellation (during powered-on state)	t_{RESWT}	—	120	—	μs	Figure 5.32	
Independent watchdog timer reset period	t_{RESWIW}	—	1	—	IWDT clock cycle	Figure 5.33	
Watchdog timer reset period	t_{RESWWW}	—	4	—	PCLKB cycle		
Software reset period	t_{RESWSW}	—	1	—	ICLK cycle		
Wait time after independent watchdog timer reset cancellation*3	t_{RESWT2}	—	300	—	μs		
Wait time after watchdog timer reset cancellation*4	t_{RESWT2}	—	300	—	μs		
Wait time after software reset cancellation	t_{RESWT2}	—	170	—	μs		

Note 1. When OFS1.(LVDAS, FASTSTUP) bits are 11b.

Note 2. When OFS1.(LVDAS, FASTSTUP) bits are a value other than 11b.

Note 3. When IWDTCR.CKS[3:0] bits are 0000b.

Note 4. When WDTCR.CKS[3:0] bits are 0001b.

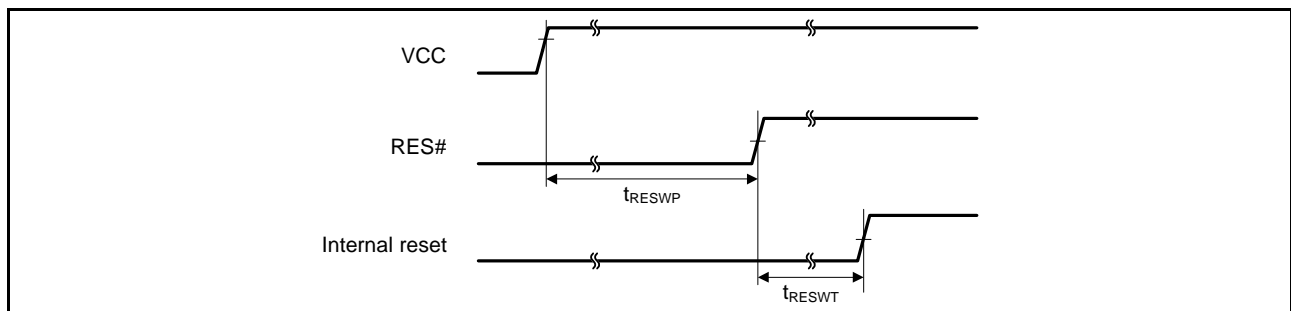


Figure 5.31 Reset Input Timing at Power-On

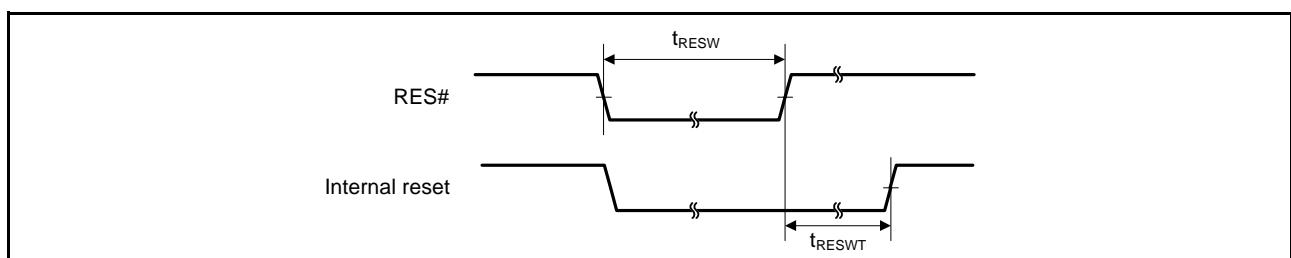


Figure 5.32 Reset Input Timing (1)

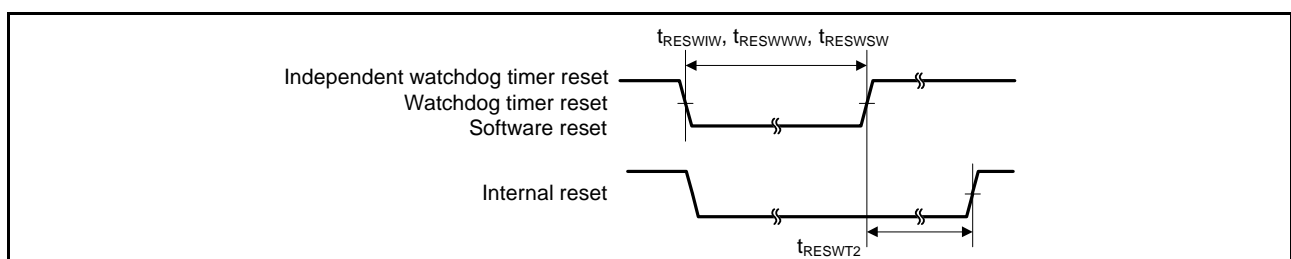


Figure 5.33 Reset Input Timing (2)

5.3.3 Timing of Recovery from Low Power Consumption Modes

Table 5.28 Timing of Recovery from Low Power Consumption Modes (1)

Conditions: $1.8\text{ V} \leq V_{CC} = V_{CC_USB} = AV_{CC0} \leq 5.5\text{ V}$, $V_{SS} = AV_{SS0} = V_{REFL0} = V_{SS_USB} = 0\text{ V}$, $T_a = -40\text{ to }+105^\circ\text{C}$

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions		
Recovery time from software standby mode*1	High-speed mode	Crystal connected to main clock oscillator	Main clock oscillator operating*2	t _{SBYMC}	—	2	3	ms	Figure 5.34
		External clock input to main clock oscillator	Main clock oscillator operating*3	t _{SBYEX}	—	35	50	μs	
		Sub-clock oscillator operating		t _{SBYSC}	—	650	800	μs	
		HOCO clock oscillator operating		t _{SBYHO}	—	40	55	μs	
		LOCO clock oscillator operating		t _{SBYLO}	—	40	55	μs	

Note 1. The recovery time varies depending on the state of each oscillator when the WAIT instruction is executed. When multiple oscillators are operating, the recovery time varies depending on the operating state of the oscillators that are not selected as the system clock source. The above table applies when only the corresponding clock is operating.

Note 2. When the frequency of the crystal is 20 MHz.

When the main clock oscillator wait control register (MOSCWTCR) is set to 04h.

Note 3. When the frequency of the external clock is 20 MHz.

When the main clock oscillator wait control register (MOSCWTCR) is set to 00h.

Table 5.29 Timing of Recovery from Low Power Consumption Modes (2)

Conditions: $1.8\text{ V} \leq V_{CC} = V_{CC_USB} = AV_{CC0} \leq 5.5\text{ V}$, $V_{SS} = AV_{SS0} = V_{REFL0} = V_{SS_USB} = 0\text{ V}$, $T_a = -40\text{ to }+105^\circ\text{C}$

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions		
Recovery time from software standby mode*1	Middle-speed mode	Crystal connected to main clock oscillator	Main clock oscillator operating*2	t _{SBYMC}	—	2	3	ms	Figure 5.34
			Main clock oscillator and PLL circuit operating*3	t _{SBYPC}	—	2	3	ms	
		External clock input to main clock oscillator	Main clock oscillator operating*4	t _{SBYEX}	—	3	4	μs	
			Main clock oscillator and PLL circuit operating*5	t _{SBYPE}	—	65	85	μs	
		Sub-clock oscillator operating		t _{SBYSC}	—	600	750	μs	
		HOCO clock oscillator operating*6		t _{SBYHO}	—	40	50	μs	
		LOCO clock oscillator operating		t _{SBYLO}	—	5	7	μs	

Note 1. The recovery time varies depending on the state of each oscillator when the WAIT instruction is executed. When multiple oscillators are operating, the recovery time varies depending on the operating state of the oscillators that are not selected as the system clock source. The above table applies when only the corresponding clock is operating.

Note 2. When the frequency of the crystal is 12 MHz.

When the main clock oscillator wait control register (MOSCWTCR) is set to 04h.

Note 3. When the frequency of PLL is 12 MHz.

When the main clock oscillator wait control register (MOSCWTCR) is set to 04h.

Note 4. When the frequency of the external clock is 12 MHz.

When the main clock oscillator wait control register (MOSCWTCR) is set to 00h.

Note 5. When the frequency of PLL is 12 MHz.

When the main clock oscillator wait control register (MOSCWTCR) is set to 00h.

Note 6. This is the case when HOCO is selected as the system clock and its frequency division is set to be 8 MHz.

Table 5.30 Timing of Recovery from Low Power Consumption Modes (3)

Conditions: $1.8\text{ V} \leq VCC = VCC_USB = AVCC0 \leq 5.5\text{ V}$, $VSS = AVSS0 = VREFL0 = VSS_USB = 0\text{ V}$, $T_a = -40\text{ to }+105^\circ\text{C}$

Item			Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Recovery time from software standby mode*1	Low-speed mode	Sub-clock oscillator operating	t_{SBYSC}	—	600	750	μs	Figure 5.34

Note 1. The sub-clock continues oscillating in software standby mode during low-speed mode.

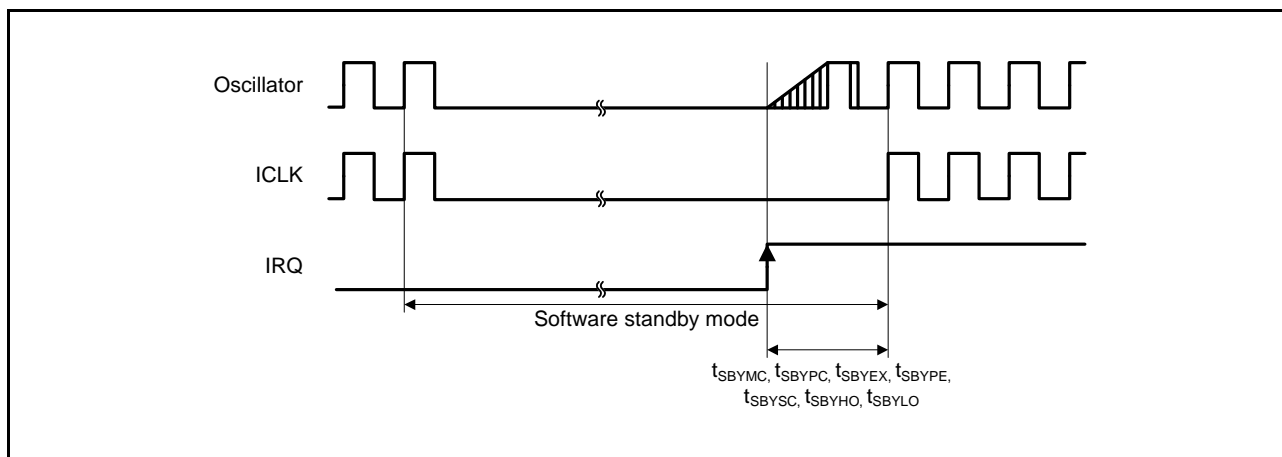


Figure 5.34 Software Standby Mode Recovery Timing

Table 5.31 Timing of Recovery from Low Power Consumption Modes (4)

Conditions: $1.8\text{ V} \leq VCC = VCC_USB = AVCC0 \leq 5.5\text{ V}$, $VSS = AVSS0 = VREFL0 = VSS_USB = 0\text{ V}$, $T_a = -40\text{ to }+105^\circ\text{C}$

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Recovery time from deep sleep mode*1	High-speed mode*2	$t_{DSL P}$	—	2	3.5	μs	Figure 5.35
	Middle-speed mode*3	$t_{DSL P}$	—	3	4	μs	
	Low-speed mode*4	$t_{DSL P}$	—	400	500	μs	

Note 1. Oscillators continue oscillating in deep sleep mode.

Note 2. When the frequency of the system clock is 32 MHz.

Note 3. When the frequency of the system clock is 12 MHz.

Note 4. When the frequency of the system clock is 32 kHz.

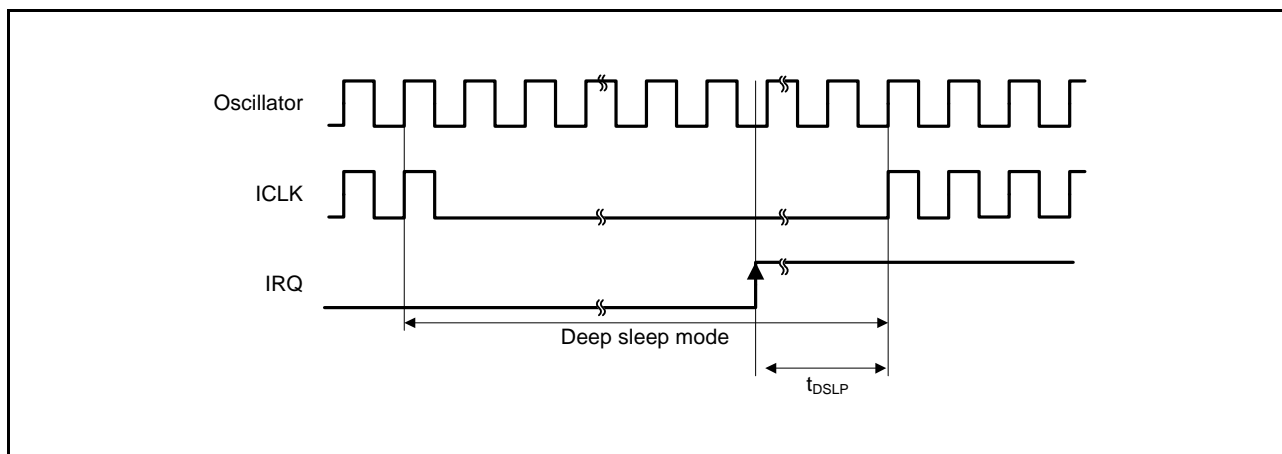


Figure 5.35 Deep Sleep Mode Recovery Timing

Table 5.32 Operating Mode Transition Time

Conditions: $1.8\text{ V} \leq VCC = VCC_USB = AVCC0 \leq 5.5\text{ V}$, $VSS = AVSS0 = VREFL0 = VSS_USB = 0\text{ V}$, $T_a = -40\text{ to }+105^\circ\text{C}$

Mode before Transition	Mode after Transition	ICLK Frequency	Transition Time			Unit
			Min.	Typ.	Max.	
High-speed operating mode	Middle-speed operating modes	8 MHz	—	10	—	μs
Middle-speed operating modes	High-speed operating mode	8 MHz	—	37.5	—	μs
Low-speed operating mode	Middle-speed operating mode, high-speed operating mode	32.768 kHz	—	215	—	μs
Middle-speed operating mode, high-speed operating mode	Low-speed operating mode	32.768 kHz	—	185	—	μs

Note: Values when the frequencies of PCLKA, PCLKB, PCLKD, FCLK, and BCLK are not divided.

5.3.4 Control Signal Timing

Table 5.33 Control Signal Timing

Conditions: $1.8\text{ V} \leq VCC = VCC_USB = AVCC0 \leq 5.5\text{ V}$, $VSS = AVSS0 = VSS_USB = 0\text{ V}$, $T_a = -40\text{ to }+105^\circ\text{C}$

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions	
NMI pulse width	t_{NMIW}	200	—	—	ns	NMI digital filter is disabled (NMIFLTE.NFLTEN = 0)	
		$t_{Pcyc} \times 2^{*1}$	—	—			$t_{Pcyc} \times 2 \leq 200\text{ ns}$
		200	—	—		NMI digital filter is enabled (NMIFLTE.NFLTEN = 1)	$t_{NMICK} \times 3 \leq 200\text{ ns}$
		$t_{NMICK} \times 3.5^{*2}$	—	—			$t_{NMICK} \times 3 > 200\text{ ns}$
IRQ pulse width	t_{IRQW}	200	—	—	ns	IRQ digital filter is disabled (IRQFLTE0.FLTENi = 0)	
		$t_{Pcyc} \times 2^{*1}$	—	—			$t_{Pcyc} \times 2 \leq 200\text{ ns}$
		200	—	—		IRQ digital filter is enabled (IRQFLTE0.FLTENi = 1)	$t_{IRQCK} \times 3 \leq 200\text{ ns}$
		$t_{IRQCK} \times 3.5^{*3}$	—	—			$t_{IRQCK} \times 3 > 200\text{ ns}$

Note: 200 ns minimum in software standby mode.

Note 1. t_{Pcyc} indicates the cycle of PCLKB.

Note 2. t_{NMICK} indicates the cycle of the NMI digital filter sampling clock.

Note 3. t_{IRQCK} indicates the cycle of the IRQi digital filter sampling clock (i = 0 to 7).

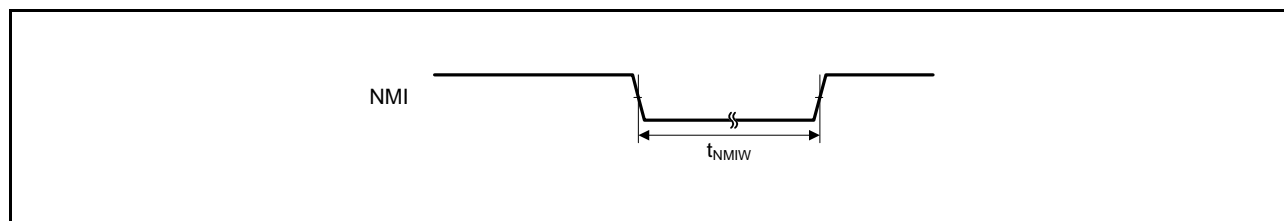


Figure 5.36 NMI Interrupt Input Timing

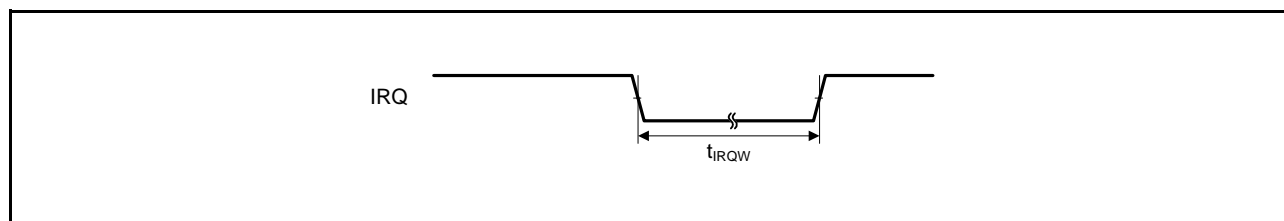


Figure 5.37 IRQ Interrupt Input Timing

5.3.5 Bus Timing

Table 5.34 Bus Timing (1)

Conditions: $2.7\text{ V} \leq V_{CC} = V_{CC_USB} = AV_{CC0} \leq 5.5\text{ V}$, $V_{SS} = AV_{SS0} = V_{SS_USB} = 0\text{ V}$,
 $f_{BCLK} \leq 32\text{ MHz}$ (BCLK pin output frequency $\leq 16\text{ MHz}$), $T_a = -40\text{ to }+105^\circ\text{C}$, $V_{OH} = V_{CC} \times 0.5$, $V_{OL} = V_{CC} \times 0.5$,
 $I_{OH} = -1.0\text{ mA}$, $I_{OL} = 1.0\text{ mA}$, $C_L = 30\text{ pF}$, when normal output is selected by the drive capacity control register

Item	Symbol	Min.	Max.	Unit	Test Conditions
Address delay time	t_{AD}	—	55	ns	Figure 5.38 to Figure 5.41
Byte control delay time	t_{BCD}	—	55	ns	
CS# delay time	t_{CSD}	—	55	ns	
RD# delay time	t_{RSD}	—	55	ns	
Read data setup time	t_{RDS}	40	—	ns	
Read data hold time	t_{RDH}	0	—	ns	
WR# delay time	t_{WRD}	—	55	ns	
Write data delay time	t_{WDD}	—	55	ns	
Write data hold time	t_{WDH}	0	—	ns	
WAIT# setup time	t_{WTS}	40	—	ns	Figure 5.42
WAIT# hold time	t_{WTH}	0	—	ns	

Table 5.35 Bus Timing (2)

Conditions: $1.8\text{ V} \leq V_{CC} = V_{CC_USB} = AV_{CC0} < 2.7\text{ V}$, $V_{SS} = AV_{SS0} = V_{SS_USB} = 0\text{ V}$,
 $f_{BCLK} \leq 16\text{ MHz}$ (BCLK pin output frequency $\leq 8\text{ MHz}$), $T_a = -40\text{ to }+105^\circ\text{C}$, $V_{OH} = V_{CC} \times 0.5$, $V_{OL} = V_{CC} \times 0.5$,
 $I_{OH} = -1.0\text{ mA}$, $I_{OL} = 1.0\text{ mA}$, $C_L = 30\text{ pF}$, when normal output is selected by the drive capacity control register

Item	Symbol	Min.	Max.	Unit	Test Conditions
Address delay time	t_{AD}	—	90	ns	Figure 5.38 to Figure 5.41
Byte control delay time	t_{BCD}	—	90	ns	
CS# delay time	t_{CSD}	—	90	ns	
RD# delay time	t_{RSD}	—	90	ns	
Read data setup time	t_{RDS}	60	—	ns	
Read data hold time	t_{RDH}	0	—	ns	
WR# delay time	t_{WRD}	—	90	ns	
Write data delay time	t_{WDD}	—	90	ns	
Write data hold time	t_{WDH}	0	—	ns	
WAIT# setup time	t_{WTS}	60	—	ns	Figure 5.42
WAIT# hold time	t_{WTH}	0	—	ns	

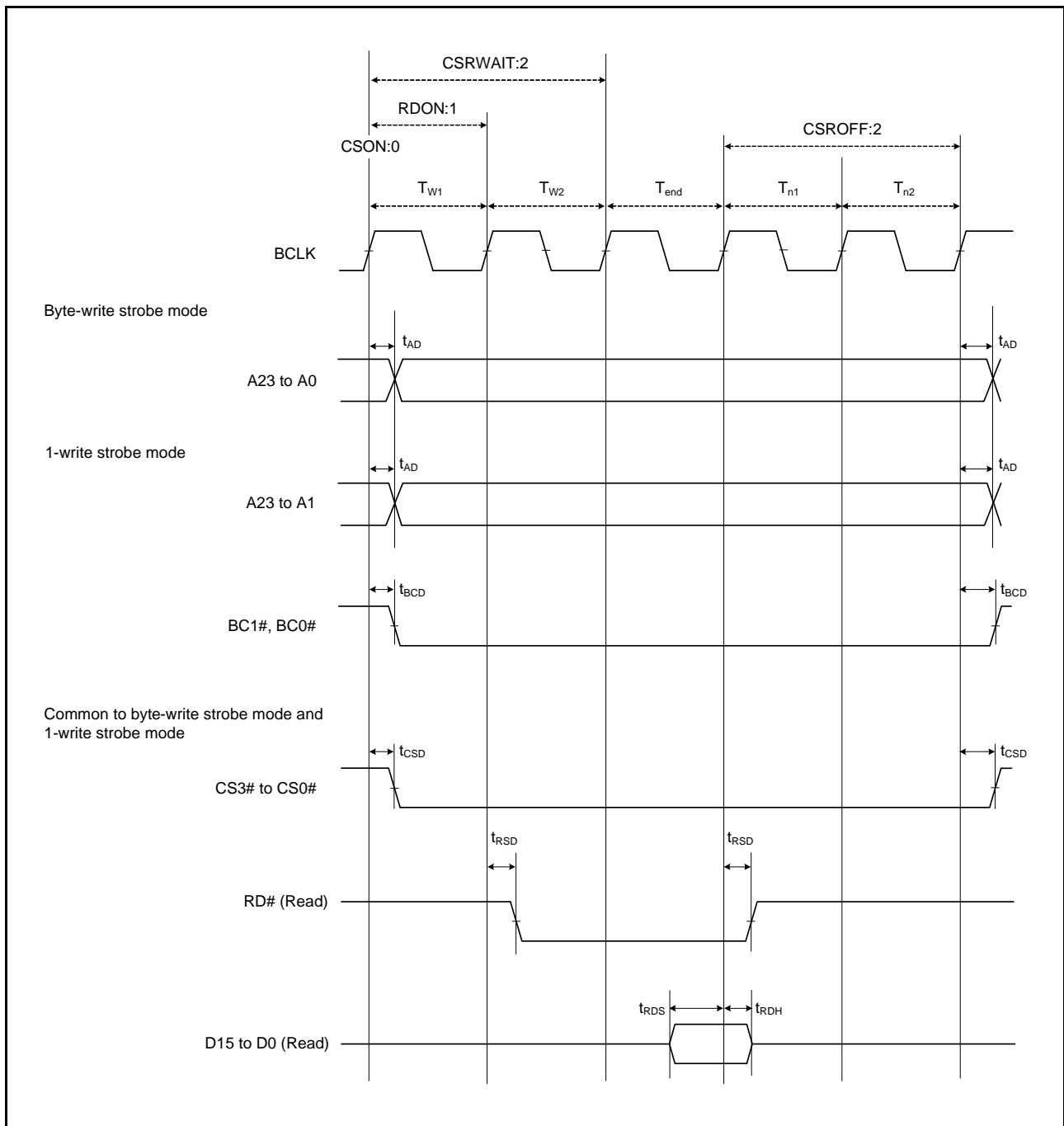


Figure 5.38 External Bus Timing/Normal Read Cycle (Bus Clock Synchronization)

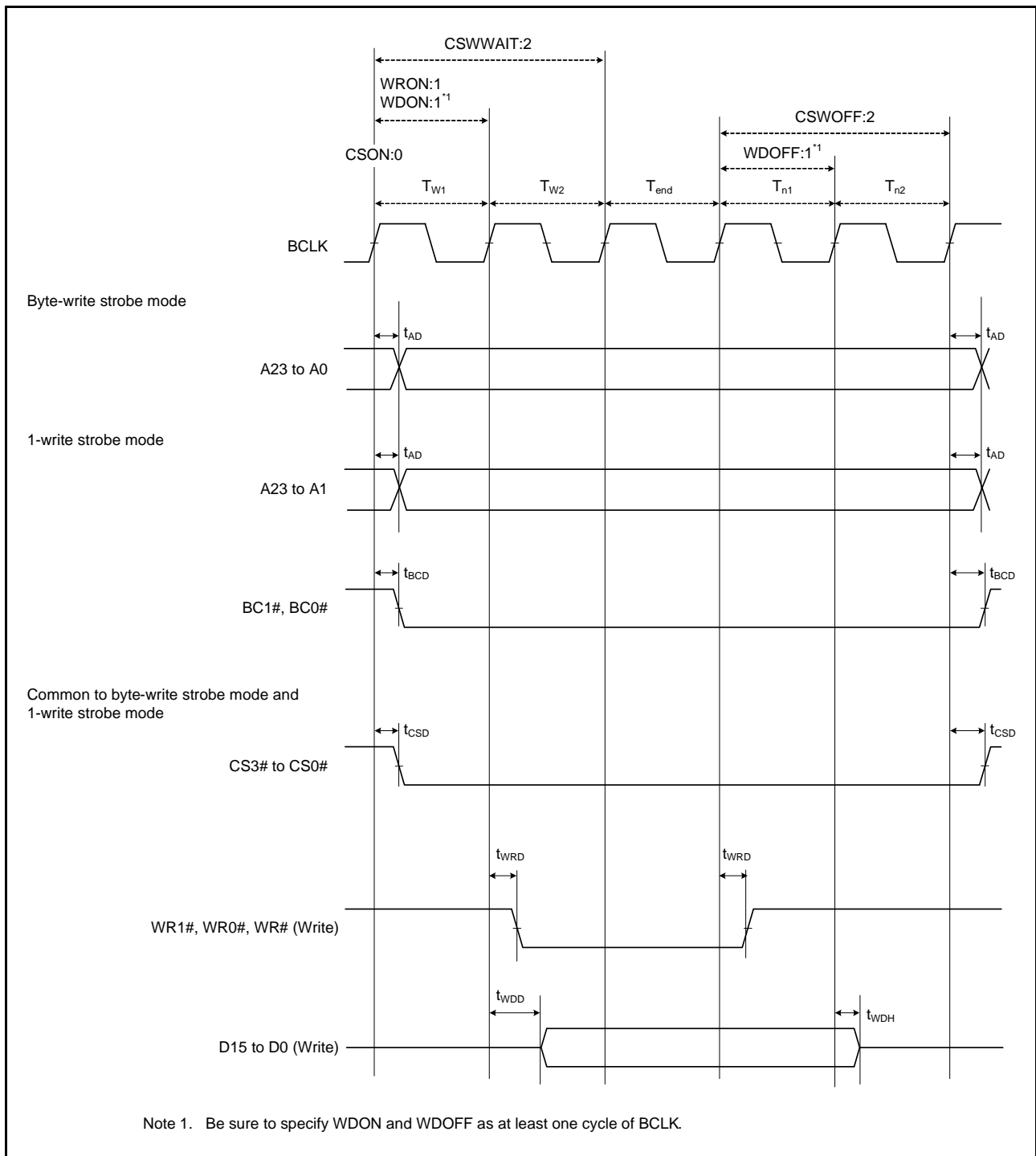


Figure 5.39 External Bus Timing/Normal Write Cycle (Bus Clock Synchronization)

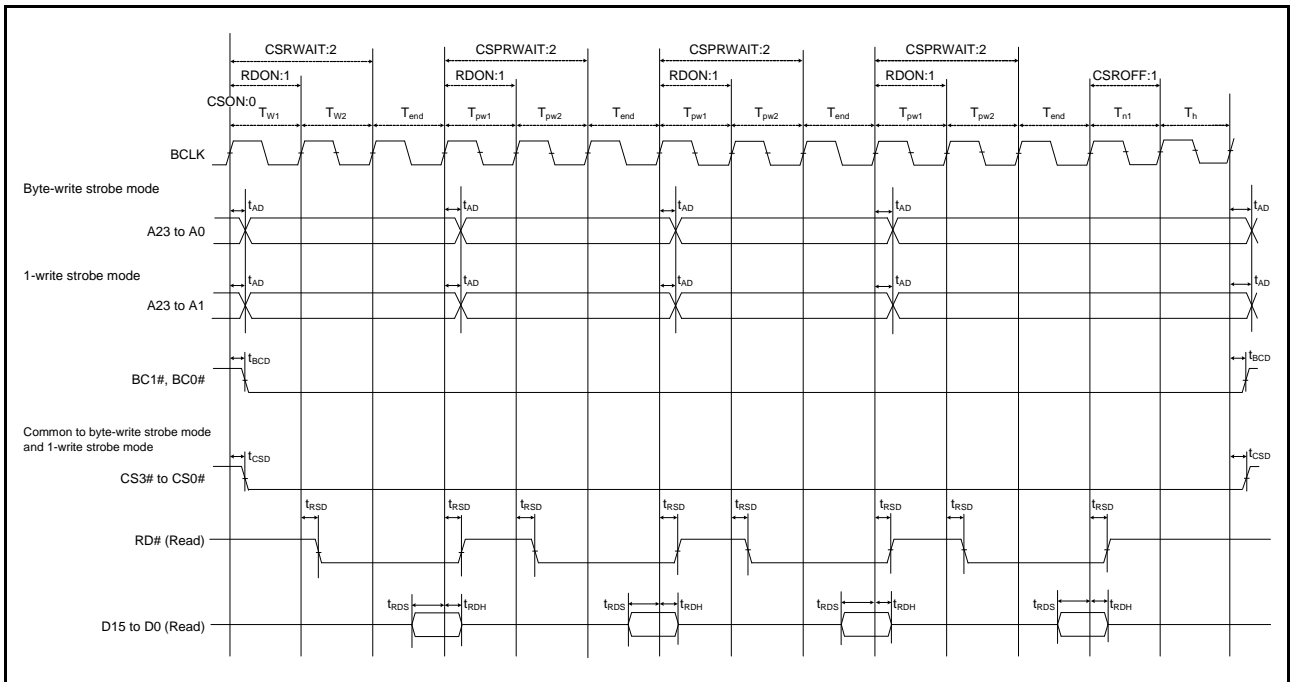


Figure 5.40 External Bus Timing/Page Read Cycle (Bus Clock Synchronization)

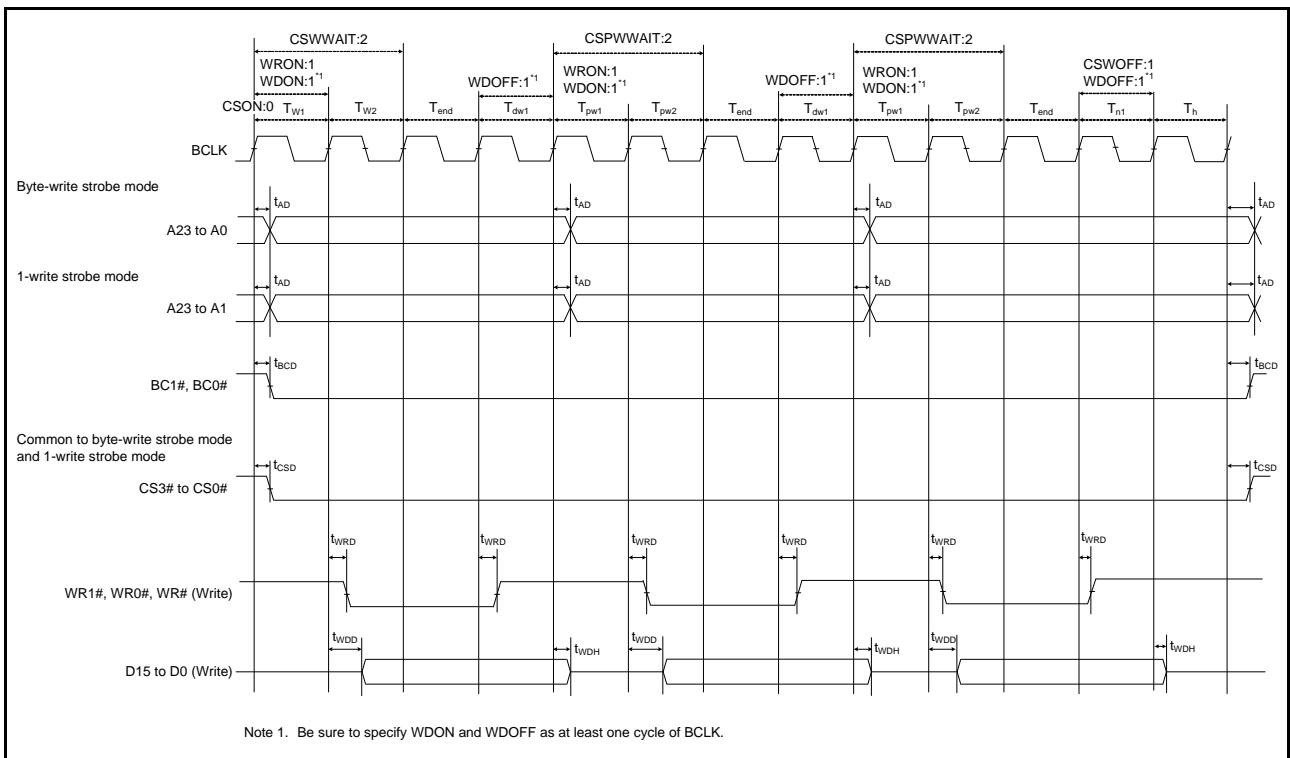


Figure 5.41 External Bus Timing/Page Write Cycle (Bus Clock Synchronization)

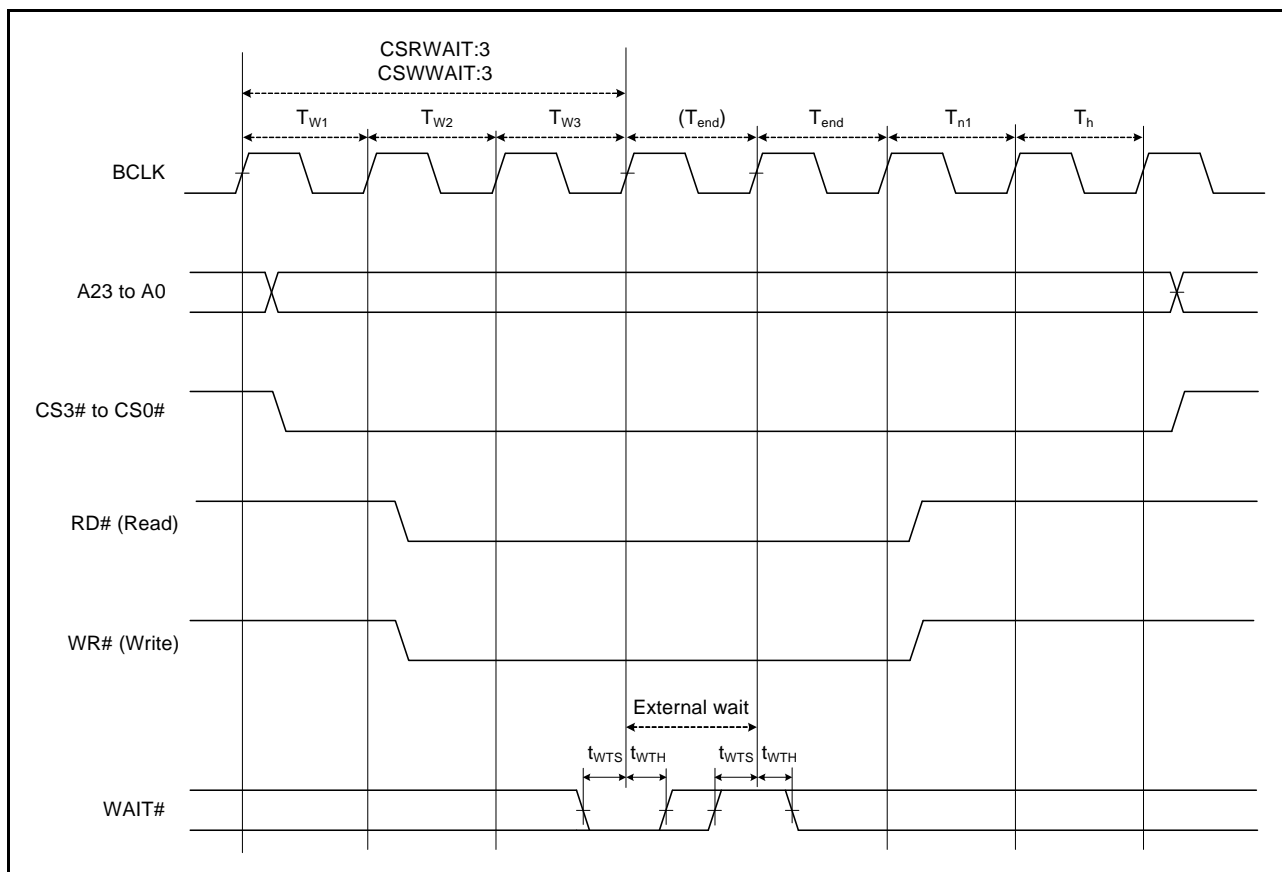


Figure 5.42 External Bus Timing/External Wait Control

Table 5.36 Bus Timing (Multiplex bus) (1)

Conditions: $2.7\text{ V} \leq V_{CC} = V_{CC_USB} = AV_{CC0} \leq 5.5\text{ V}$, $V_{SS} = AV_{SS0} = V_{SS_USB} = 0\text{ V}$,
 $f_{BCLK} \leq 32\text{ MHz}$ (BCLK pin output frequency $\leq 16\text{ MHz}$), $T_a = -40\text{ to }+105^\circ\text{C}$, $V_{OH} = V_{CC} \times 0.5$, $V_{OL} = V_{CC} \times 0.5$,
 $I_{OH} = -1.0\text{ mA}$, $I_{OL} = 1.0\text{ mA}$, $C_L = 30\text{ pF}$, when normal output is selected by the drive capacity control register

Item	Symbol	Min.	Max.	Unit	Test Conditions
Address delay time	t_{AD}	—	55	ns	Figure 5.43, Figure 5.44
Byte control delay time	t_{BCD}	—	55	ns	
CS# delay time	t_{CSD}	—	55	ns	
RD# delay time	t_{RSD}	—	55	ns	
ALE delay time	t_{ALED}	—	55	ns	
Read data setup time	t_{RDS}	40	—	ns	
Read data hold time	t_{RDH}	0	—	ns	
WR# delay time	t_{WRD}	—	55	ns	
Write data delay time	t_{WDD}	—	55	ns	
Write data hold time	t_{WDH}	0	—	ns	
WAIT# setup time	t_{WTS}	40	—	ns	Figure 5.42
WAIT# hold time	t_{WTH}	0	—	ns	

Table 5.37 Bus Timing (Multiplex bus) (2)

Conditions: $1.8\text{ V} \leq V_{CC} = V_{CC_USB} = AV_{CC0} < 5.5\text{ V}$, $V_{SS} = AV_{SS0} = V_{SS_USB} = 0\text{ V}$,
 $f_{BCLK} \leq 16\text{ MHz}$ (BCLK pin output frequency $\leq 8\text{ MHz}$), $T_a = -40\text{ to }+105^\circ\text{C}$, $V_{OH} = V_{CC} \times 0.5$, $V_{OL} = V_{CC} \times 0.5$,
 $I_{OH} = -1.0\text{ mA}$, $I_{OL} = 1.0\text{ mA}$, $C_L = 30\text{ pF}$, when normal output is selected by the drive capacity control register

Item	Symbol	Min.	Max.	Unit	Test Conditions
Address delay time	t_{AD}	—	90	ns	Figure 5.43, Figure 5.44
Byte control delay time	t_{BCD}	—	90	ns	
CS# delay time	t_{CSD}	—	90	ns	
RD# delay time	t_{RSD}	—	90	ns	
ALE delay time	t_{ALED}	—	90	ns	
Read data setup time	t_{RDS}	60	—	ns	
Read data hold time	t_{RDH}	0	—	ns	
WR# delay time	t_{WRD}	—	90	ns	
Write data delay time	t_{WDD}	—	90	ns	
Write data hold time	t_{WDH}	0	—	ns	
WAIT# setup time	t_{WTS}	60	—	ns	Figure 5.42
WAIT# hold time	t_{WTH}	0	—	ns	

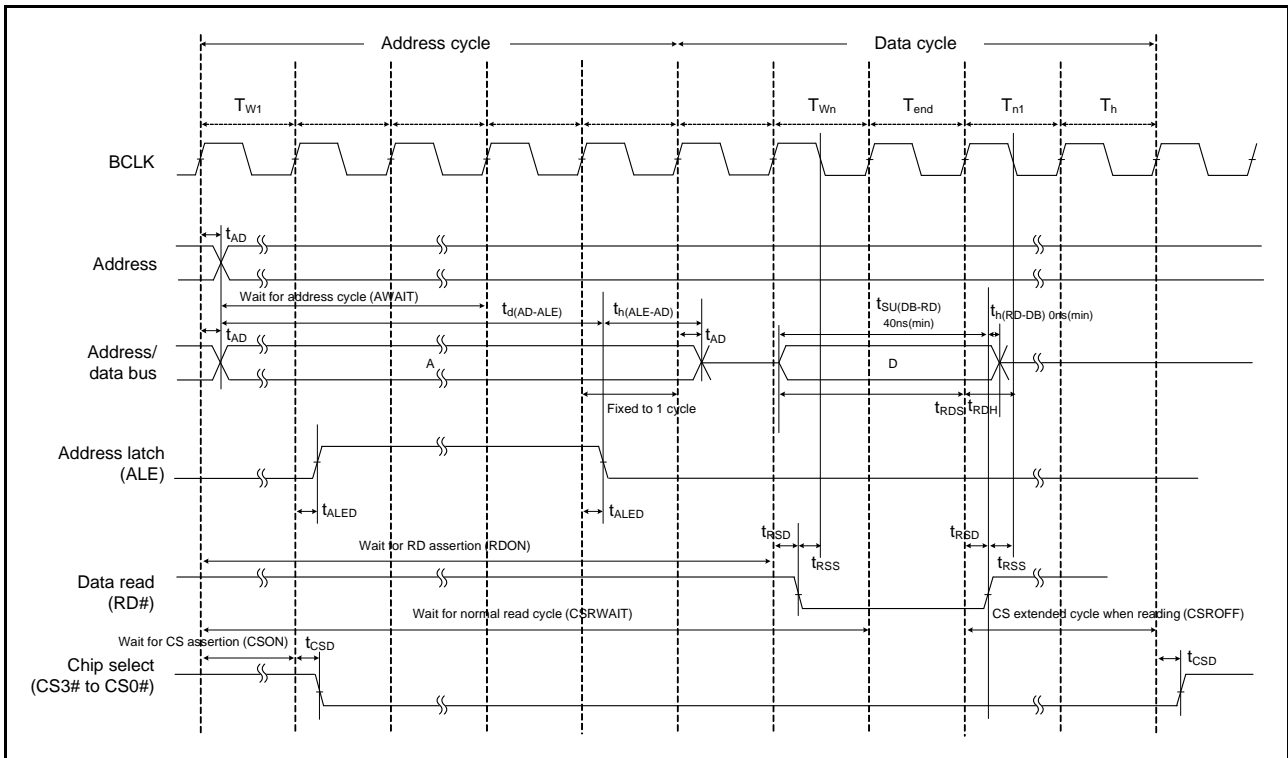


Figure 5.43 External Bus Timing/Read Access Operation Example (Multiplex)

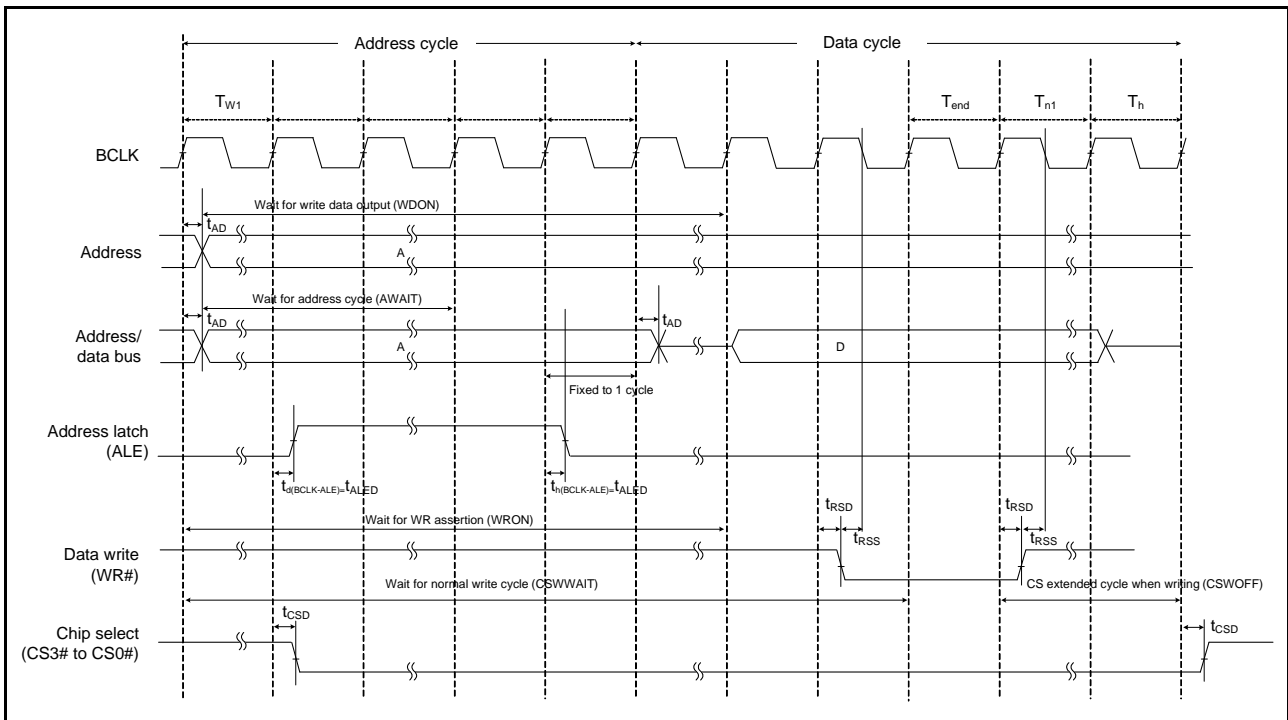


Figure 5.44 External Bus Timing/Write Access Operation Example (Multiplex)

5.3.6 Timing of On-Chip Peripheral Modules

Table 5.38 Timing of On-Chip Peripheral Modules (1)Conditions: $1.8\text{ V} \leq VCC = VCC_USB = AVCC0 \leq 5.5\text{ V}$, $VSS = AVSS0 = VSS_USB = 0\text{ V}$, $T_a = -40\text{ to }+105^\circ\text{C}$

Item			Symbol	Min.	Max.	Unit ^{*1}	Test Conditions	
I/O ports	Input data pulse width		t_{PRW}	1.5	—	t_{Pcyc}	Figure 5.45	
MTU2/TPU	Input capture input pulse width	Single-edge setting	t_{TICW}	1.5	—	t_{Pcyc}	Figure 5.46	
		Both-edge setting		2.5	—			
	Timer clock pulse width	Single-edge setting	t_{TCKWH} , t_{TCKWL}	1.5	—	t_{Pcyc}	Figure 5.47	
Both-edge setting		2.5		—				
Phase counting mode		2.5		—				
POE2	POE# input pulse width		t_{POEW}	1.5	—	t_{Pcyc}	Figure 5.48	
TMR	Timer clock pulse width	Single-edge setting	t_{TMCWH} , t_{TMCWL}	1.5	—	t_{Pcyc}	Figure 5.49	
		Both-edge setting		2.5	—			
SCI	Input clock cycle time	Asynchronous	t_{Scyc}	4	—	t_{Pcyc}	Figure 5.50	
		Clock synchronous		6	—			
	Input clock pulse width		t_{SCKW}	0.4	0.6	t_{Scyc}		
	Input clock rise time		t_{SCKr}	—	20	ns		
	Input clock fall time		t_{SCKf}	—	20	ns		
	Output clock cycle time	Asynchronous	t_{Scyc}	16	—	t_{Pcyc}	Figure 5.51	
		Clock synchronous		4	—			
	Output clock pulse width		t_{SCKW}	0.4	0.6	t_{Scyc}		
	Output clock rise time		t_{SCKr}	—	20	ns		
	Output clock fall time		t_{SCKf}	—	20	ns		
	Transmit data delay time (master)	Clock synchronous		t_{TXD}	—	40	ns	
		Transmit data delay time (slave)	Clock synchronous		2.7 V or above	—	65	ns
	1.8 V or above			—	100	ns		
	Receive data setup time (master)	Clock synchronous	2.7 V or above	t_{RXS}	65	—	ns	
1.8 V or above			90		—	ns		
Receive data setup time (slave)	Clock synchronous		t_{RXS}	40	—	ns		
Receive data hold time	Clock synchronous		t_{RXH}	40	—	ns		
A/D converter	Trigger input pulse width		t_{TRGW}	1.5	—	t_{Pcyc}	Figure 5.52	
CAC	CACREF input pulse width	$t_{Pcyc} \leq t_{cac}^2$	t_{CACREF}	$4.5 t_{cac} + 3 t_{Pcyc}$	—	ns		
		$t_{Pcyc} > t_{cac}^2$		$5 t_{cac} + 6.5 t_{Pcyc}$				
CLKOUT	CLKOUT pin output cycle ^{*4}	VCC = 2.7 V or above	t_{Cyc}	62.5	—	ns	Figure 5.53	
		VCC = 1.8 V or above		125				
	CLKOUT pin high pulse width ^{*3}	VCC = 2.7 V or above	t_{CH}	15	—	ns		
		VCC = 1.8 V or above		30				
	CLKOUT pin low pulse width ^{*3}	VCC = 2.7 V or above	t_{CL}	15	—	ns		
		VCC = 1.8 V or above		30				
	CLKOUT pin output rise time	VCC = 2.7 V or above	t_{Cr}	—	12	ns		
		VCC = 1.8 V or above		25				
	CLKOUT pin output fall time	VCC = 2.7 V or above	t_{Cf}	—	12	ns		
		VCC = 1.8 V or above		25				

Note 1. t_{Pcyc} : PCLK cycleNote 2. t_{cac} : CAC count clock source cycle

Note 3. When the LOCO is selected as the clock output source (the CKOCR.CKOSEL[2:0] bits are 000b), set the clock output division ratio selection to divided by 2 (the CKOCR.CKODIV[2:0] bits are 001b).

Note 4. When the EXTAL external clock input or an oscillator is used with divided by 1 (the CKOCR.CKOSEL[2:0] bits are 010b and the CKOCR.CKODIV[2:0] bits are 000b) to output from CLKOUT, the above should be satisfied with an input duty cycle of 45 to 55%.

Table 5.39 Timing of On-Chip Peripheral Modules (2)

Conditions: $1.8\text{ V} \leq V_{CC} = V_{CC_USB} = AV_{CC0} \leq 5.5\text{ V}$, $V_{SS} = AV_{SS0} = V_{SS_USB} = 0\text{ V}$, $T_a = -40\text{ to }+105^\circ\text{C}$, $C = 30\text{ pF}$, when high-drive output is selected by the drive capacity control register

Item		Symbol	Min.	Max.	Unit	Test Conditions		
RSPI	RSPCK clock cycle	Master	t_{SPCyc}	2	4096	t_{PCyc}^{*1}	Figure 5.54	
		Slave		8	4096			
RSPCK clock high pulse width	Master	t_{SPCKWH}	$(t_{SPCyc} - t_{SPCKr} - t_{SPCKf})/2 - 3$	—	ns			
	Slave		$(t_{SPCyc} - t_{SPCKr} - t_{SPCKf})/2$	—				
RSPCK clock low pulse width	Master	t_{SPCKWL}	$(t_{SPCyc} - t_{SPCKr} - t_{SPCKf})/2 - 3$	—	ns			
	Slave		$(t_{SPCyc} - t_{SPCKr} - t_{SPCKf})/2$	—				
RSPCK clock rise/fall time	Output	2.7 V or above	t_{SPCKr}	—	10	ns		
		1.8 V or above	t_{SPCKf}	—	15			
	Input			—	1	μs		
Data input setup time	Master	2.7 V or above	t_{SU}	10	—	ns		Figure 5.55 to Figure 5.58
		1.8 V or above		30	—			
	Slave			$25 - t_{PCyc}$	—			
Data input hold time	Master	RSPCK set to a division ratio other than PCLKB divided by 2	t_H	t_{PCyc}	—	ns		
		RSPCK set to PCLKB divided by 2	t_{HF}	0	—			
	Slave		t_H	$20 + 2 \times t_{PCyc}$	—			
SSL setup time	Master		t_{LEAD}	$-30 + N^2 \times t_{SPCyc}$	—	ns		
	Slave			2	—	t_{PCyc}		
SSL hold time	Master		t_{LAG}	$-30 + N^3 \times t_{SPCyc}$	—	ns		
	Slave			2	—	t_{PCyc}		
Data output delay time	Master	2.7 V or above	t_{OD}	—	14	ns		
		1.8 V or above		—	30			
	Slave	2.7 V or above		—	$3 \times t_{PCyc} + 65$			
		1.8 V or above		—	$3 \times t_{PCyc} + 105$			
Data output hold time	Master		t_{OH}	0	—	ns		
	Slave			0	—			
Successive transmission delay time	Master		t_{TD}	$t_{SPCyc} + 2 \times t_{PCyc}$	$8 \times t_{SPCyc} + 2 \times t_{PCyc}$	ns		
	Slave			$4 \times t_{PCyc}$	—			
MOSI and MISO rise/fall time	Output	2.7 V or above	t_{Dr}, t_{Df}	—	10	ns		
		1.8 V or above		—	15			
	Input			—	1	μs		
SSL rise/fall time	Output	2.7 V or above	t_{SSLr}	—	10	ns		
		1.8 V or above	t_{SSLf}	—	15	ns		
	Input			—	1	μs		
Slave access time	2.7 V or above	t_{SA}	—	6	t_{PCyc}	Figure 5.57, Figure 5.58		
	1.8 V or above		—	7				
Slave output release time	2.7 V or above	t_{REL}	—	5	t_{PCyc}			
	1.8 V or above		—	6				

Note 1. t_{PCyc} : PCLK cycle

Note 2. N: An integer from 1 to 8 that can be set by the RSPI clock delay register (SPCKD)

Note 3. N: An integer from 1 to 8 that can be set by the RSPI slave select negation delay register (SSLND)

Table 5.40 Timing of On-Chip Peripheral Modules (3)Conditions: $1.8\text{ V} \leq VCC = VCC_USB = AVCC0 \leq 5.5\text{ V}$, $VSS = AVSS0 = VSS_USB = 0\text{ V}$, $T_a = -40\text{ to }+105^\circ\text{C}$

Item		Symbol	Min.	Max.	Unit*1	Test Conditions	
Simple SPI	SCK clock cycle output (master)	t_{SPCyc}	4	65536	t_{PCyc}	Figure 5.54	
	SCK clock cycle input (slave)		6	65536	t_{PCyc}		
	SCK clock high pulse width	t_{SPCKWH}	0.4	0.6	t_{SPCyc}		
	SCK clock low pulse width	t_{SPCKWL}	0.4	0.6	t_{SPCyc}		
	SCK clock rise/fall time	t_{SPCKr}, t_{SPCKf}	—	20	ns		
	Data input setup time (master)	2.7 V or above	t_{SU}	65	—	ns	Figure 5.55, Figure 5.56
		1.8 V or above		95	—		
	Data input setup time (slave)	40		—			
	Data input hold time	t_H	40	—	ns		
	SSL input setup time	t_{LEAD}	3	—	t_{SPCyc}		
	SSL input hold time	t_{LAG}	3	—	t_{SPCyc}		
	Data output delay time (master)	t_{OD}	—	40	ns		
	Data output delay time (slave)		2.7 V or above	—		65	
			1.8 V or above	—		100	
	Data output hold time (master)	2.7 V or above	t_{OH}	-10	—	ns	
		1.8 V or above		-20	—		
Data output hold time (slave)	-10	—					
Data rise/fall time	t_{Dr}, t_{Df}	—	20	ns			
SSL input rise/fall time	t_{SSLr}, t_{SSLf}	—	20	ns			
Slave access time	t_{SA}	—	6	t_{PCyc}	Figure 5.57, Figure 5.58		
Slave output release time	t_{REL}	—	6	t_{PCyc}			

Note 1. t_{PCyc} : PCLK cycle

Table 5.41 Timing of On-Chip Peripheral Modules (4)

Conditions: $2.7\text{ V} \leq V_{CC} = V_{CC_USB} = AV_{CC0} \leq 5.5\text{ V}$, $V_{SS} = AV_{SS0} = V_{SS_USB} = 0\text{ V}$, $f_{PCLKB} \leq 32\text{ MHz}$,
 $T_a = -40\text{ to }+105^\circ\text{C}$

Item	Symbol	Min. *1, *2	Max.	Unit	Test Conditions	
RIIC (Standard mode, SMBus)	SCL cycle time	t_{SCL}	$6 (12) \times t_{IICcyc} + 1300$	—	ns	Figure 5.59
	SCL high pulse width	t_{SCLH}	$3 (6) \times t_{IICcyc} + 300$	—	ns	
	SCL low pulse width	t_{SCLL}	$3 (6) \times t_{IICcyc} + 300$	—	ns	
	SCL, SDA rise time	t_{Sr}	—	1000	ns	
	SCL, SDA fall time	t_{Sf}	—	300	ns	
	SCL, SDA spike pulse removal time	t_{SP}	0	$1 (4) \times t_{IICcyc}$	ns	
	SDA bus free time	t_{BUF}	$3 (6) \times t_{IICcyc} + 300$	—	ns	
	START condition hold time	t_{STAH}	$t_{IICcyc} + 300$	—	ns	
	Repeated START condition setup time	t_{STAS}	1000	—	ns	
	STOP condition setup time	t_{STOS}	1000	—	ns	
	Data setup time	t_{SDAS}	$t_{IICcyc} + 50$	—	ns	
	Data hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b	—	400	pF	
RIIC (Fast mode)	SCL cycle time	t_{SCL}	$6 (12) \times t_{IICcyc} + 600$	—	ns	Figure 5.59
	SCL high pulse width	t_{SCLH}	$3 (6) \times t_{IICcyc} + 300$	—	ns	
	SCL low pulse width	t_{SCLL}	$3 (6) \times t_{IICcyc} + 300$	—	ns	
	SCL, SDA rise time	t_{Sr}	—	300	ns	
	SCL, SDA fall time	t_{Sf}	—	300	ns	
	SCL, SDA spike pulse removal time	t_{SP}	0	$1 (4) \times t_{IICcyc}$	ns	
	SDA bus free time	t_{BUF}	$3 (6) \times t_{IICcyc} + 300$	—	ns	
	START condition hold time	t_{STAH}	$t_{IICcyc} + 300$	—	ns	
	Repeated START condition setup time	t_{STAS}	300	—	ns	
	STOP condition setup time	t_{STOS}	300	—	ns	
	Data setup time	t_{SDAS}	$t_{IICcyc} + 50$	—	ns	
	Data hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b	—	400	pF	

Note: t_{IICcyc} : RIIC internal reference clock (IIC ϕ) cycle

Note 1. The value in parentheses is used when the ICMR3.NF[1:0] bits are set to 11b while a digital filter is enabled with the ICFER.NFE bit = 1.

Note 2. C_b is the total capacitance of the bus lines.

Table 5.42 Timing of On-Chip Peripheral Modules (5)

Conditions: $2.7\text{ V} \leq VCC = VCC_USB = AVCC0 \leq 5.5\text{ V}$, $VSS = AVSS0 = VSS_USB = 0\text{ V}$, $fPCLKB \leq 32\text{ MHz}$,
 $T_a = -40\text{ to }+105^\circ\text{C}$

Item		Symbol	Min.*1	Max.	Unit	Test Conditions
Simple I ² C (Standard mode)	SDA rise time	t_{Sr}	—	1000	ns	Figure 5.59
	SDA fall time	t_{Sf}	—	300	ns	
	SDA spike pulse removal time	t_{SP}	0	$4 \times t_{Pcyc}$	ns	
	Data setup time	t_{SDAS}	250	—	ns	
	Data hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b	—	400	pF	
Simple I ² C (Fast mode)	SDA rise time	t_{Sr}	—	300	ns	Figure 5.59
	SDA fall time	t_{Sf}	—	300	ns	
	SDA spike pulse removal time	t_{SP}	0	$4 \times t_{Pcyc}$	ns	
	Data setup time	t_{SDAS}	100	—	ns	
	Data hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b	—	400	pF	

Note: t_{Pcyc} : PCLK cycle

Note 1. C_b is the total capacitance of the bus lines.

Table 5.43 Timing of On-Chip Peripheral Modules (6)

Conditions: $1.8\text{ V} \leq VCC = VCC_USB = AVCC0 \leq 5.5\text{ V}$, $VSS = AVSS0 = VSS_USB = 0\text{ V}$, $fPCLKB \leq 32\text{ MHz}$,
 $T_a = -40\text{ to }+105^\circ\text{C}$

Item		Symbol	Min.	Max.	Unit	Test Conditions	
SSI	AUDIO_MCLK input frequency	t_{AUDIO}	2.7 V or above	1	25	MHz	Figure 5.60 Figure 5.61 Figure 5.62 Figure 5.63
			1.8 V or above	1	4		
	Output clock cycle		t_O	250	—	ns	
	Input clock cycle		t_I	250	—	ns	
	Clock high level		t_{HC}	0.4	0.6	to, ti	
	Clock low level		t_{LC}	0.4	0.6	to, ti	
	Clock rise time		t_{RC}	—	20	ns	
	Data delay time	2.7 V or above	t_{DTR}	—	65	ns	
		1.8 V or above		—	105		
	Setup time	2.7 V or above	t_{SR}	65	—	ns	
		1.8 V or above		90	—		
	Hold time		t_{HTR}	40	—	ns	
WS changing edge SSIDATA output delay		t_{DTRW}	—	105	ns		

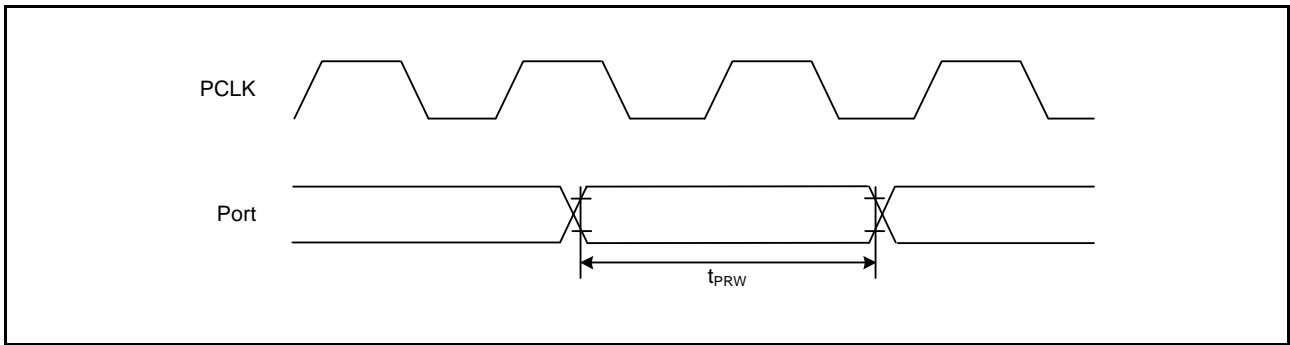


Figure 5.45 I/O Port Input Timing

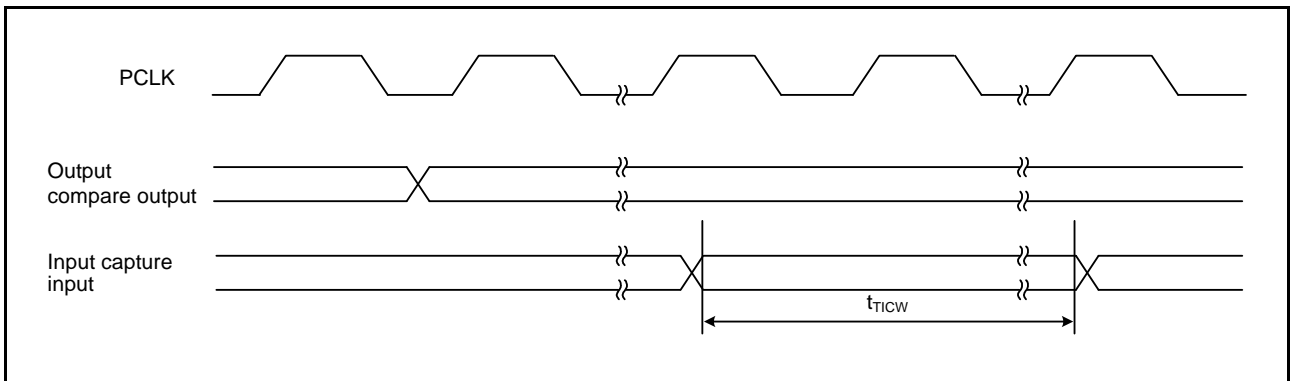


Figure 5.46 MTU2 Input/Output Timing

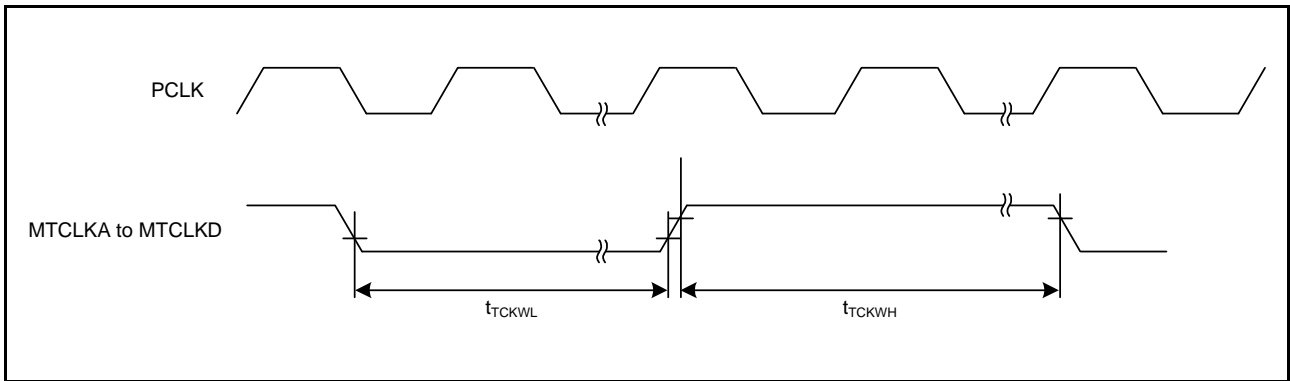


Figure 5.47 MTU2 Clock Input Timing

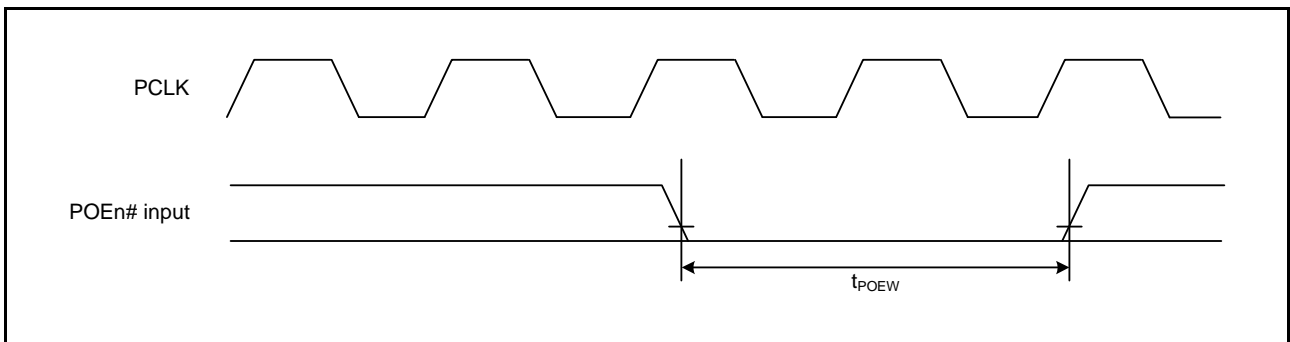


Figure 5.48 POE# Input Timing

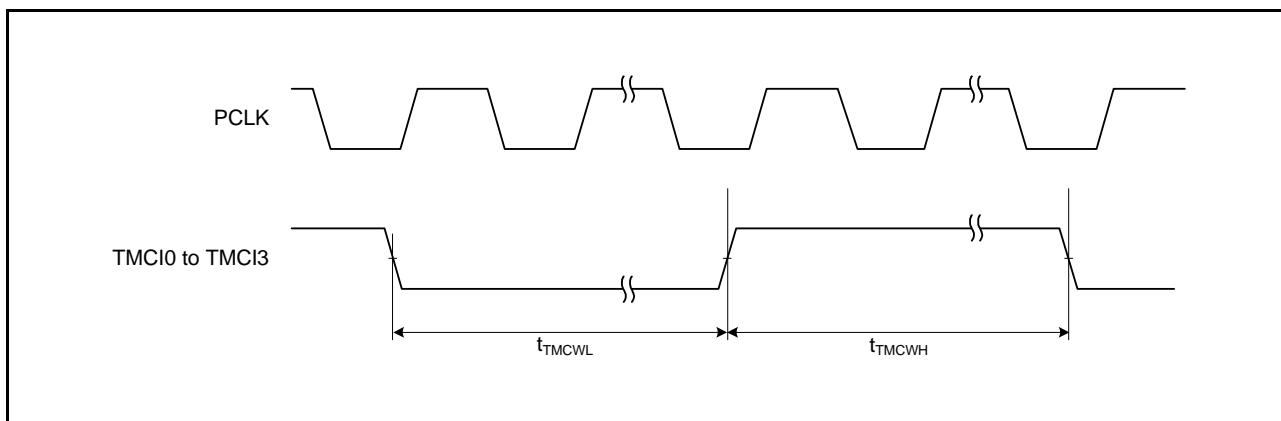


Figure 5.49 TMR Clock Input Timing

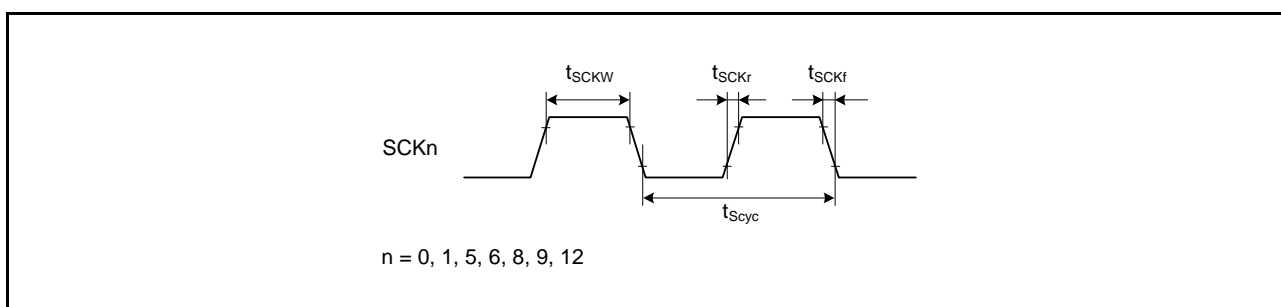


Figure 5.50 SCK Clock Input Timing

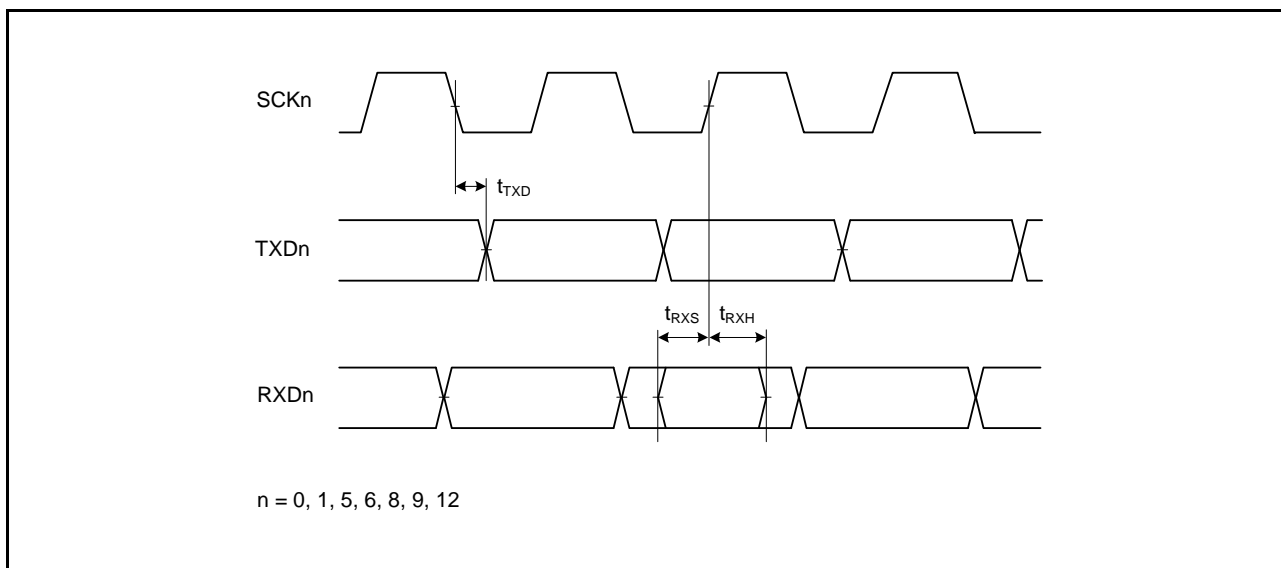


Figure 5.51 SCI Input/Output Timing: Clock Synchronous Mode

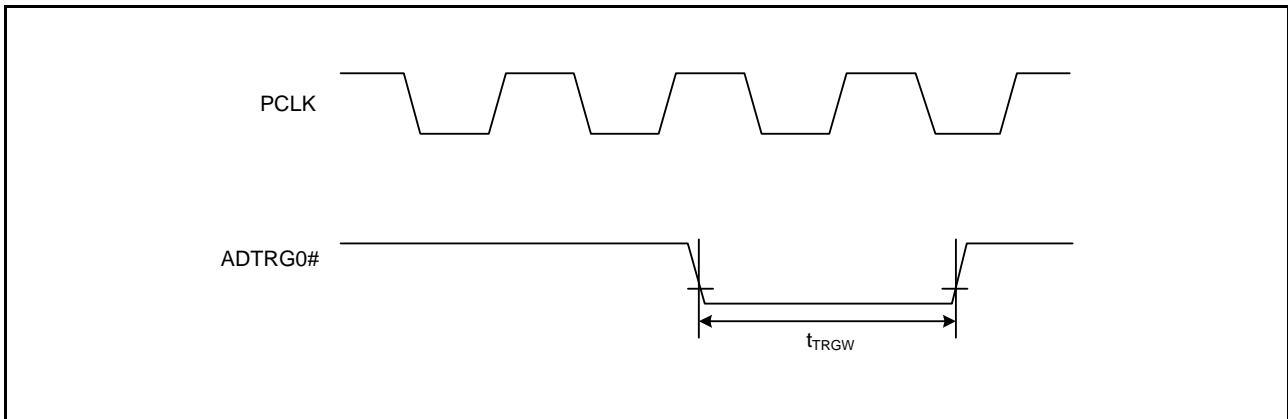


Figure 5.52 A/D Converter External Trigger Input Timing

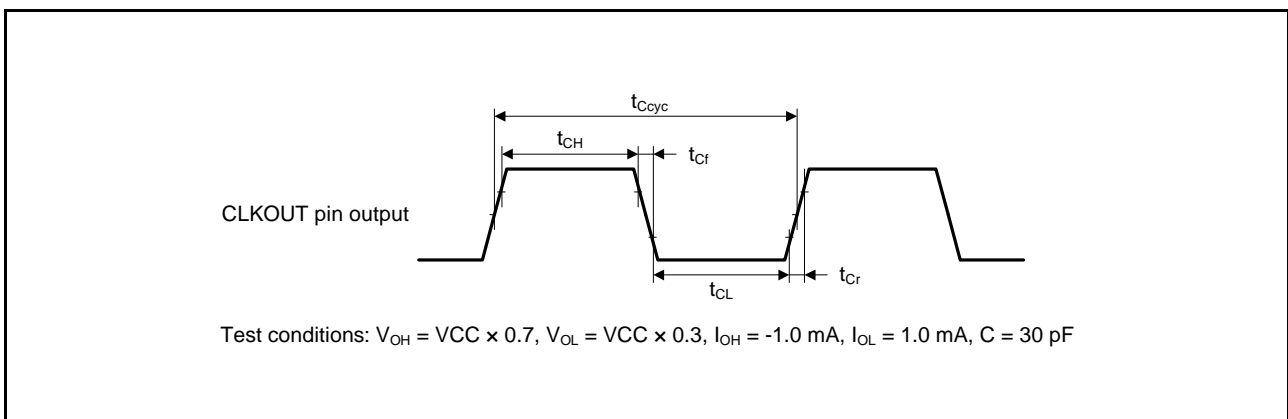


Figure 5.53 CLKOUT Output Timing

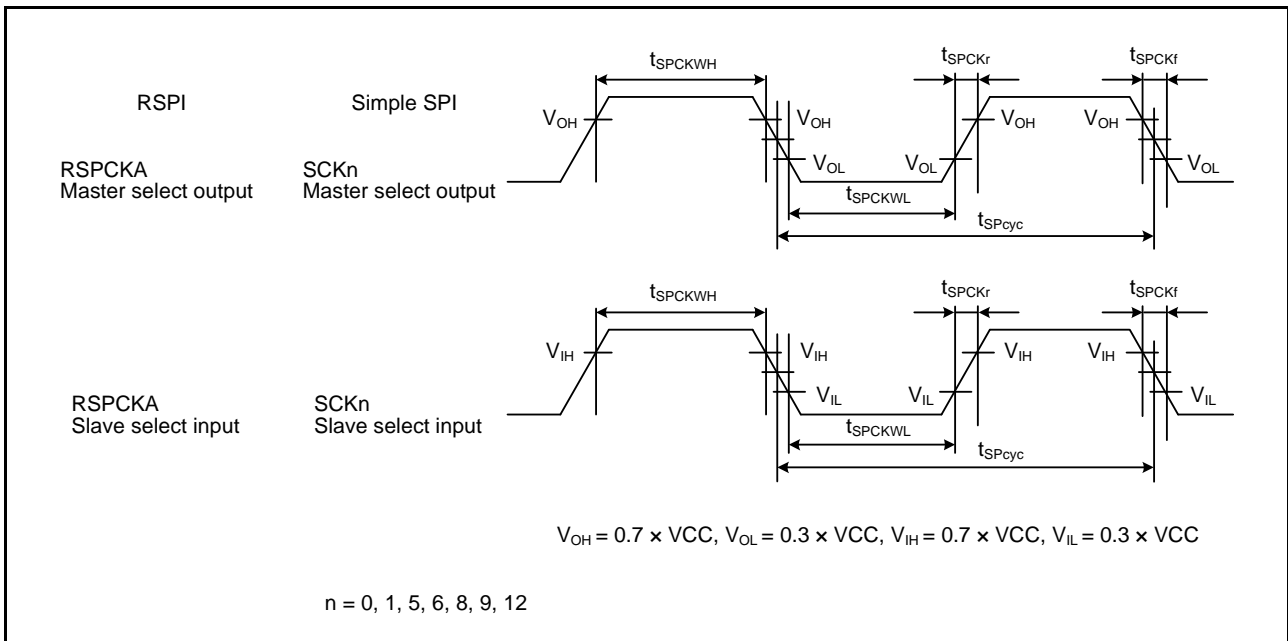


Figure 5.54 RSPi Clock Timing and Simple SPI Clock Timing

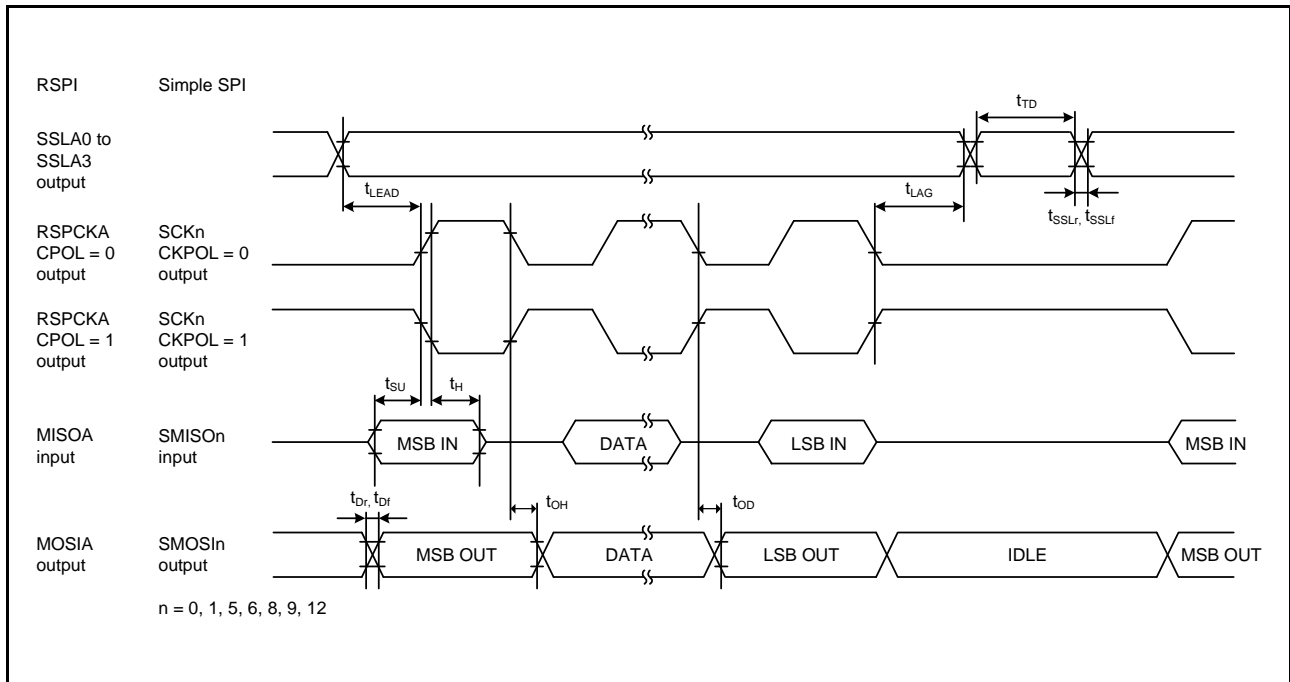


Figure 5.55 RSPI Timing (Master, CPHA = 0) and Simple SPI Clock Timing (Master, CKPH = 1)

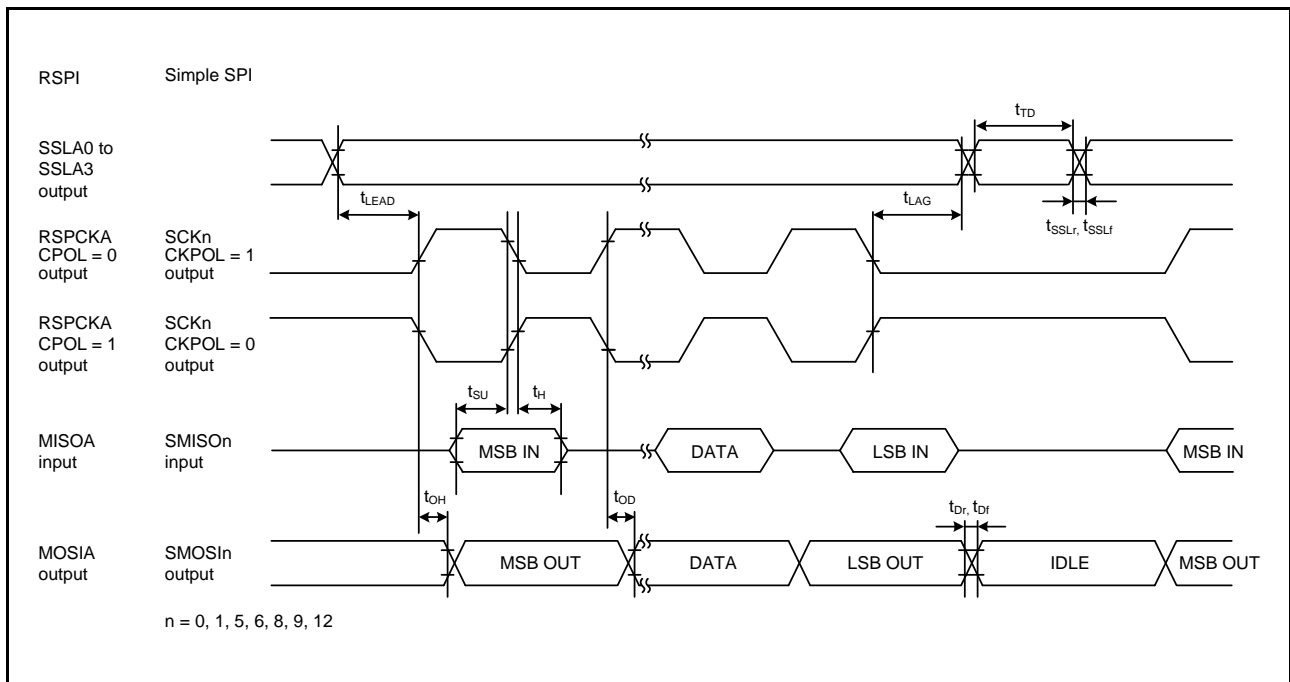


Figure 5.56 RSPI Timing (Master, CPHA = 1) and Simple SPI Clock Timing (Master, CKPH = 0)

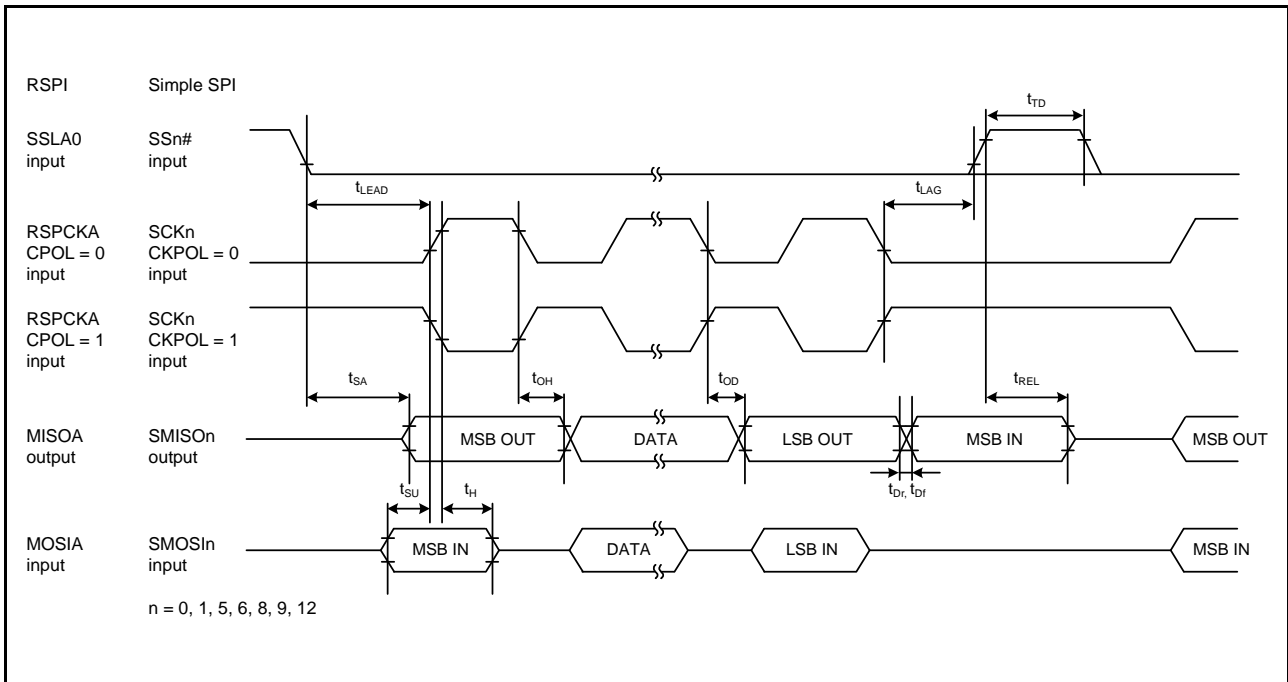


Figure 5.57 RSPI Timing (Slave, CPHA = 0) and Simple SPI Clock Timing (Slave, CKPH = 1)

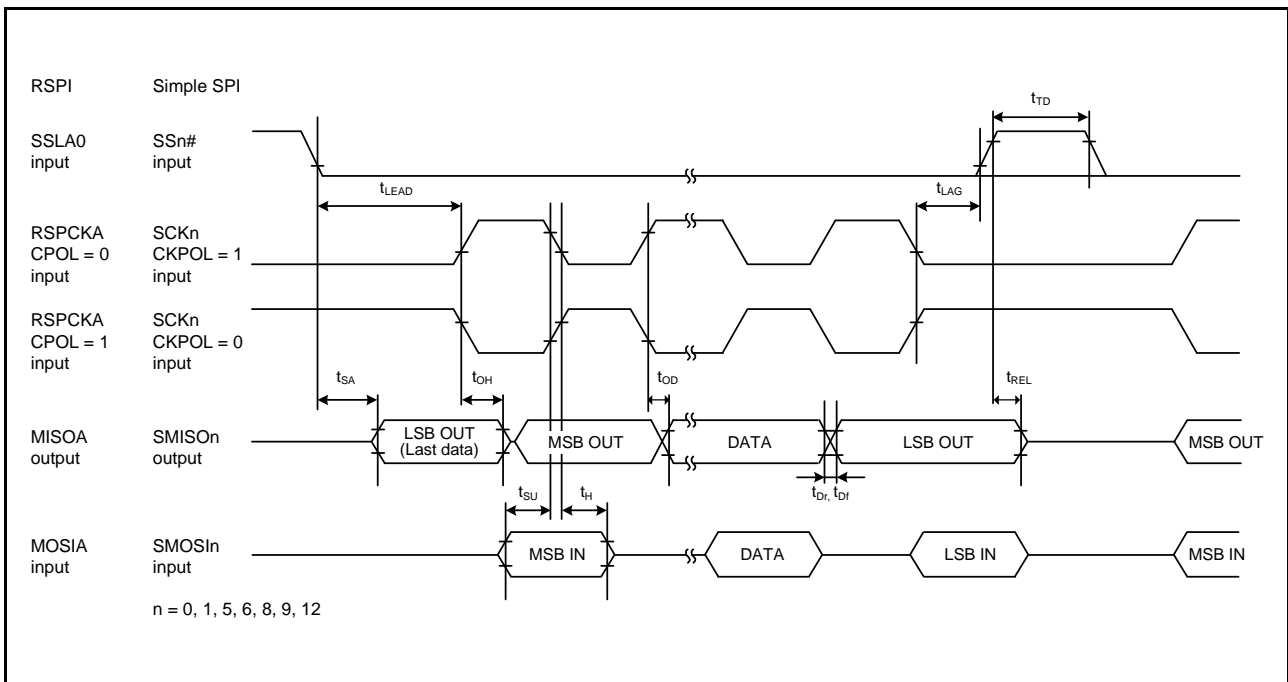


Figure 5.58 RSPI Timing (Slave, CPHA = 1) and Simple SPI Clock Timing (Slave, CKPH = 0)

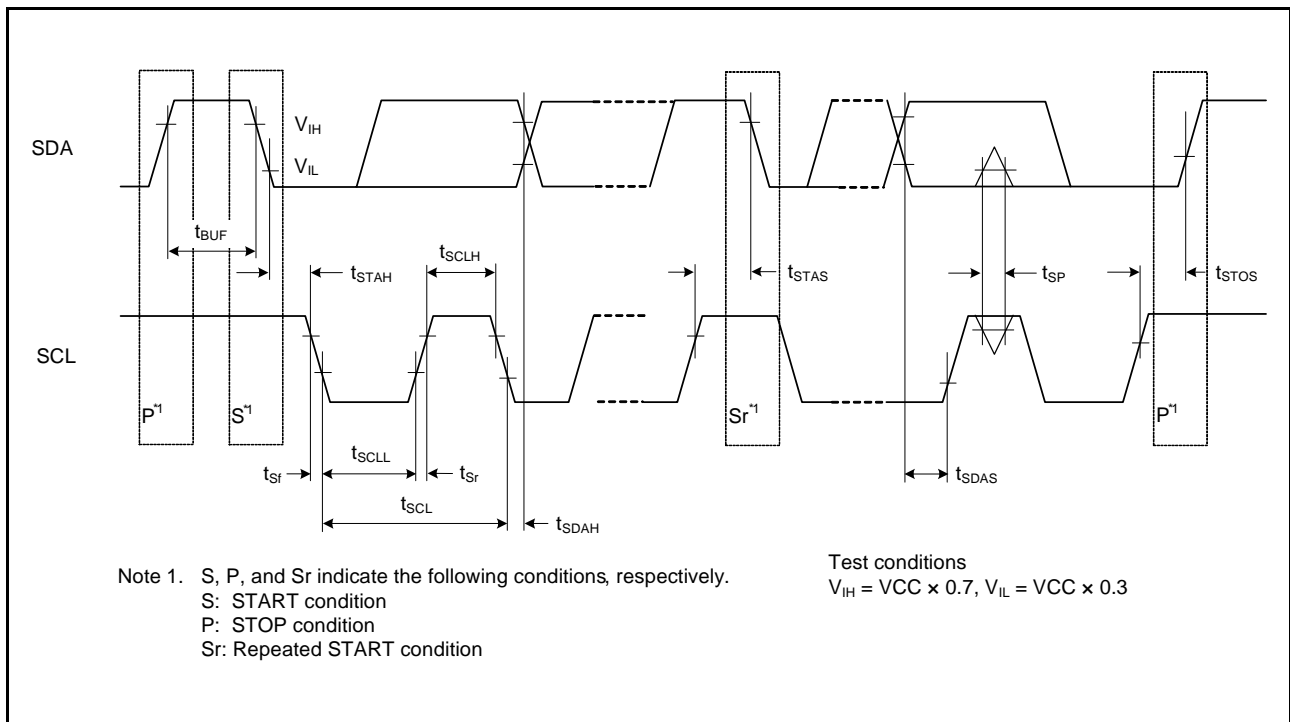


Figure 5.59 RIIC Bus Interface Input/Output Timing and Simple I²C Bus Interface Input/Output Timing

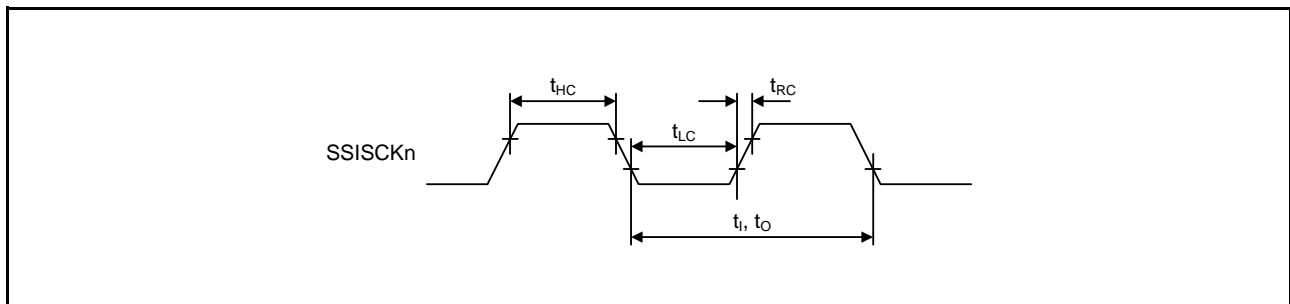


Figure 5.60 SSI Clock Input/Output Timing

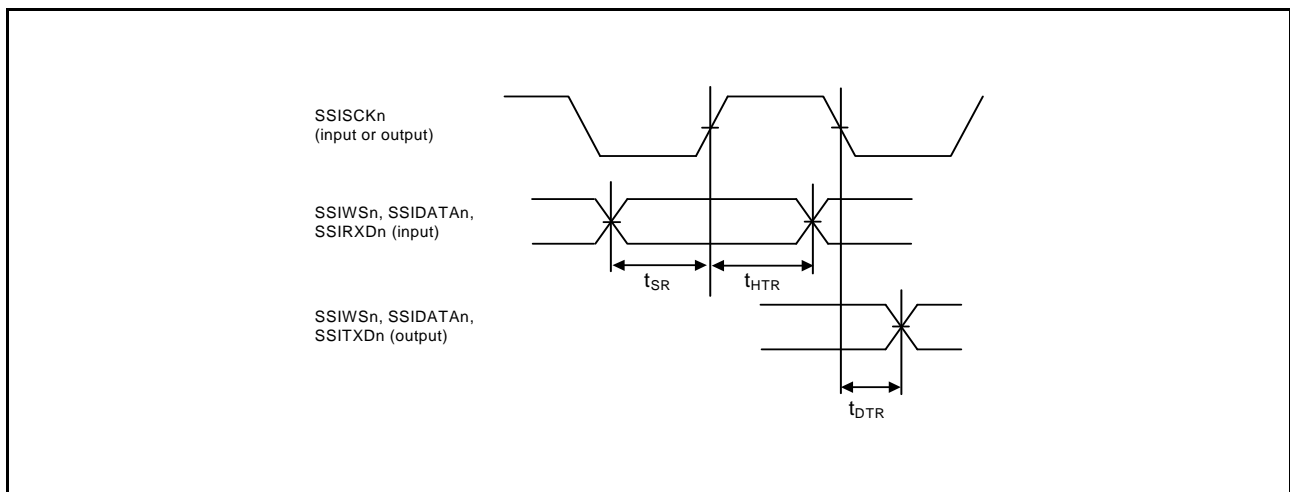


Figure 5.61 SSI Transmission/Reception Timing (SSICR.SCKP=0)

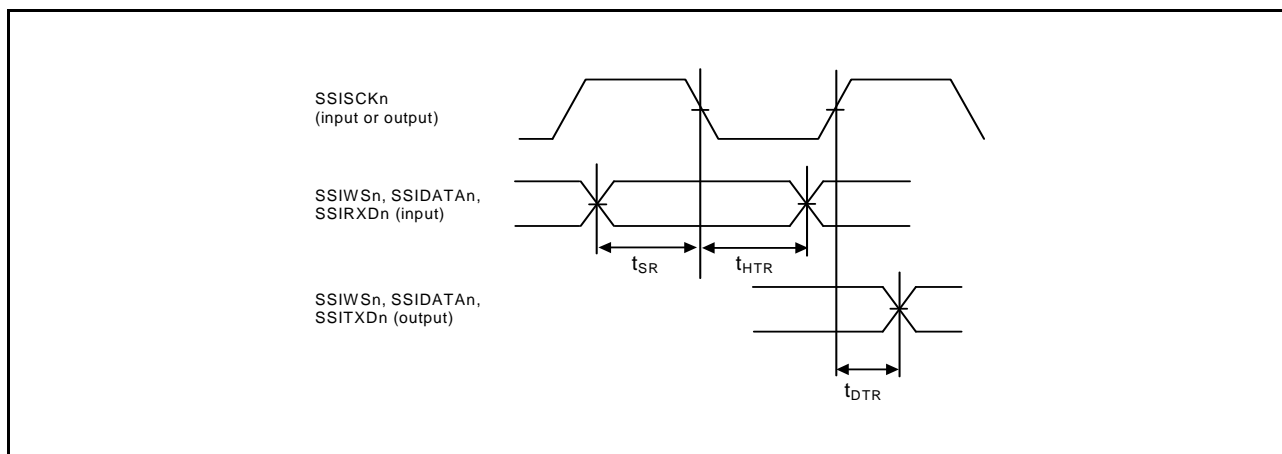


Figure 5.62 SSI Transmission/Reception Timing (SSICR.SCKP=1)

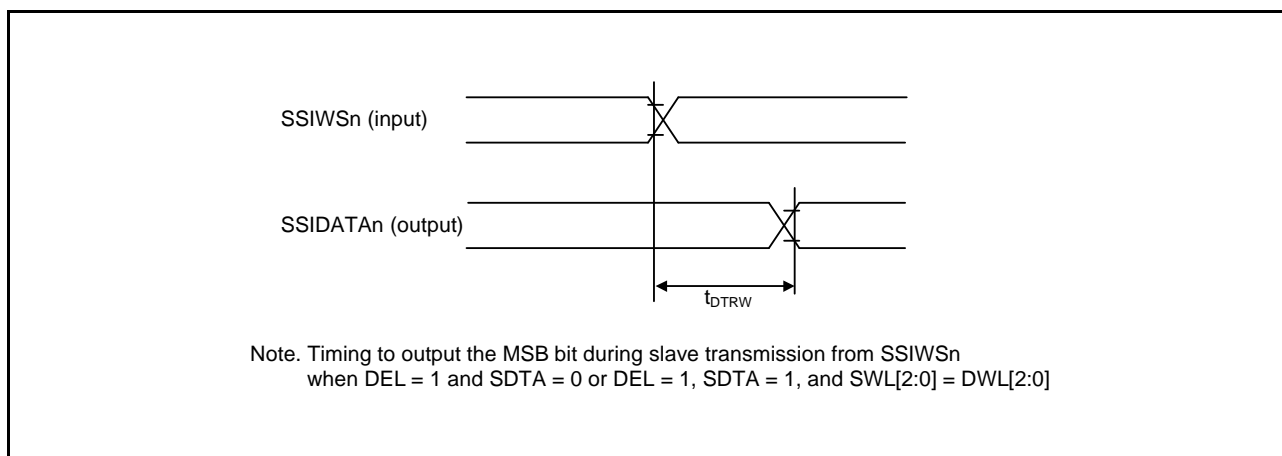


Figure 5.63 SSIDATA Output Delay After SSIWSn Changing Edge

5.4 USB Characteristics

Table 5.44 USB Characteristics (USB0_DP and USB0_DM Pin Characteristics)

Conditions: $3.0\text{ V} \leq VCC = VCC_USB = AVCC0 \leq 5.5\text{ V}$, $VSS = AVSS0 = VSS_USB = 0\text{ V}$, $T_a = -40\text{ to }+105^\circ\text{C}$

Item		Symbol	Min.	Max.	Unit	Test Conditions	
Input characteristics	Input high level voltage	V_{IH}	2.0	—	V		
	Input low level voltage	V_{IL}	—	0.8	V		
	Differential input sensitivity	V_{DI}	0.2	—	V	USB0_DP – USB0_DM	
	Differential common mode range	V_{CM}	0.8	2.5	V		
Output characteristics	Output high level voltage	V_{OH}	2.8	VCC_USB	V	$I_{OH} = -200\ \mu\text{A}$	
	Output low level voltage	V_{OL}	0.0	0.3	V	$I_{OL} = 2\ \text{mA}$	
	Cross-over voltage	V_{CRS}	1.3	2.0	V	Figure 5.64, Figure 5.65	
	Rise time	FS	t_r	4	20		ns
		LS		75	300		
	Fall time	FS	t_f	4	20		ns
		LS		75	300		
	Rise/fall time ratio	FS	t_r/t_f	90	111.11		%
LS			80	125			
Output resistance	Z_{DRV}	28	44	Ω	(Adjusting the resistance by external elements is not necessary.)		
VBUS characteristics	VBUS input voltage	V_{IH}	$VCC \times 0.8$	—	V		
		V_{IL}	—	$VCC \times 0.2$	V		
Pull-up, pull-down	Pull-down resistor	R_{PD}	14.25	24.80	k Ω		
	Pull-up resistor	R_{PUI}	0.9	1.575	k Ω	During idle state	
		R_{PUA}	1.425	3.09	k Ω	During reception	
Battery Charging Specification Ver 1.2	D+ sink current	I_{DP_SINK}	25	175	μA		
	D- sink current	I_{DM_SINK}	25	175	μA		
	DCD source current	I_{DP_SRC}	7	13	μA		
	Data detection voltage	V_{DAT_REF}	0.25	0.4	V		
	D+ source current	V_{DP_SRC}	0.5	0.7	V	Output current = 250 μA	
	D- source current	V_{DM_SRC}	0.5	0.7	V	Output current = 250 μA	

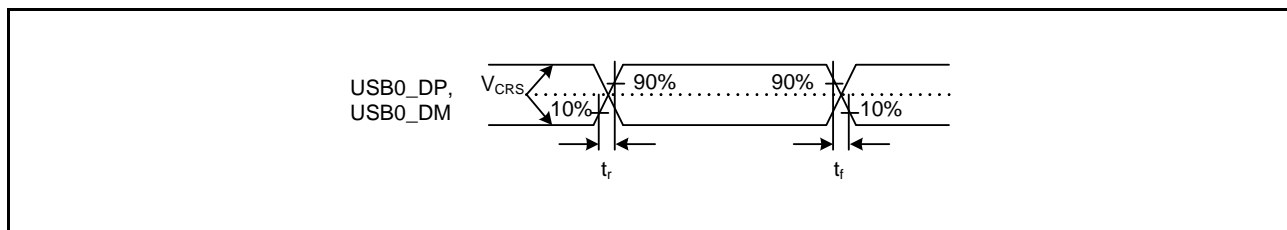


Figure 5.64 USB0_DP and USB0_DM Output Timing

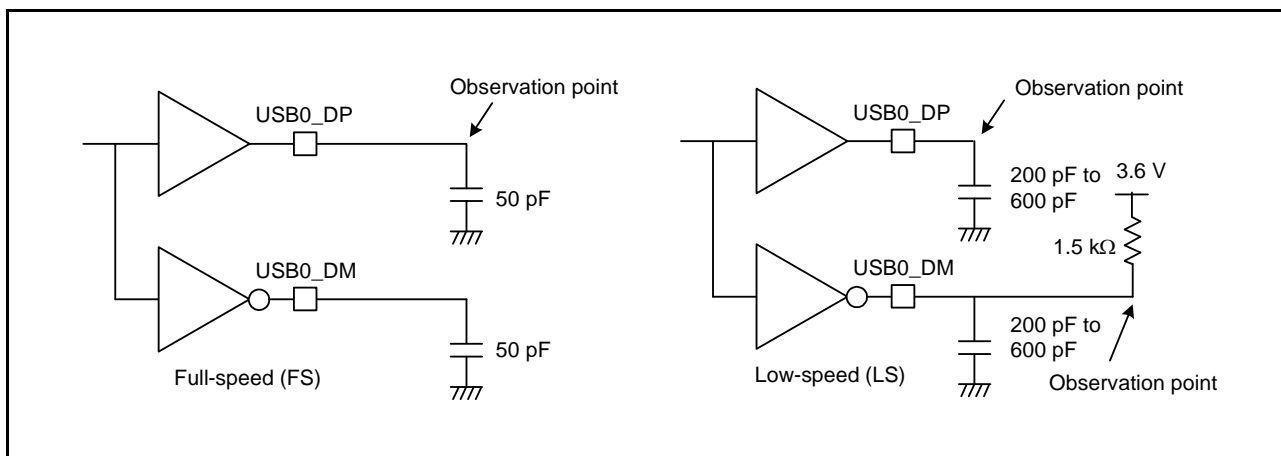


Figure 5.65 Test Circuit

5.5 A/D Conversion Characteristics

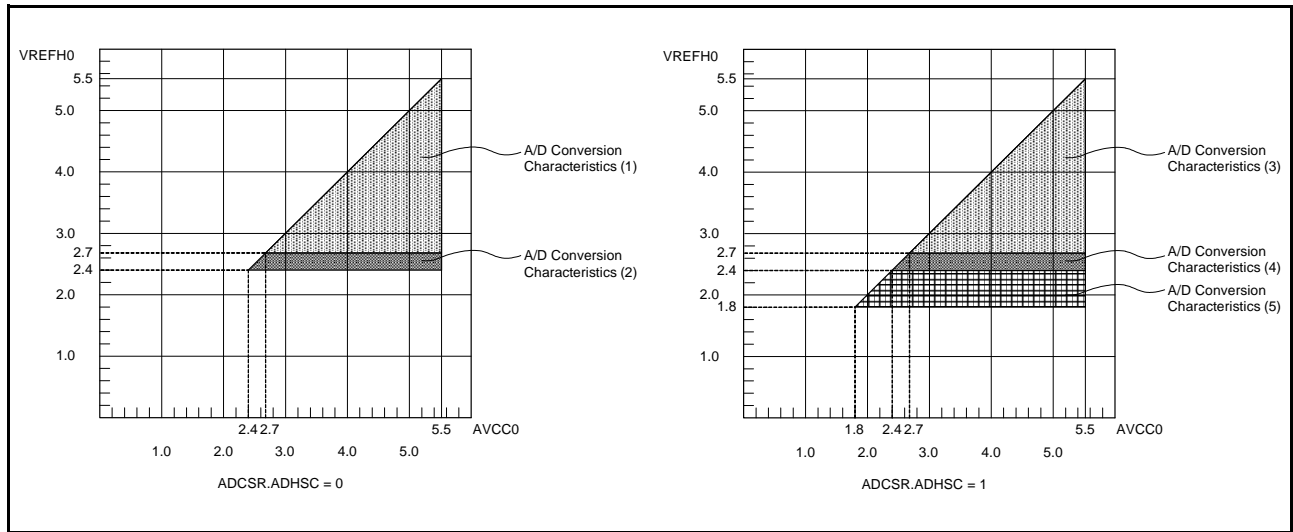


Figure 5.66 VREFH0 Voltage Range vs. AVCC0

Table 5.45 A/D Conversion Characteristics (1)

Conditions: $2.7\text{ V} \leq VCC = VCC_USB = AVCC0 \leq 5.5\text{ V}$, $2.7\text{ V} \leq VREFH0 \leq AVCC0$, reference voltage = VREFH0 selected, $VSS = AVSS0 = VREFL0 = VSS_USB = 0\text{ V}$, $T_a = -40\text{ to }+105^\circ\text{C}$

Item		Min.	Typ.	Max.	Unit	Test Conditions
Frequency		1	—	54	MHz	
Resolution		—	—	12	Bit	
Conversion time*1 (Operation at PCLKD = 54 MHz)	Permissible signal source impedance (Max.) = 0.3 kΩ	0.83	—	—	μs	High-precision channel The ADCSR.ADHSC bit is 0 The ADSSTRn register is 0Dh
		1.33	—	—		Normal-precision channel The ADCSR.ADHSC bit is 0 The ADSSTRn register is 28h
Analog input capacitance	Cs	—	—	15	pF	Pin capacitance included Figure 5.67
Analog input resistance	Rs	—	—	2.5	kΩ	Figure 5.67
Analog input voltage range	Ain	0	—	VREFH0	V	
Offset error		—	±0.5	±4.5	LSB	High-precision channel
				±6.0	LSB	Other than above
Full-scale error		—	±0.75	±4.5	LSB	High-precision channel
				±6.0	LSB	Other than above
Quantization error		—	± 0.5	—	LSB	
Absolute accuracy		—	± 1.25	±5.0	LSB	High-precision channel
				±8.0	LSB	Other than above
DNL differential non-linearity error		—	±1.0	—	LSB	
INL integral non-linearity error		—	±1.0	±3.0	LSB	

Note: The characteristics apply when no pin functions other than A/D converter input are used. Absolute accuracy includes quantization errors. Offset error, full-scale error, DNL differential non-linearity error, and INL integral non-linearity error do not include quantization errors.

Note 1. The conversion time is the sum of the sampling time and the comparison time. As the test conditions, the number of sampling states is indicated.

Table 5.46 A/D Conversion Characteristics (2)

Conditions: $2.4\text{ V} \leq VCC = VCC_USB = AVCC0 \leq 5.5\text{ V}$, $2.4\text{ V} \leq VREFH0 \leq AVCC0$, reference voltage = VREFH0 selected, $VSS = AVSS0 = VREFL0 = VSS_USB = 0\text{ V}$, $T_a = -40\text{ to }+105^\circ\text{C}$

Item		Min.	Typ.	Max.	Unit	Test Conditions
Frequency		1	—	32	MHz	
Resolution		—	—	12	Bit	
Conversion time*1 (Operation at PCLKD = 32 MHz)	Permissible signal source impedance (Max.) = 1.3 k Ω	1.41	—	—	μs	High-precision channel The ADCSR.ADHSC bit is 0 The ADSSTRn register is 0Dh
		2.25	—	—		Normal-precision channel The ADCSR.ADHSC bit is 0 The ADSSTRn register is 28h
Analog input capacitance	Cs	—	—	15	pF	Pin capacitance included Figure 5.67
Analog input resistance	Rs	—	—	2.5	k Ω	Figure 5.67
Offset error		—	± 0.5	± 4.5	LSB	
Full-scale error		—	± 0.75	± 4.5	LSB	
Quantization error		—	± 0.5	—	LSB	
Absolute accuracy		—	± 1.25	± 5.0	LSB	High-precision channel
				± 8.0	LSB	Other than above
DNL differential non-linearity error		—	± 1.0	—	LSB	
INL integral non-linearity error		—	± 1.0	± 4.5	LSB	

Note: The characteristics apply when no pin functions other than A/D converter input are used. Absolute accuracy includes quantization errors. Offset error, full-scale error, DNL differential non-linearity error, and INL integral non-linearity error do not include quantization errors.

Note 1. The conversion time is the sum of the sampling time and the comparison time. As the test conditions, the number of sampling states is indicated.

Table 5.47 A/D Conversion Characteristics (3)

Conditions: $2.7V \leq VCC = VCC_USB = AVCC0 \leq 5.5V$, $2.7V \leq VREFH0 \leq AVCC0$, reference voltage = VREFH0 selected, $VSS = AVSS0 = VREFL0 = VSS_USB = 0V$, $T_a = -40$ to $+105^\circ C$

Item		Min.	Typ.	Max.	Unit	Test Conditions
Frequency		1	—	27	MHz	
Resolution		—	—	12	Bit	
Conversion time*1 (Operation at PCLKD = 27 MHz)	Permissible signal source impedance (Max.) = 1.1 k Ω	2	—	—	μs	High-precision channel The ADCSR.ADHSC bit is 1 The ADSSTRn.SST[7:0] bits are 0Dh
		3	—	—		Normal-precision channel The ADCSR.ADHSC bit is 1 The ADSSTRn.SST[7:0] bits are 28h
Analog input capacitance	Cs	—	—	15	pF	Pin capacitance included Figure 5.67
Analog input resistance	Rs	—	—	2.5	k Ω	Figure 5.67
Offset error		—	± 0.5	± 4.5	LSB	
Full-scale error		—	± 0.75	± 4.5	LSB	
Quantization error		—	± 0.5	—	LSB	
Absolute accuracy		—	± 1.25	± 5.0	LSB	High-precision channel
				± 8.0	LSB	Other than above
DNL differential non-linearity error		—	± 1.0	—	LSB	
INL integral non-linearity error		—	± 1.0	± 3.0	LSB	

Note: The characteristics apply when no pin functions other than A/D converter input are used. Absolute accuracy includes quantization errors. Offset error, full-scale error, DNL differential non-linearity error, and INL integral non-linearity error do not include quantization errors.

Note 1. The conversion time is the sum of the sampling time and the comparison time. As the test conditions, the number of sampling states is indicated.

Table 5.48 A/D Conversion Characteristics (4)

Conditions: $2.4V \leq VCC = VCC_USB = AVCC0 \leq 5.5V$, $2.4V \leq VREFH0 \leq AVCC0$, $VSS = AVSS0 = VSS_USB = 0V$,
reference voltage = VREFH0 selected, $T_a = -40$ to $+105^\circ C$

Item		Min.	Typ.	Max.	Unit	Test Conditions
Frequency		1	—	16	MHz	
Resolution		—	—	12	Bit	
Conversion time*1 (Operation at PCLKD = 16 MHz)	Permissible signal source impedance (Max.) = 2.2 k Ω	3.38	—	—	μs	High-precision channel The ADCSR.ADHSC bit is 1 The ADSSTRn register is 0Dh
		5.06	—	—		Normal-precision channel The ADCSR.ADHSC bit is 1 The ADSSTRn register is 28h
Analog input capacitance	Cs	—	—	15	pF	Pin capacitance included Figure 5.67
Analog input resistance	Rs	—	—	2.5	k Ω	Figure 5.67
Offset error		—	± 0.5	± 4.5	LSB	
Full-scale error		—	± 0.75	± 4.5	LSB	
Quantization error		—	± 0.5	—	LSB	
Absolute accuracy		—	± 1.25	± 5.0	LSB	High-precision channel
				± 8.0	LSB	Other than above
DNL differential non-linearity error		—	± 1.0	—	LSB	
INL integral non-linearity error		—	± 1.0	± 3.0	LSB	

Note: The characteristics apply when no pin functions other than A/D converter input are used. Absolute accuracy includes quantization errors. Offset error, full-scale error, DNL differential non-linearity error, and INL integral non-linearity error do not include quantization errors.

Note 1. The conversion time is the sum of the sampling time and the comparison time. As the test conditions, the number of sampling states is indicated.

Table 5.49 A/D Conversion Characteristics (5)

Conditions: $1.8V \leq VCC = VCC_USB = AVCC0 \leq 5.5V$, $1.8V \leq VREFH0 \leq AVCC0$, $VSS = AVSS0 = VSS_USB = 0V$, reference voltage = VREFH0 selected, $T_a = -40$ to $+105^\circ C$

Item		Min.	Typ.	Max.	Unit	Test Conditions
Frequency		1	—	8	MHz	
Resolution		—	—	12	Bit	
Conversion time*1 (Operation at PCLKD = 8 MHz)	Permissible signal source impedance (Max.) = 5 kΩ	6.75	—	—	μs	High-precision channel The ADCSR.ADHSC bit is 1 The ADSSTRn register is 0Dh
		10.13	—	—		Normal-precision channel The ADCSR.ADHSC bit is 1 The ADSSTRn register is 28h
Analog input capacitance	Cs	—	—	15	pF	Pin capacitance included Figure 5.67
Analog input resistance	Rs	—	—	2.5	kΩ	Figure 5.67
Offset error		—	±1	±7.5	LSB	
Full-scale error		—	±1.5	±7.5	LSB	
Quantization error		—	±0.5	—	LSB	
Absolute accuracy		—	±3.0	±8.0	LSB	
DNL differential non-linearity error		—	±1.0	—	LSB	
INL integral non-linearity error		—	±1.25	±3.0	LSB	

Note: The characteristics apply when no pin functions other than A/D converter input are used. Absolute accuracy includes quantization errors. Offset error, full-scale error, DNL differential non-linearity error, and INL integral non-linearity error do not include quantization errors.

Note 1. The conversion time is the sum of the sampling time and the comparison time. As the test conditions, the number of sampling states is indicated.

Table 5.50 A/D Converter Channel Classification

Classification	Channel	Conditions	Remarks
High-precision channel	AN000 to AN007	AVCC0 = 1.8 to 5.5 V	Pins AN000 to AN007 cannot be used as digital outputs when the A/D converter is in use.
Normal-precision channel	AN016 to AN031		
Internal reference voltage input channel	Internal reference voltage	AVCC0 = 2.0 to 5.5 V	
Temperature sensor input channel	Temperature sensor output	AVCC0 = 2.0 to 5.5 V	

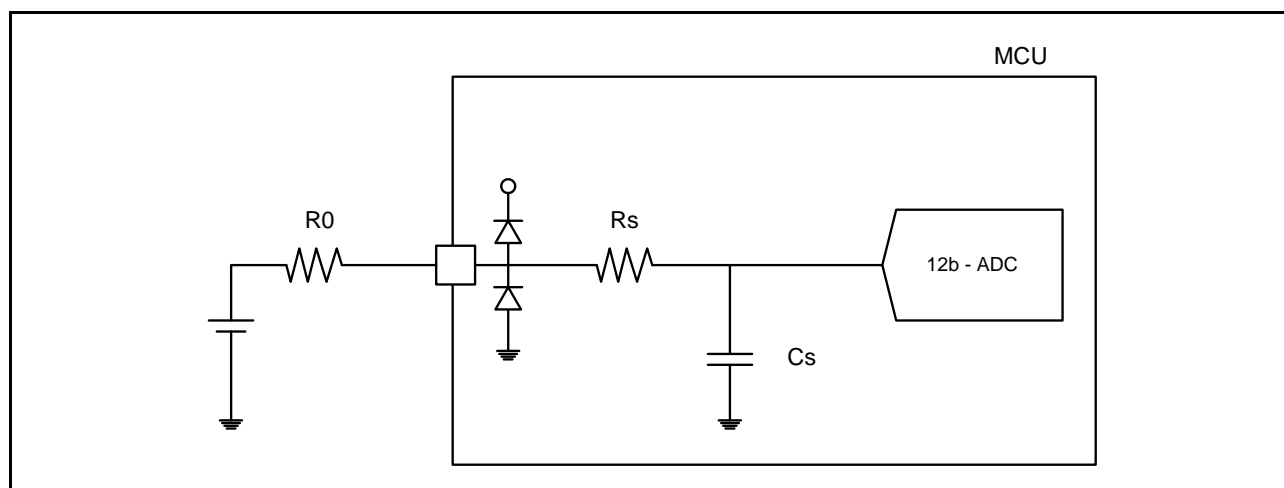


Figure 5.67 Equivalent Circuit

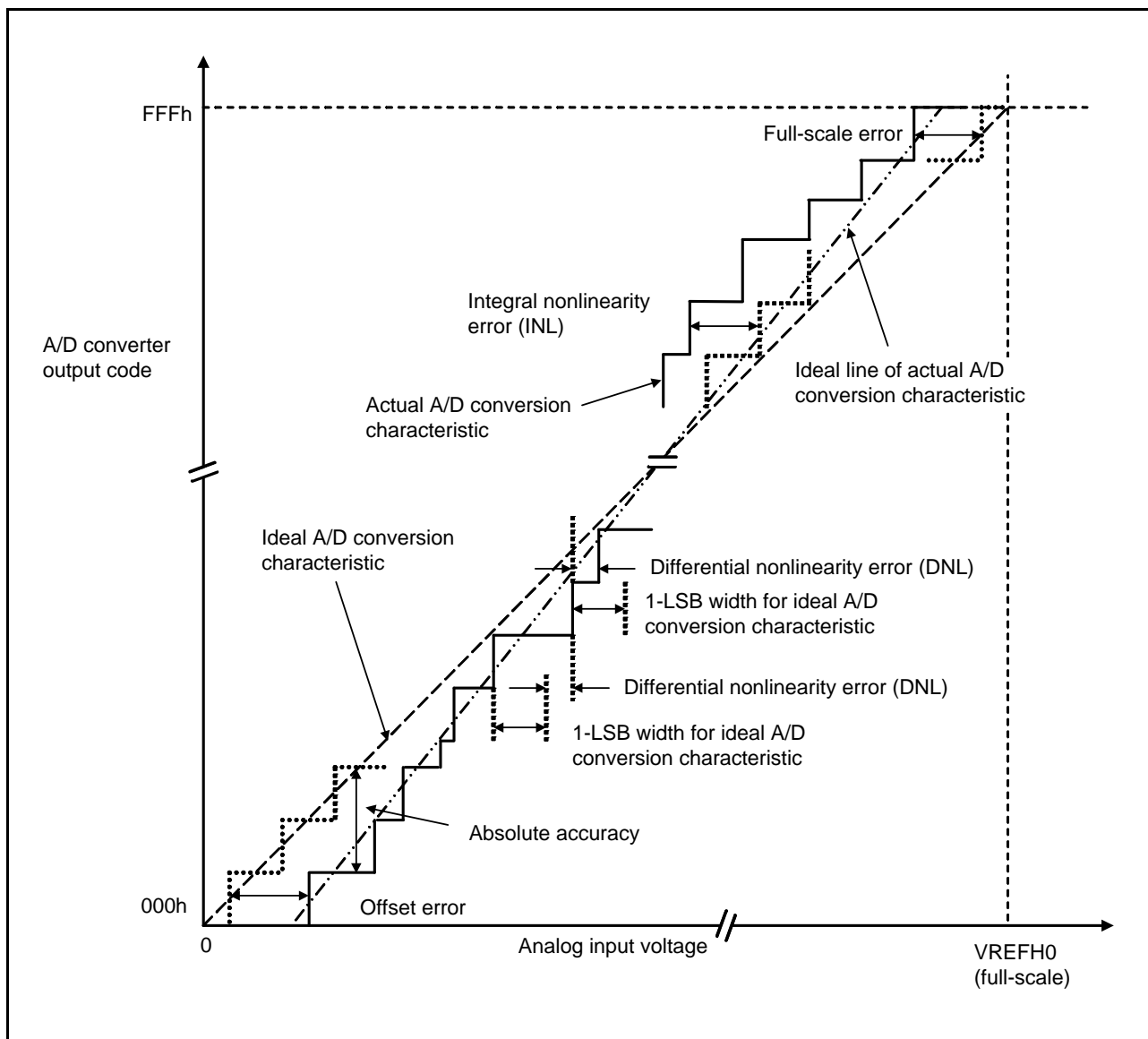


Figure 5.68 Illustration of A/D Converter Characteristic Terms

Absolute accuracy

Absolute accuracy is the difference between output code based on the theoretical A/D conversion characteristics and the actual A/D conversion result. When measuring absolute accuracy, the voltage at the midpoint of the width of analog input voltage (1-LSB width), that can meet the expectation of outputting an equal code based on the theoretical A/D conversion characteristics, is used as an analog input voltage. For example, if 12-bit resolution is used and if reference voltage (VREFH0 = 3.072 V), then 1-LSB width becomes 0.75 mV, and 0 mV, 0.75 mV, 1.5 mV, ... are used as analog input voltages.

If analog input voltage is 6 mV, absolute accuracy = ±5 LSB means that the actual A/D conversion result is in the range of 003h to 00Dh, although an output code, 008h, can be expected from the theoretical A/D conversion characteristics.

Integral non-linearity error (INL)

The integral non-linearity error is the maximum deviation between the ideal line when the measured offset and full-scale errors are zeroed, and the actual output code.

Differential non-linearity error (DNL)

The differential non-linearity error is the difference between 1-LSB width based on the ideal A/D conversion characteristics and the width of the actual output code.

Offset error

An offset error is the difference between a transition point of the ideal first output code and the actual first output code.

Full-scale error

A full-scale error is the difference between a transition point of the ideal last output code and the actual last output code.

5.6 D/A Conversion Characteristics

Table 5.51 D/A Conversion Characteristics (1)

Conditions: $1.8\text{ V} \leq VCC = VCC_USB = AVCC0 \leq 5.5\text{ V}$, $VSS = AVSS0 = VSS_USB = 0\text{ V}$, $T_a = -40\text{ to }+105^\circ\text{C}$
Reference voltage = VREFH or VREFL selected

Item	Min.	Typ.	Max.	Unit	Test Conditions
Resolution	—	—	12	Bit	
Resistive load	30	—	—	k Ω	
Capacitive load	—	—	50	pF	
Output voltage range	0.35	—	AVCC0 - 0.47	V	
DNL differential non-linearity error	—	± 0.5	± 1.0	LSB	
INL integral non-linearity error	—	± 2.0	± 8.0	LSB	
Offset error	—	—	± 20	mV	
Full-scale error	—	—	± 20	mV	
Output resistance	—	5	—	Ω	
Conversion time	—	—	30	μs	

Table 5.52 D/A Conversion Characteristics (2)

Conditions: $1.8\text{ V} \leq VCC = VCC_USB = AVCC0 \leq 5.5\text{ V}$, $VSS = AVSS0 = VREFL = VSS_USB = 0\text{ V}$, $T_a = -40\text{ to }+105^\circ\text{C}$
Reference voltage = AVCC0 or AVSS0 selected

Item	Min.	Typ.	Max.	Unit	Test Conditions
Resolution	—	—	12	Bit	
Resistive load	30	—	—	k Ω	
Capacitive load	—	—	50	pF	
Output voltage range	0.35	—	AVCC0 - 0.47	V	
DNL differential non-linearity error	—	± 0.5	± 2.0	LSB	
INL integral non-linearity error	—	± 2.0	± 8.0	LSB	
Offset error	—	—	± 30	mV	
Full-scale error	—	—	± 30	mV	
Output resistance	—	5	—	Ω	
Conversion time	—	—	30	μs	

Table 5.53 D/A Conversion Characteristics (3)

Conditions: $1.8\text{ V} \leq VCC = VCC_USB = AVCC0 \leq 5.5\text{ V}$, $VSS = AVSS0 = VSS_USB = 0\text{ V}$, $T_a = -40\text{ to }+105^\circ\text{C}$
Reference voltage = internal reference voltage selected

Item	Min.	Typ.	Max.	Unit	Test Conditions
Resolution	—	—	12	Bit	
Internal reference voltage (Vbgr)	1.36	1.43	1.50	V	
Resistive load	30	—	—	k Ω	
Capacitive load	—	—	50	pF	
Output voltage range	0.35	—	Vbgr	V	
DNL differential non-linearity error	—	± 2.0	± 16.0	LSB	
INL integral non-linearity error	—	± 8.0	± 16.0	LSB	
Offset error	—	—	30	mV	
Output resistance	—	5	—	Ω	
Conversion time	—	—	30	μs	

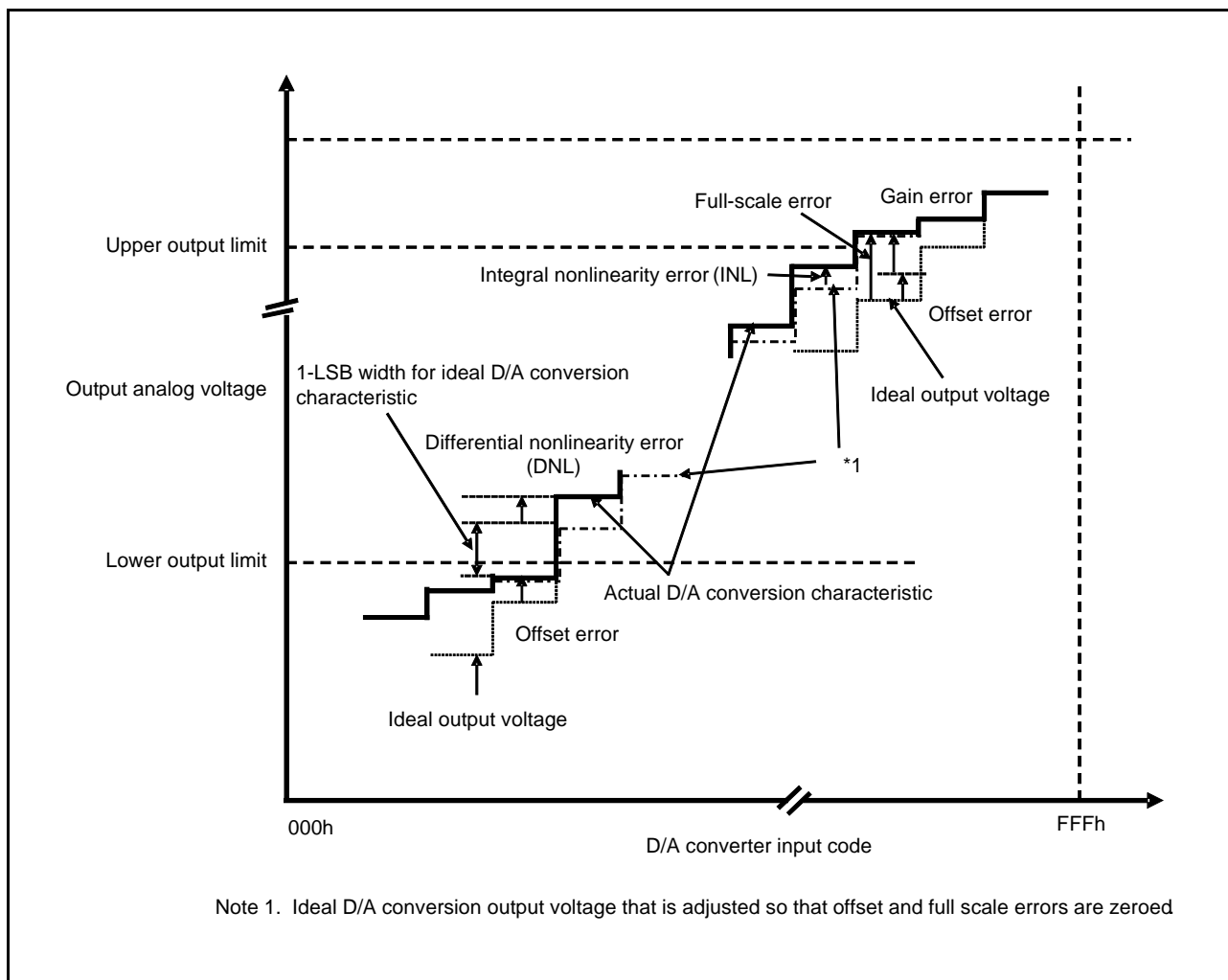


Figure 5.69 Illustration of D/A Converter Characteristic Terms

Integral non-linearity error (INL)

The integral non-linearity error is the maximum deviation between the ideal line when the measured offset and full-scale errors are zeroed, and the actual output code.

Differential non-linearity error (DNL)

The differential non-linearity error is the difference between 1-LSB width based on the ideal D/A conversion characteristics and the width of the actually output code.

Offset error

An offset error is the difference between a transition point of the ideal first output code and the actual first output code.

Full-scale error

A full-scale error is the difference between a transition point of the ideal last output code and the actual last output code.

5.7 Temperature Sensor Characteristics

Table 5.54 Temperature Sensor Characteristics

Conditions: $2.0\text{ V} \leq V_{CC} = V_{CC_USB} = AV_{CC0} \leq 5.5\text{ V}$, $V_{SS} = AV_{SS0} = V_{SS_USB} = 0\text{ V}$, $T_a = -40\text{ to }+105^\circ\text{C}$

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Relative accuracy	—	—	± 1.5	—	°C	2.4 V or above
		—	± 2.0	—		Below 2.4 V
Temperature slope	—	—	-3.65	—	mV/°C	
Output voltage (25°C)	—	—	1.05	—	V	VCC = 3.3 V
Temperature sensor start time	t _{START}	—	—	5	µs	
Sampling time	—	5	—	—	µs	

5.8 Comparator Characteristics

Table 5.55 Comparator Characteristics

Conditions: $1.8\text{ V} \leq V_{CC} = V_{CC_USB} = AV_{CC0} \leq 5.5\text{ V}$, $V_{SS} = AV_{SS0} = V_{SS_USB} = 0\text{ V}$, $T_a = -40\text{ to }+105^\circ\text{C}$

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
CVREFB0 to CVREFB3 input reference voltage	VREF	0	—	VCC - 1.4	V	
CMPB0 to CMPB3 input voltage	VI	-0.3	—	VCC + 0.3	V	
Offset	Comparator high-speed mode	—	—	50	mV	
	Comparator high-speed mode Window function enabled	—	—	60	mV	
	Comparator low-speed mode	—	—	40	mV	
Comparator output delay time	Comparator high-speed mode	Td	—	1.2	µs	VCC = 3 V, input slew rate $\geq 50\text{ mV}/\mu\text{s}$
	Comparator high-speed mode Window function enabled	Tdw	—	2.0	µs	
	Comparator low-speed mode	Td	—	5.0	µs	
High-side reference voltage (comparator high-speed mode, window function enabled)	VRFH	—	0.76 VCC	—	V	
Low-side reference voltage (comparator high-speed mode, window function enabled)	VRFL	—	0.24 VCC	—	V	
Operation stabilization wait time	Tcmp	100	—	—	µs	

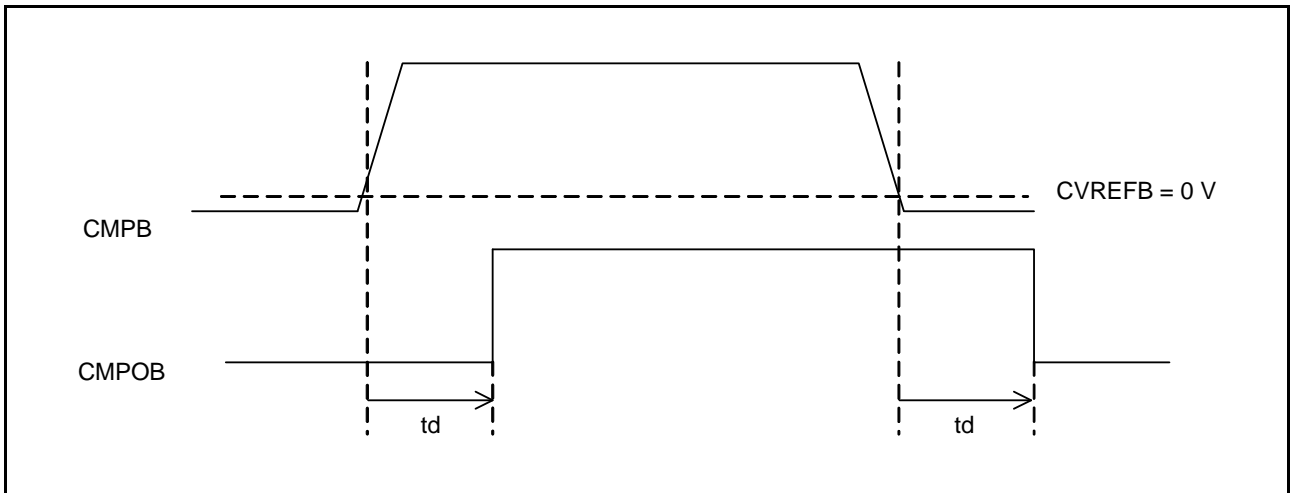


Figure 5.70 Comparator Output Delay Time in Comparator High-Speed Mode and Low-Speed Mode

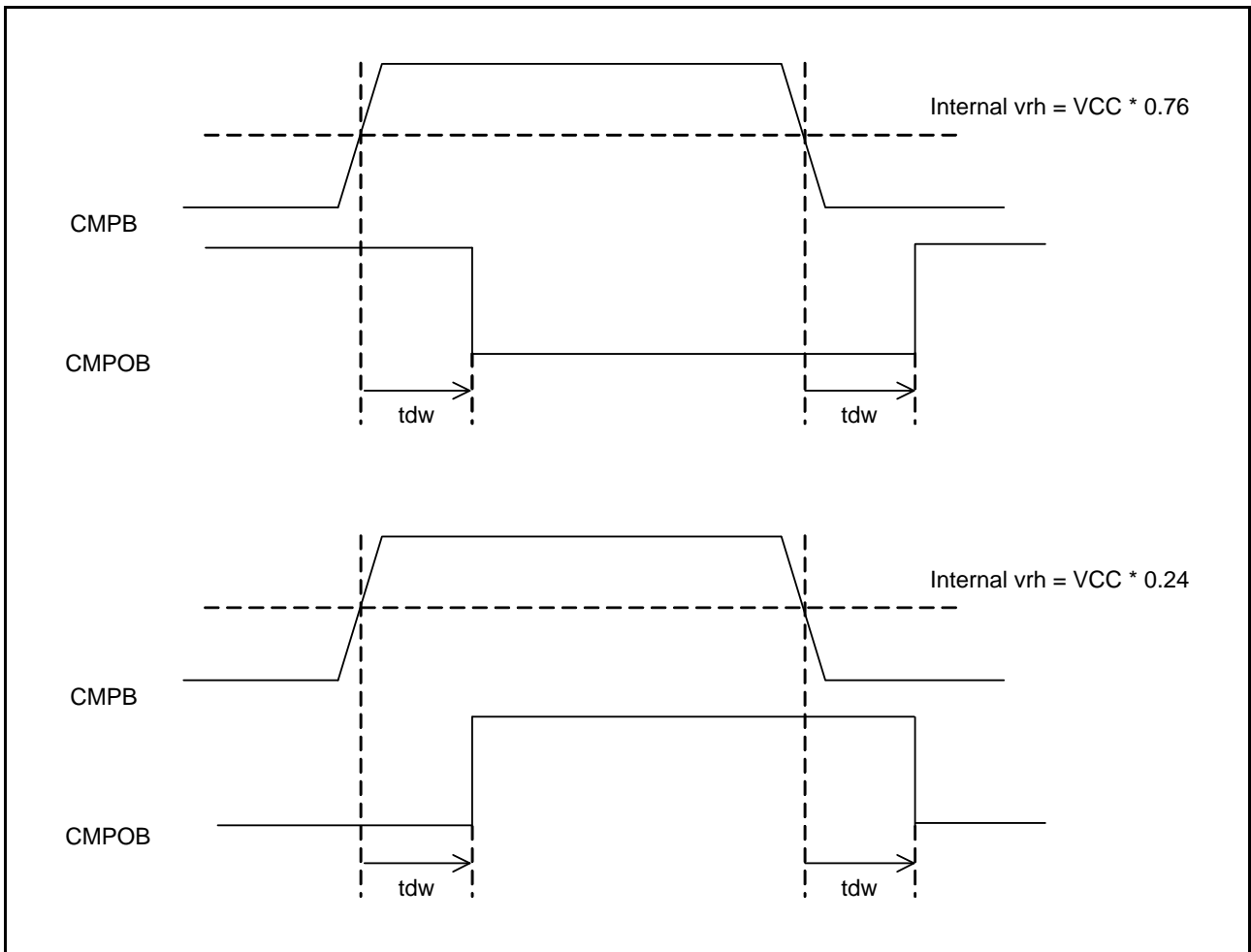


Figure 5.71 Comparator Output Delay Time in High-Speed Mode with Window Function Enabled

5.9 CTSU Characteristics

Table 5.56 CTSU Characteristics

 Conditions: $1.8\text{ V} \leq V_{CC} = V_{CC_USB} = AV_{CC0} \leq 5.5\text{ V}$, $V_{SS} = AV_{SS0} = V_{SS_USB} = 0\text{ V}$, $T_a = -40\text{ to }+105^\circ\text{C}$

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
External capacitance connected to TSCAP pin	C_{Tscap}	9	10	11	nF	
TS pin capacitive load	C_{base}	—	—	50	pF	
Permissible output high current	ΣI_{OH}	—	—	-24	mA	When the mutual capacitance method is applied

5.10 Characteristics of Power-On Reset Circuit and Voltage Detection Circuit

Table 5.57 Characteristics of Power-On Reset Circuit and Voltage Detection Circuit (1)

 Conditions: $1.8\text{ V} \leq V_{CC} = V_{CC_USB} = AV_{CC0} \leq 5.5\text{ V}$, $V_{SS} = AV_{SS0} = V_{SS_USB} = 0\text{ V}$, $T_a = -40\text{ to }+105^\circ\text{C}$

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions	
Voltage detection level	Power-on reset (POR)	V_{POR}	1.35	1.50	1.65	V	Figure 5.72, Figure 5.73
	Voltage detection circuit (LVD0)* ¹	V_{det0_0}	3.67	3.84	3.97	V	Figure 5.74 At falling edge VCC
		V_{det0_1}	2.70	2.82	3.00		
		V_{det0_2}	2.37	2.51	2.67		
		V_{det0_3}	1.80	1.90	1.99		
	Voltage detection circuit (LVD1)* ²	V_{det1_0}	4.12	4.29	4.42	V	Figure 5.75 At falling edge VCC
		V_{det1_1}	3.98	4.14	4.28		
		V_{det1_2}	3.86	4.02	4.16		
		V_{det1_3}	3.68	3.84	3.98		
		V_{det1_4}	2.99	3.10	3.29		
		V_{det1_5}	2.89	3.00	3.19		
		V_{det1_6}	2.79	2.90	3.09		
		V_{det1_7}	2.68	2.79	2.98		
		V_{det1_8}	2.57	2.68	2.87		
		V_{det1_9}	2.47	2.58	2.67		
V_{det1_A}		2.37	2.48	2.57			
V_{det1_B}		2.10	2.20	2.30			
Voltage detection circuit (LVD2)* ³	V_{det2_0}	4.08	4.29	4.48	V	Figure 5.76 At falling edge VCC	
	V_{det2_1}	3.95	4.14	4.35			
	V_{det2_2}	3.82	4.02	4.22			
	V_{det2_3}	3.62	3.84	4.02			

Note: These characteristics apply when noise is not superimposed on the power supply. When a setting is made so that the voltage detection level overlaps with that of the voltage detection circuit (LVD2), it cannot be specified which of LVD1 and LVD2 is used for voltage detection.

Note 1. n in the symbol V_{det0_n} denotes the value of the OFS1.VDSEL[1:0] bits.

Note 2. n in the symbol V_{det1_n} denotes the value of the LVDLVLRLVD1LVL[3:0] bits.

Note 3. n in the symbol V_{det2_n} denotes the value of the LVDLVLRLVD2LVL[1:0] bits.

Table 5.58 Characteristics of Power-On Reset Circuit and Voltage Detection Circuit (2)Conditions: $1.8\text{ V} \leq V_{CC0} = V_{CC_USB} = AV_{CC0} \leq 5.5\text{ V}$, $V_{SS} = AV_{SS0} = V_{SS_USB} = 0\text{ V}$, $T_a = -40\text{ to }+105^\circ\text{C}$

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Wait time after power-on reset cancellation	At normal startup*1	t_{POR}	—	9.1	—	ms Figure 5.73
	During fast startup time*2	t_{POR}	—	1.6	—	
Wait time after voltage monitoring 0 reset cancellation	Power-on voltage monitoring 0 reset disabled*1	t_{LVD0}	—	568	—	μs Figure 5.74
	Power-on voltage monitoring 0 reset enabled*2		—	100	—	
Wait time after voltage monitoring 1 reset cancellation	t_{LVD1}	—	100	—	μs	Figure 5.75
Wait time after voltage monitoring 2 reset cancellation	t_{LVD2}	—	100	—	μs	Figure 5.76
Response delay time	t_{det}	—	—	350	μs	Figure 5.72
Minimum VCC down time*3	t_{VOFF}	350	—	—	μs	Figure 5.72, VCC = 1.0 V or above
Power-on reset enable time	$t_{W(POR)}$	1	—	—	ms	Figure 5.73, VCC = below 1.0 V
LVD operation stabilization time (after LVD is enabled)	$T_{d(E-A)}$	—	—	300	μs	Figure 5.75, Figure 5.76
Hysteresis width (power-on rest (POR))	V_{PORH}	—	110	—	mV	
Hysteresis width (voltage detection circuit: LVD1 and LVD2)	V_{LVH}	—	70	—	mV	When Vdet1_0 to Vdet1_4 is selected
		—	60	—		When Vdet1_5 to Vdet1_9 is selected
		—	50	—		When Vdet1_A or Vdet1_B is selected
		—	40	—		When Vdet1_C or Vdet1_D is selected
		—	60	—		When LVD2 is selected

Note: These characteristics apply when noise is not superimposed on the power supply. When a setting is made so that the voltage detection level overlaps with that of the voltage detection circuit (LVD1), it cannot be specified which of LVD1 and LVD2 is used for voltage detection.

Note 1. When OFS1.(LVDAS, FASTSTUP) = 11b.

Note 2. When OFS1.(LVDAS, FASTSTUP) \neq 11b.

Note 3. The minimum VCC down time indicates the time when VCC is below the minimum value of voltage detection levels V_{POR} , V_{det0} , V_{det1} , and V_{det2} for the POR/LVD.

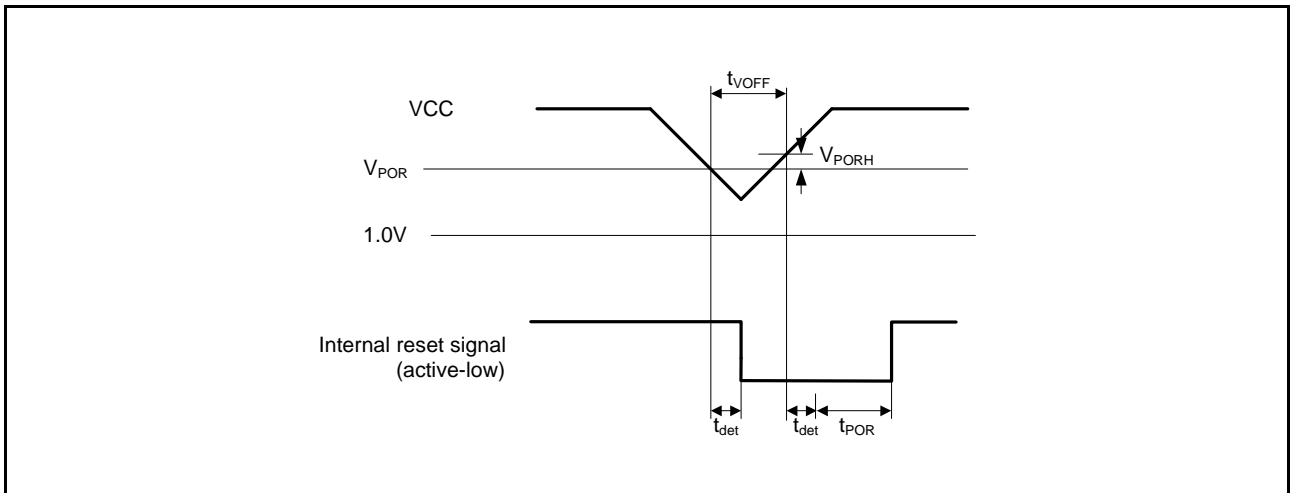
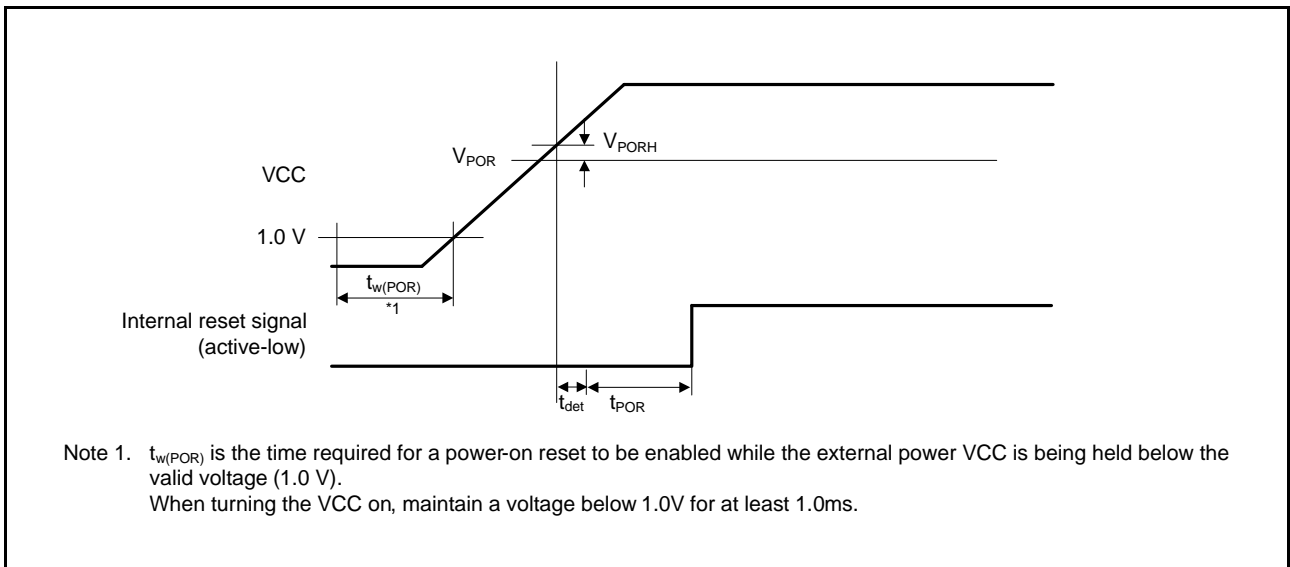


Figure 5.72 Voltage Detection Reset Timing



Note 1. t_{w(POR)} is the time required for a power-on reset to be enabled while the external power VCC is being held below the valid voltage (1.0 V).
When turning the VCC on, maintain a voltage below 1.0V for at least 1.0ms.

Figure 5.73 Power-On Reset Timing

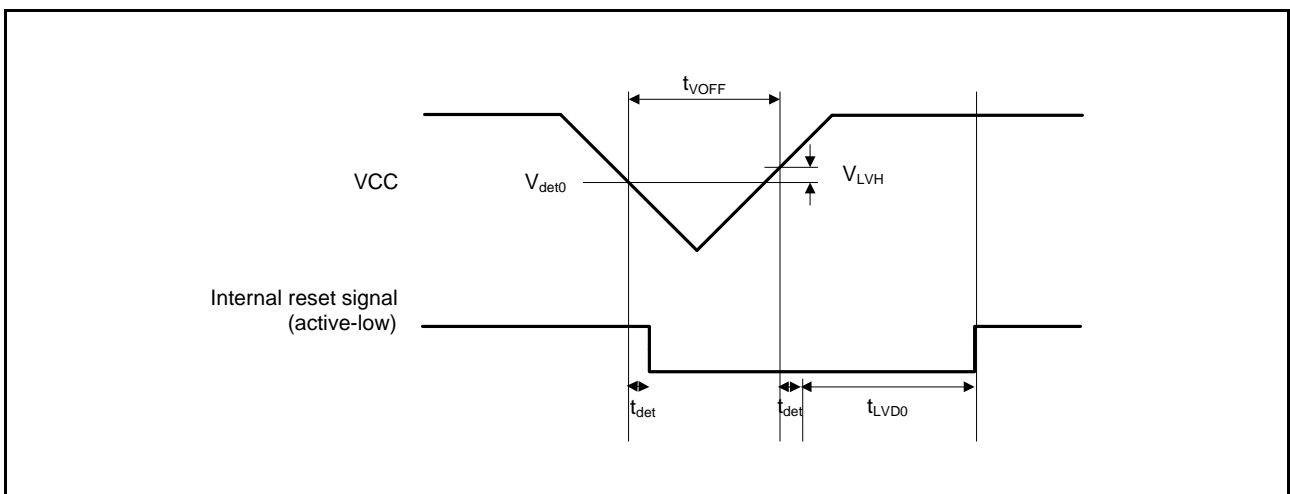


Figure 5.74 Voltage Detection Circuit Timing (Vdet0)

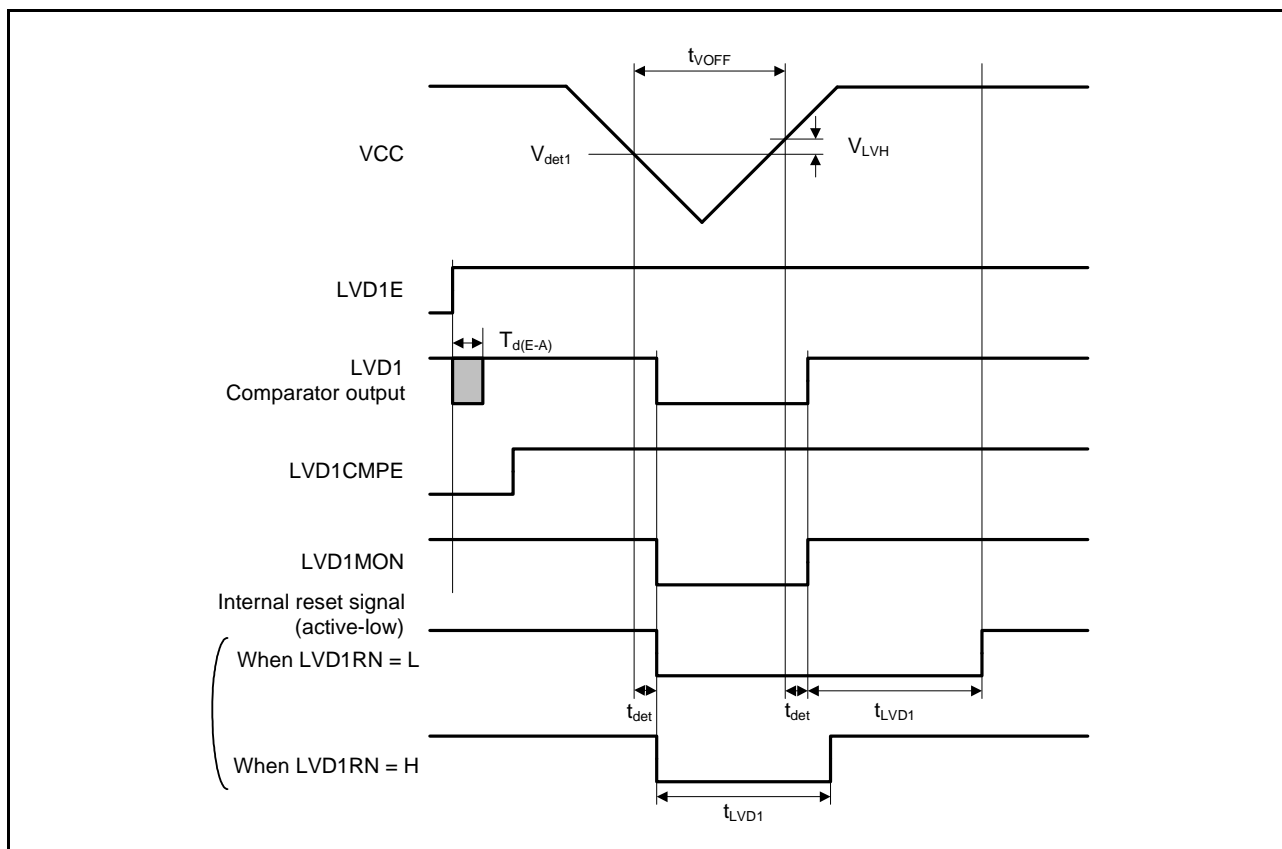


Figure 5.75 Voltage Detection Circuit Timing (V_{det1})

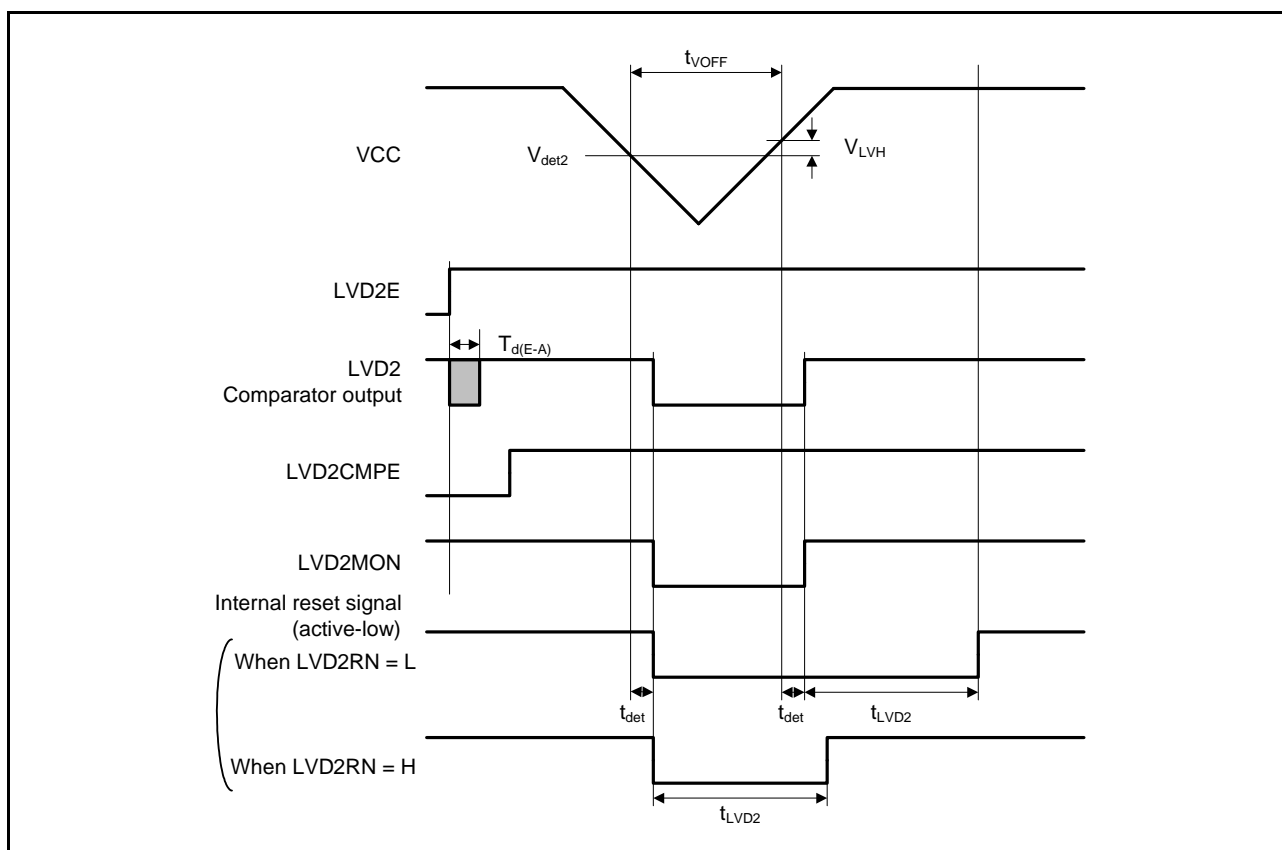


Figure 5.76 Voltage Detection Circuit Timing (V_{det2})

5.11 Oscillation Stop Detection Timing

Table 5.59 Oscillation Stop Detection Timing

Conditions: $1.8\text{ V} \leq VCC = VCC_USB = AVCC0 \leq 5.5\text{ V}$, $VSS = AVSS0 = VREFL0 = VSS_USB = 0\text{ V}$, $T_a = -40\text{ to }+105^\circ\text{C}$

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Detection time	t_{dr}	—	—	1	ms	Figure 5.77

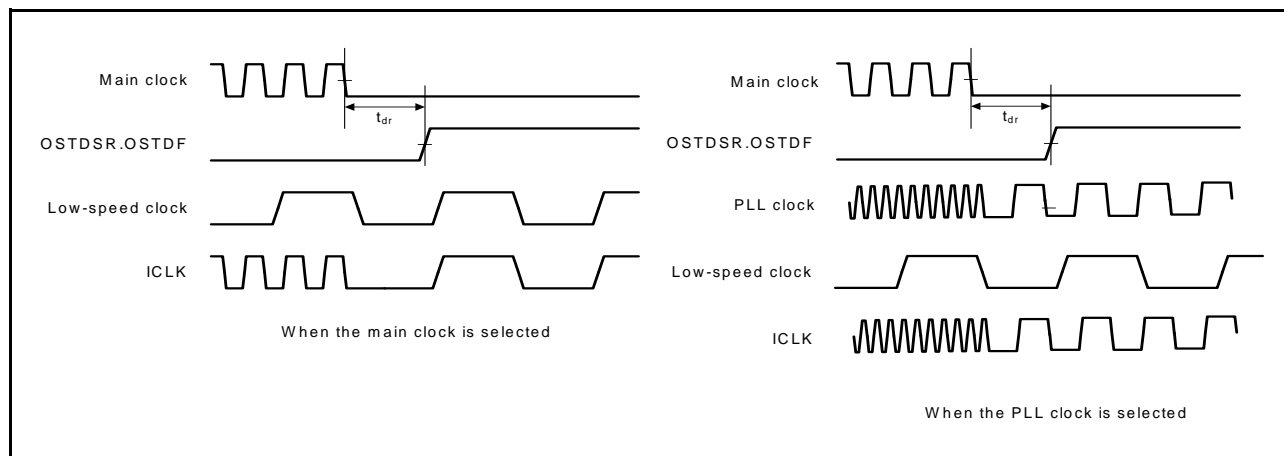


Figure 5.77 Oscillation Stop Detection Timing

5.12 Battery Backup Function Characteristics

Table 5.60 Battery Backup Function Characteristics

Conditions: $1.8\text{ V} \leq \text{VCC} = \text{VCC_USB} = \text{AVCC0} \leq 5.5\text{ V}$, $1.8\text{ V} \leq \text{VBATT} \leq 5.5\text{ V}$, $\text{VSS} = \text{AVSS0} = \text{VREFL0} = \text{VSS_USB} = 0\text{ V}$, $T_a = -40\text{ to }+105^\circ\text{C}$

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions	
Voltage level for switching to battery backup (falling)	V_{DETBATT}	1.99	2.09	2.19	V	Figure 5.78	
Hysteresis width	V_{VBATTH}	—	100	—	mV		
VCC-off period for starting power supply switching	t_{VOFFBATT}	—	—	350	μs		
Allowable voltage change rising/falling gradient	$dt/d\text{VCC}$	1.0	—	—	ms/V	Figure 5.7	
Level for detection of voltage drop on the VBATT pin (falling)	$\text{VBTLVDLVL}[1:0] = 10\text{b}$	$V_{\text{DETBATLVD}}$	2.11	2.20	2.29	V	Figure 5.78
	$\text{VBTLVDLVL}[1:0] = 11\text{b}$		1.87	2.00	2.13	V	
Hysteresis width for detection of voltage drop on the VBATT pin	V_{BATLVDH}	—	50	—	mV		

Note: The VCC-off period for starting power supply switching indicates the period in which VCC is below the minimum value of the voltage level for switching to battery backup (V_{DETBATT}).

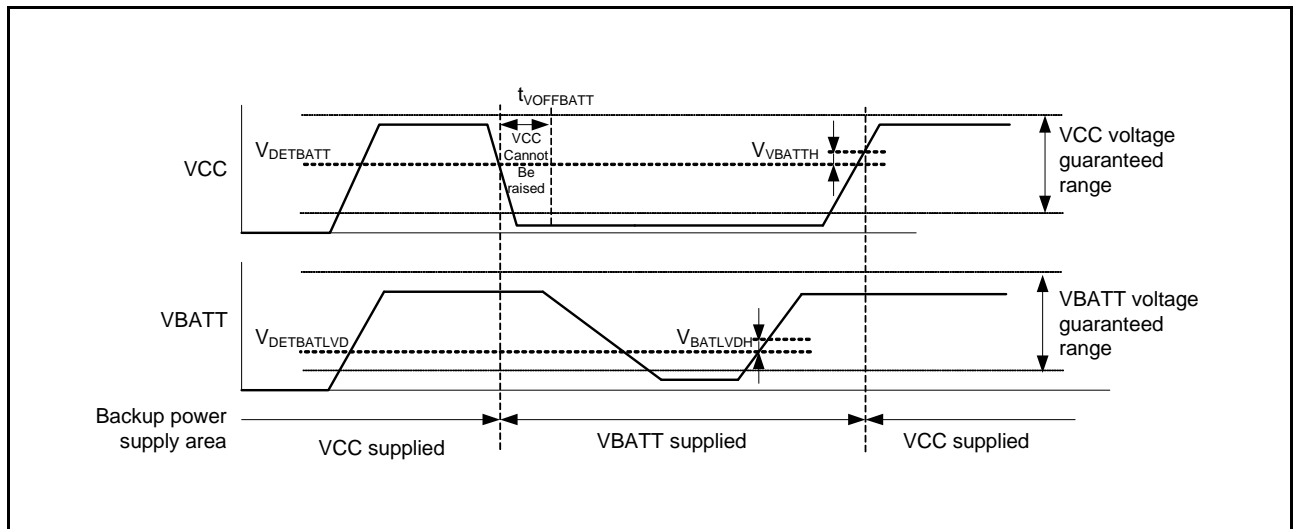


Figure 5.78 Battery Backup Function Characteristics

5.13 ROM (Flash Memory for Code Storage) Characteristics

Table 5.61 ROM (Flash Memory for Code Storage) Characteristics (1)

Item	Symbol	Min.	Typ.	Max.	Unit	Conditions
Reprogramming/erasure cycle*1	N_{PEC}	1000	—	—	Times	
Data hold time	After 1000 times of N_{PEC}	t_{DRP}	20*2, *3	—	Year	$T_a = +85^\circ\text{C}$

Note 1. Definition of reprogram/erase cycle: The reprogram/erase cycle is the number of erasing for each block. When the reprogram/erase cycle is n times ($n = 1000$), erasing can be performed n times for each block. For instance, when 4-byte programming is performed 256 times for different addresses in a 1-Kbyte block and then the entire block is erased, the reprogram/erase cycle is counted as one. However, programming the same address for several times as one erasing is not enabled (overwriting is prohibited).

Note 2. Characteristic when using the flash memory programmer and the self-programming library provided from Renesas Electronics.

Note 3. This result is obtained from reliability testing.

Table 5.62 ROM (Flash Memory for Code Storage) Characteristics (2) High-Speed Operating Mode

Conditions: $2.7\text{ V} \leq V_{CC} = V_{CC_USB} = AV_{CC0} \leq 5.5\text{ V}$, $V_{SS} = AV_{SS0} = V_{SS_USB} = 0\text{ V}$

Temperature range for the programming/erasure operation: $T_a = -40$ to $+105^\circ\text{C}$

Item	Symbol	FCLK = 1 MHz			FCLK = 32 MHz			Unit	
		Min.	Typ.	Max.	Min.	Typ.	Max.		
Programming time	8-byte	t_{PB}	—	112	967	—	52.3	491	μs
Erasure time	2-Kbyte	t_{E2K}	—	8.75	278	—	5.50	215	ms
	512-Kbyte (when block erase command is used)	t_{E512K}	—	928	19218	—	72.0	1679	ms
	512-Kbyte (when all-block erase command is used)	t_{EA512K}	—	923	19013	—	66.7	1469	ms
Blank check time	8-byte	t_{BC8}	—	—	55.0	—	—	16.1	μs
	2-Kbyte	t_{BC2K}	—	—	1840	—	—	136	ms
Erase operation forced stop time		t_{SED}	—	—	18.0	—	—	10.7	μs
Start-up area switching setting time		t_{SAS}	—	12.3	566.5	—	6.2	434	ms
Access window time		t_{AWS}	—	12.3	566.5	—	6.2	434	ms
ROM mode transition wait time 1		t_{DIS}	2.0	—	—	2.0	—	—	μs
ROM mode transition wait time 2		t_{MS}	5.0	—	—	5.0	—	—	μs

Note: The time until each operation of the flash memory is started after instructions are executed by software is not included.

Note: The lower-limit frequency of FCLK is 1 MHz during programming or erasing of the flash memory. When using FCLK at below 4 MHz, the frequency can be set to 1 MHz, 2 MHz, or 3 MHz. A non-integer frequency such as 1.5 MHz cannot be set.

Note: The frequency accuracy of FCLK must be within $\pm 3.5\%$.

Table 5.63 ROM (Flash Memory for Code Storage) Characteristics (3) Middle-Speed Operating ModeConditions: $1.8\text{ V} \leq V_{CC} = V_{CC_USB} = AV_{CC0} \leq 5.5\text{ V}$, $V_{SS} = AV_{SS0} = V_{SS_USB} = 0\text{ V}$ Temperature range for the programming/erasure operation: $T_a = -40$ to $+85^\circ\text{C}$

Item	Symbol	FCLK = 1 MHz			FCLK = 8 MHz			Unit	
		Min.	Typ.	Max.	Min.	Typ.	Max.		
Programming time	8-byte	t_{P8}	—	152	1367	—	97.9	936	μs
Erasure time	2-Kbyte	t_{E2K}	—	8.8	279.7	—	5.9	221	ms
	512-Kbyte (when block erase command is used)	t_{E512K}	—	928	19221	—	191	4108	ms
	512-Kbyte (when all- block erase command is used)	t_{EA512K}	—	923	19015	—	185	3901	ms
Blank check time	8-byte	t_{BC8}	—	—	85.0	—	—	50.88	μs
	2-Kbyte	t_{BC2K}	—	—	1870	—	—	402	μs
Erase operation forced stop time		t_{SED}	—	—	28.0	—	—	21.3	μs
Start-up area switching setting time		t_{SAS}	—	13.0	573.3	—	7.7	451	ms
Access window time		t_{AWS}	—	13.0	573.3	—	7.7	451	ms
ROM mode transition wait time 1		t_{DIS}	2.0	—	—	2.0	—	—	μs
ROM mode transition wait time 2		t_{MS}	3.0	—	—	3.0	—	—	μs

Note: The time until each operation of the flash memory is started after instructions are executed by software is not included.

Note: The lower-limit frequency of FCLK is 1 MHz during programming or erasing of the flash memory. When using FCLK at below 4 MHz, the frequency can be set to 1 MHz, 2 MHz, or 3 MHz. A non-integer frequency such as 1.5 MHz cannot be set.

Note: The frequency accuracy of FCLK must be within $\pm 3.5\%$.

5.14 E2 DataFlash Characteristics (Flash Memory for Data Storage)

Table 5.64 E2 DataFlash Characteristics (1)

Item		Symbol	Min.	Typ.	Max.	Unit	Conditions
Reprogramming/erasure cycle*1		N _{DPEC}	100000	1000000	—	Times	
Data hold time	After 10000 times of N _{DPEC}	t _{DDRP}	20*2, *3	—	—	Year	T _a = +85°C
	After 100000 times of N _{DPEC}		5*2, *3	—	—	Year	
	After 1000000 times of N _{DPEC}		—	1*2, *3	—	Year	

Note 1. The reprogram/erase cycle is the number of erasing for each block. When the reprogram/erase cycle is n times (n = 100000), erasing can be performed n times for each block. For instance, when 1-byte programming is performed 1000 times for different addresses in a 1-Kbyte block and then the entire block is erased, the reprogram/erase cycle is counted as one. However, programming the same address for several times as one erasing is not enabled (overwriting is prohibited).

Note 2. Characteristic when the flash memory programmer is used and the self-programming library is provided from Renesas Electronics.

Note 3. These results are obtained from reliability testing.

**Table 5.65 E2 DataFlash Characteristics (2)
: high-speed operating mode**

Conditions: 2.7 V ≤ VCC = VCC_USB = AVCC0 ≤ 5.5 V, VSS = AVSS0 = VSS_USB = 0 V

Temperature range for the programming/erasure operation: T_a = -40 to +105°C

Item		Symbol	FCLK = 1 MHz			FCLK = 32 MHz			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Programming time	1 byte	t _{DP1}	—	95.0	797	—	40.8	376	μs
Erasure time	1 Kbyte	t _{DE1K}	—	19.5	498	—	6.2	230	ms
	8 Kbyte	t _{DE8K}	—	119.8	2556	—	12.9	368	ms
Blank check time	1 byte	t _{DBC1}	—	—	55.00	—	—	16.1	μs
	1 Kbyte	t _{DBC1K}	—	—	0.72	—	—	0.50	ms
Erase operation forced stop time		t _{DSED}	—	—	16.0	—	—	10.7	μs
DataFlash STOP recovery time		t _{DSTOP}	5.0	—	—	5.0	—	—	μs

Note: The time until each operation of the flash memory is started after instructions are executed by software is not included.

Note: The lower-limit frequency of FCLK is 1 MHz during programming or erasing of the flash memory. When using FCLK at below 4 MHz, the frequency can be set to 1 MHz, 2 MHz, or 3 MHz. A non-integer frequency such as 1.5 MHz cannot be set.

Note: The frequency accuracy of FCLK must be within ±3.5%.

**Table 5.66 E2 DataFlash Characteristics (3)
: middle-speed operating mode**

Conditions: 1.8 V ≤ VCC0 = VCC_USB = AVCC0 ≤ 5.5 V, VSS = AVSS0 = VSS_USB = 0 V

Temperature range for the programming/erasure operation: T_a = -40 to +85°C

Item		Symbol	FCLK = 1 MHz			FCLK = 8 MHz			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Programming time	1 byte	t _{DP1}	—	135	1197	—	86.5	823	μs
Erasure time	1 Kbyte	t _{DE1K}	—	19.6	501	—	8.0	265	ms
	8 Kbyte	t _{DE8K}	—	120	2558	—	27.7	669	ms
Blank check time	1 byte	t _{DBC1}	—	—	85.0	—	—	50.9	μs
	1 Kbyte	t _{DBC1K}	—	—	0.72	—	—	1.45	ms
Erase operation forced stop time		t _{DSED}	—	—	28.0	—	—	21.3	μs
DataFlash STOP recovery time		t _{DSTOP}	0.72	—	—	0.72	—	—	μs

Note: The time until each operation of the flash memory is started after instructions are executed by software is not included.

Note: The lower-limit frequency of FCLK is 1 MHz during programming or erasing of the flash memory. When using FCLK at below 4 MHz, the frequency can be set to 1 MHz, 2 MHz, or 3 MHz. A non-integer frequency such as 1.5 MHz cannot be set.

Note: The frequency accuracy of FCLK must be within ±3.5%.

5.15 Usage Notes

5.15.1 Connecting VCL Capacitor and Bypass Capacitors

This MCU integrates an internal voltage-down circuit, which is used for lowering the power supply voltage in the internal MCU automatically to the optimum level. A 4.7- μ F capacitor needs to be connected between this internal voltage-down power supply (VCL pin) and the VSS pin. Figure 5.79 to Figure 5.81 shows how to connect external capacitors. Place an external capacitor close to the pins. Do not apply the power supply voltage to the VCL pin. Insert a multilayer ceramic capacitor as a bypass capacitor between each pair of the power supply pins. Implement a bypass capacitor as closer to the MCU power supply pins as possible. Use a recommended value of 0.1 μ F as the capacitance of the capacitors. For the capacitors related to crystal oscillation, see section 9, Clock Generation Circuit in the User's Manual: Hardware. For the capacitors related to analog modules, also see section 43, 12-Bit A/D Converter (S12ADE) in the User's Manual: Hardware.

For notes on designing the printed circuit board, see the descriptions of the application note, the Hardware Design Guide (R01AN1411EJ). The latest version can be downloaded from the Renesas Electronics website.

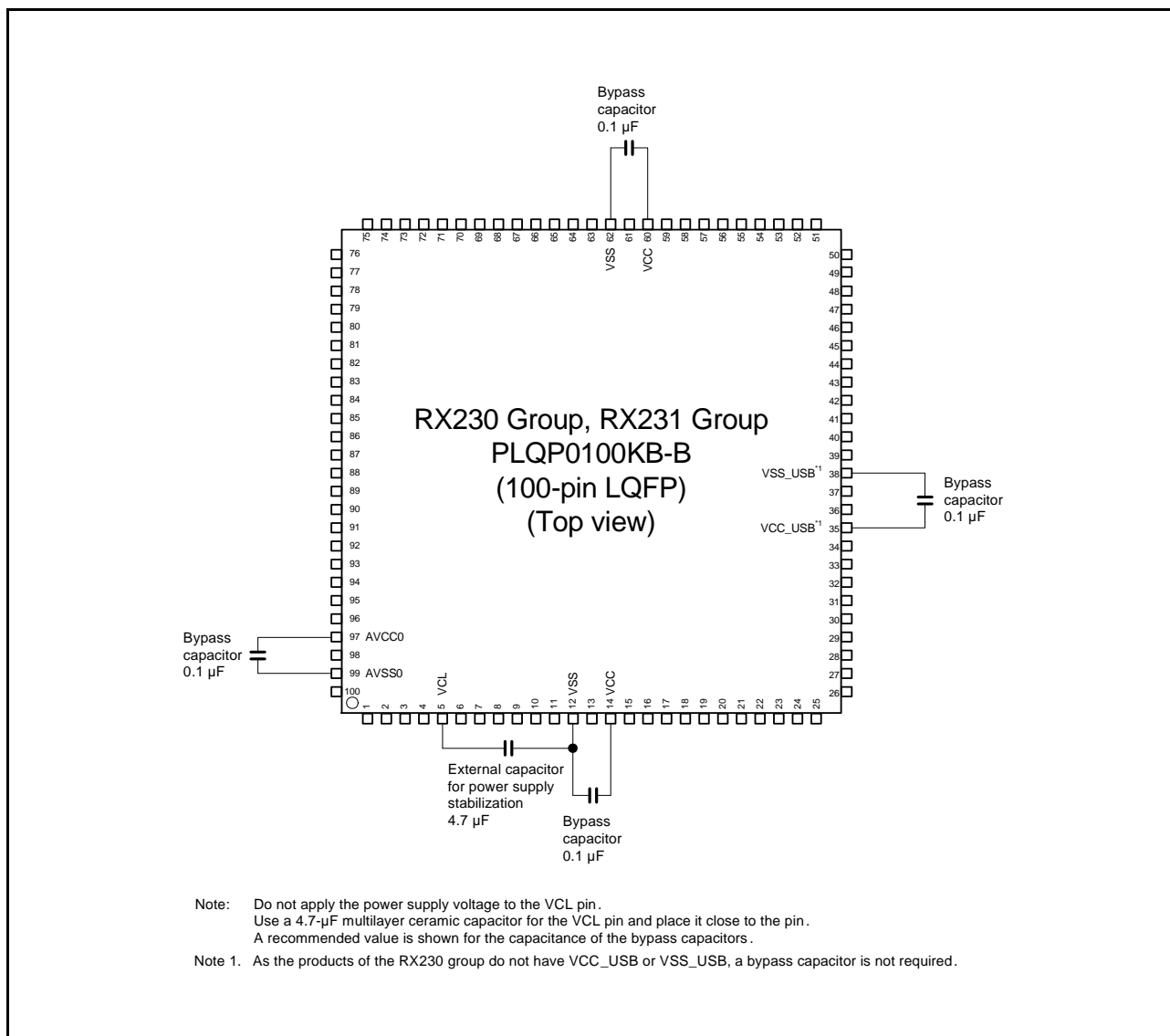


Figure 5.79 Connecting Capacitors (100 Pins)

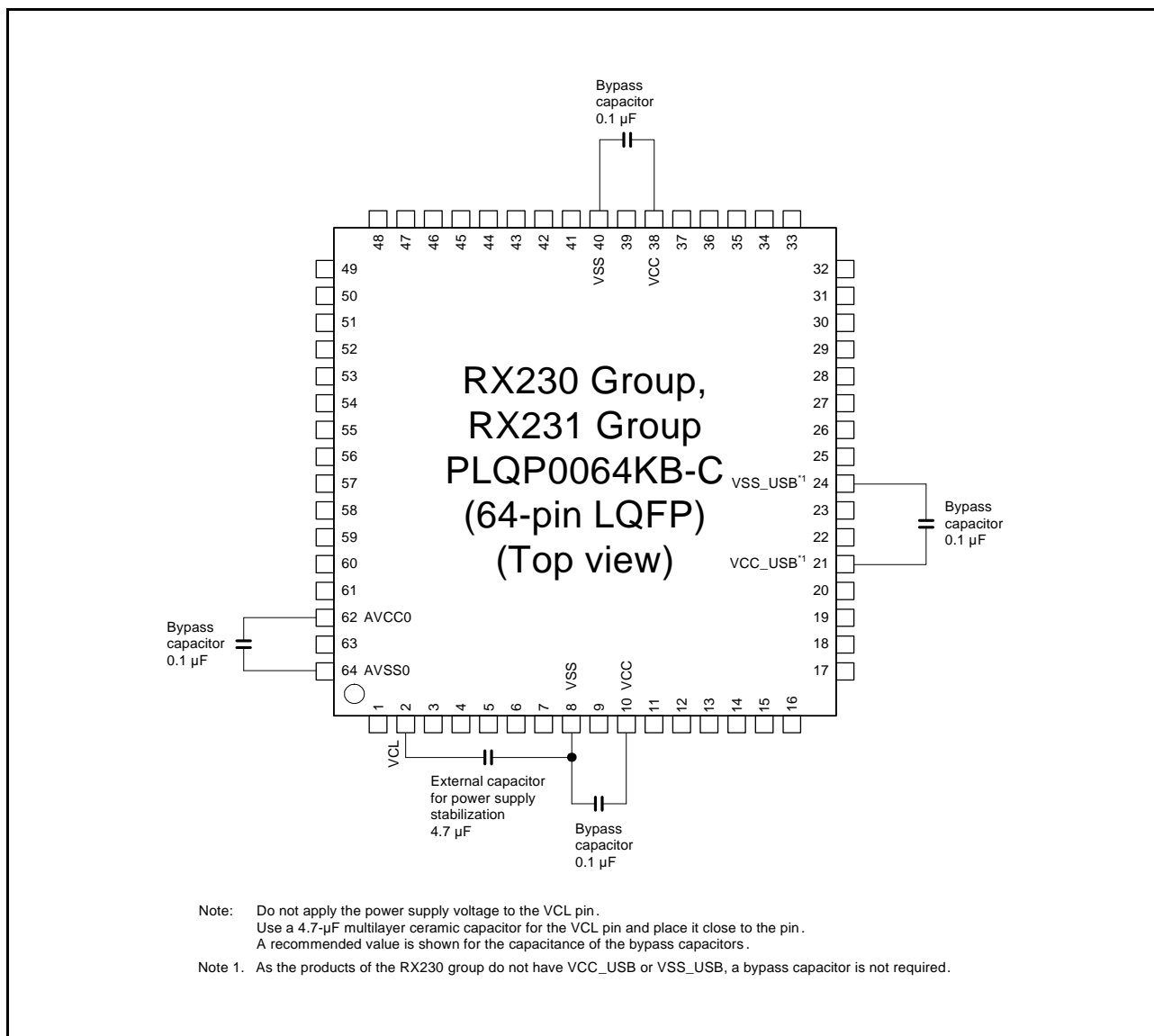


Figure 5.80 Connecting Capacitors (64 Pins)

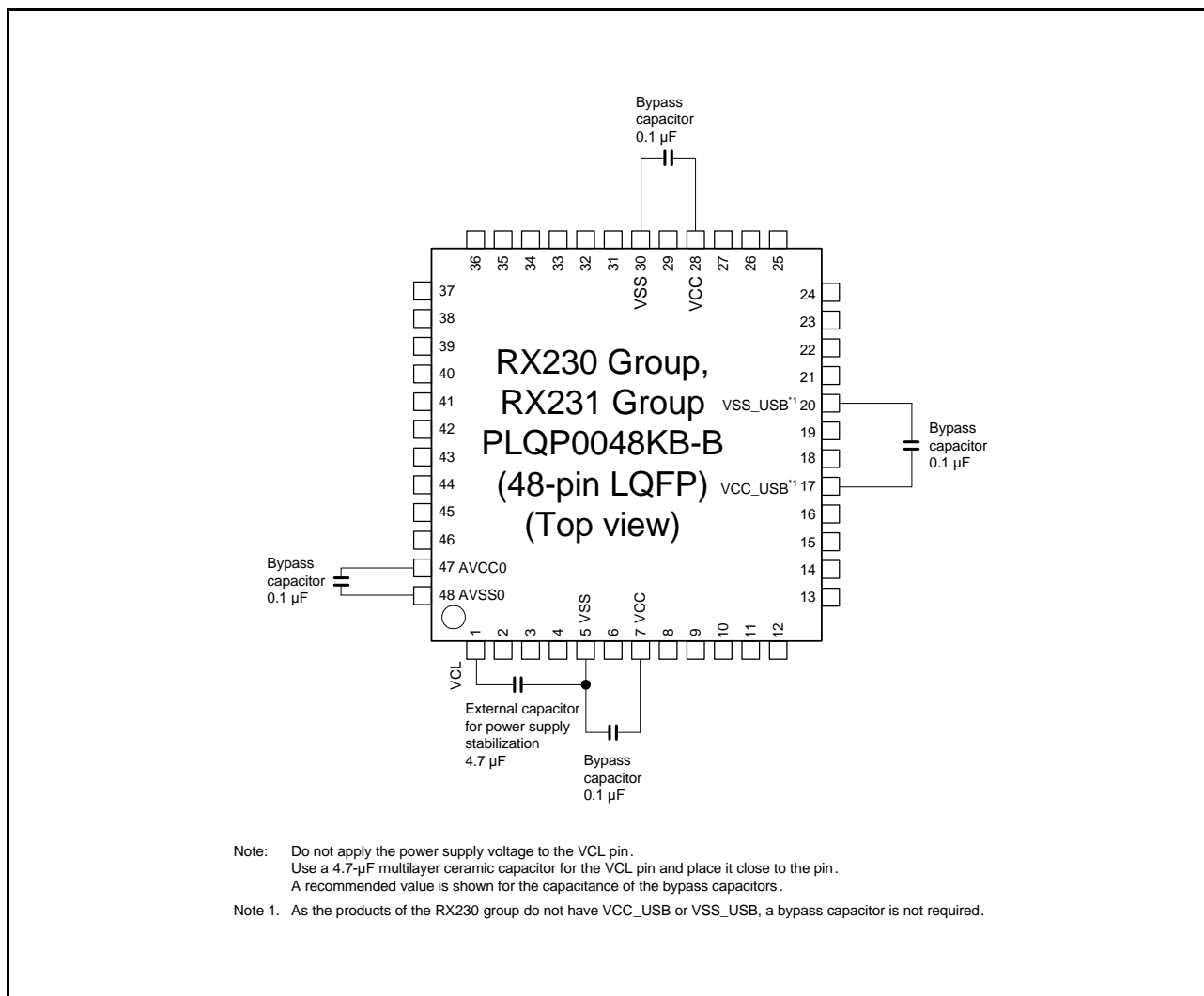


Figure 5.81 Connecting Capacitors (48 Pins)

Appendix 1. Package Dimensions

Information on the latest version of the package dimensions or mountings has been displayed in “Packages” on Renesas Electronics Corporation website.

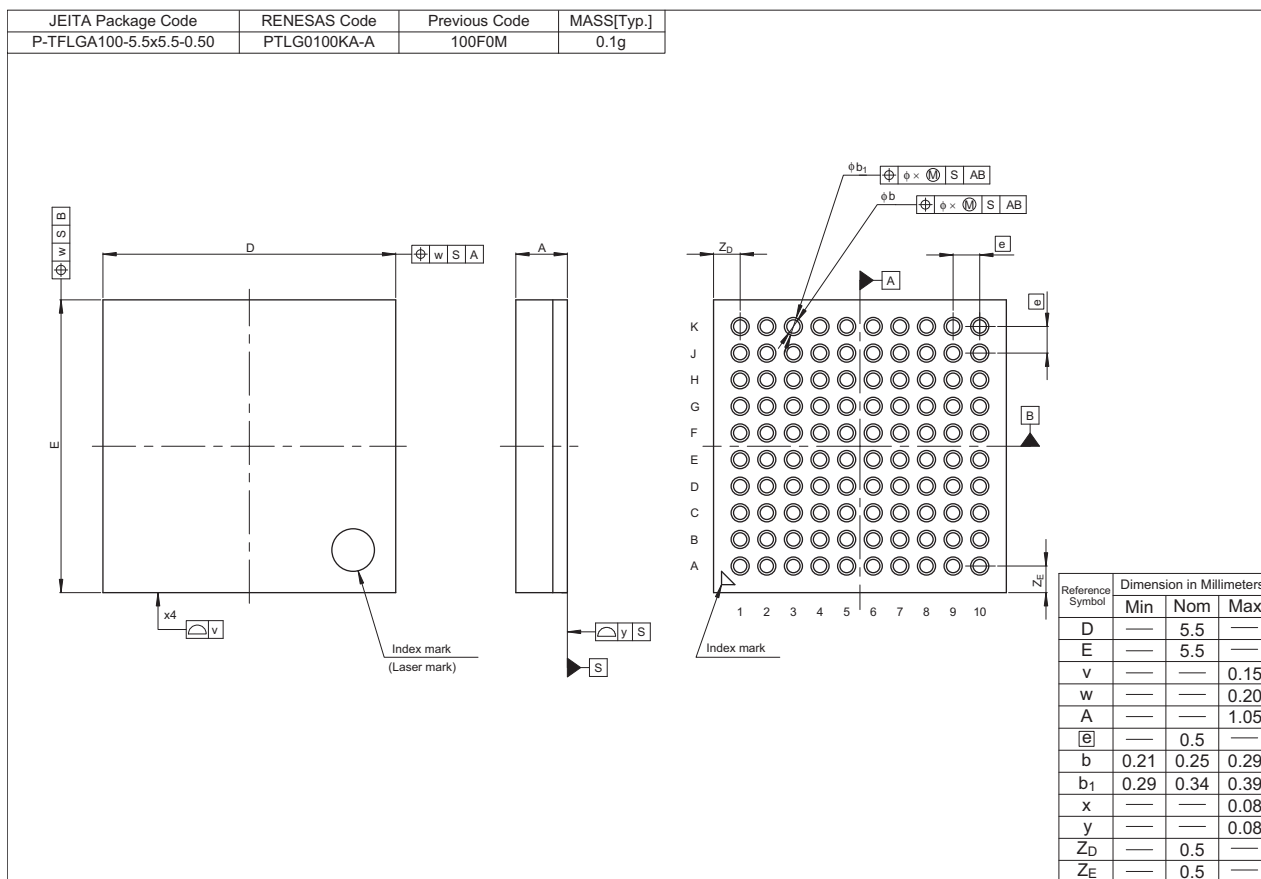


Figure A 100 -Pin TFLGA (PTLG0100KA-A)

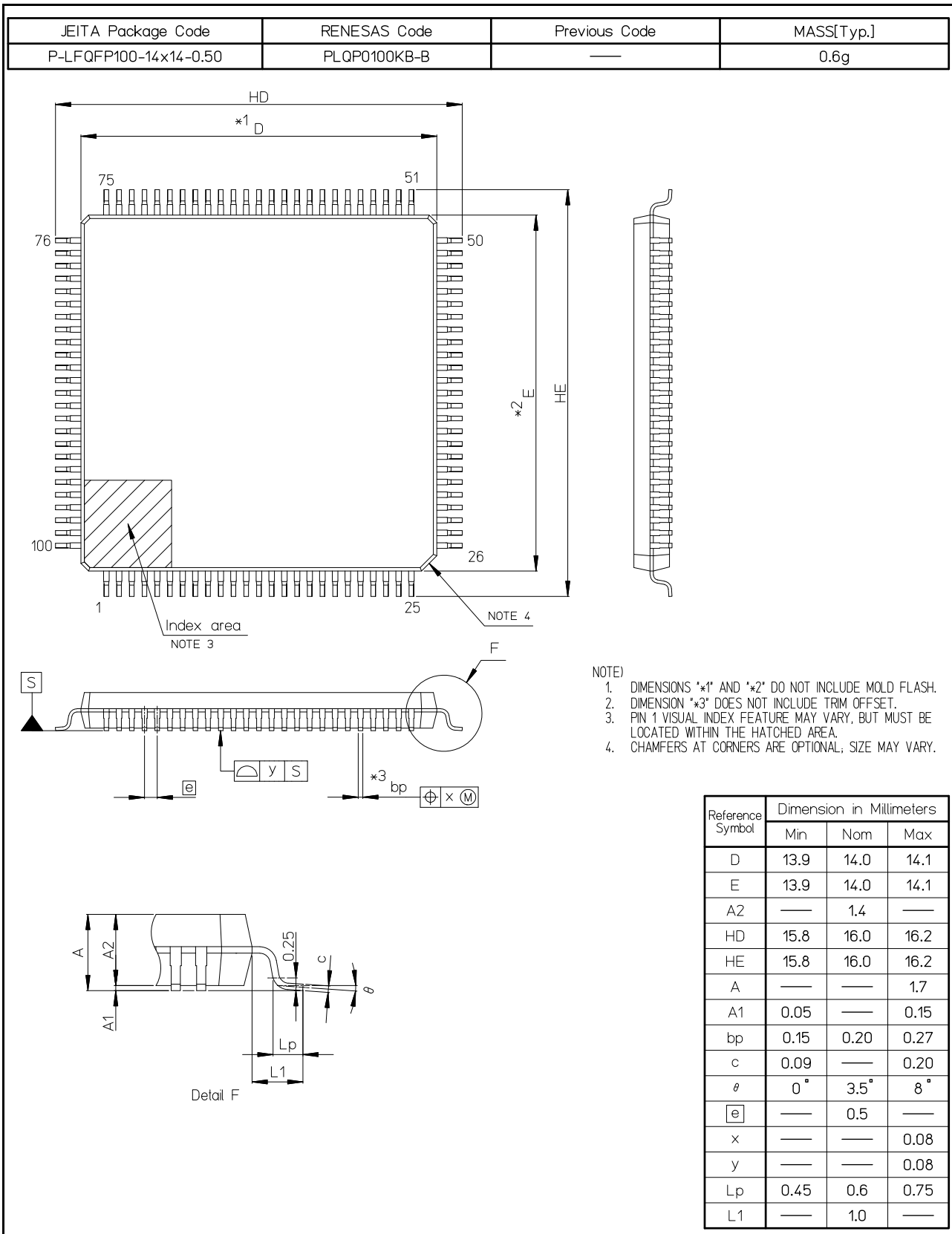


Figure B 100 -Pin LQFP (PLQP0100KB-B)

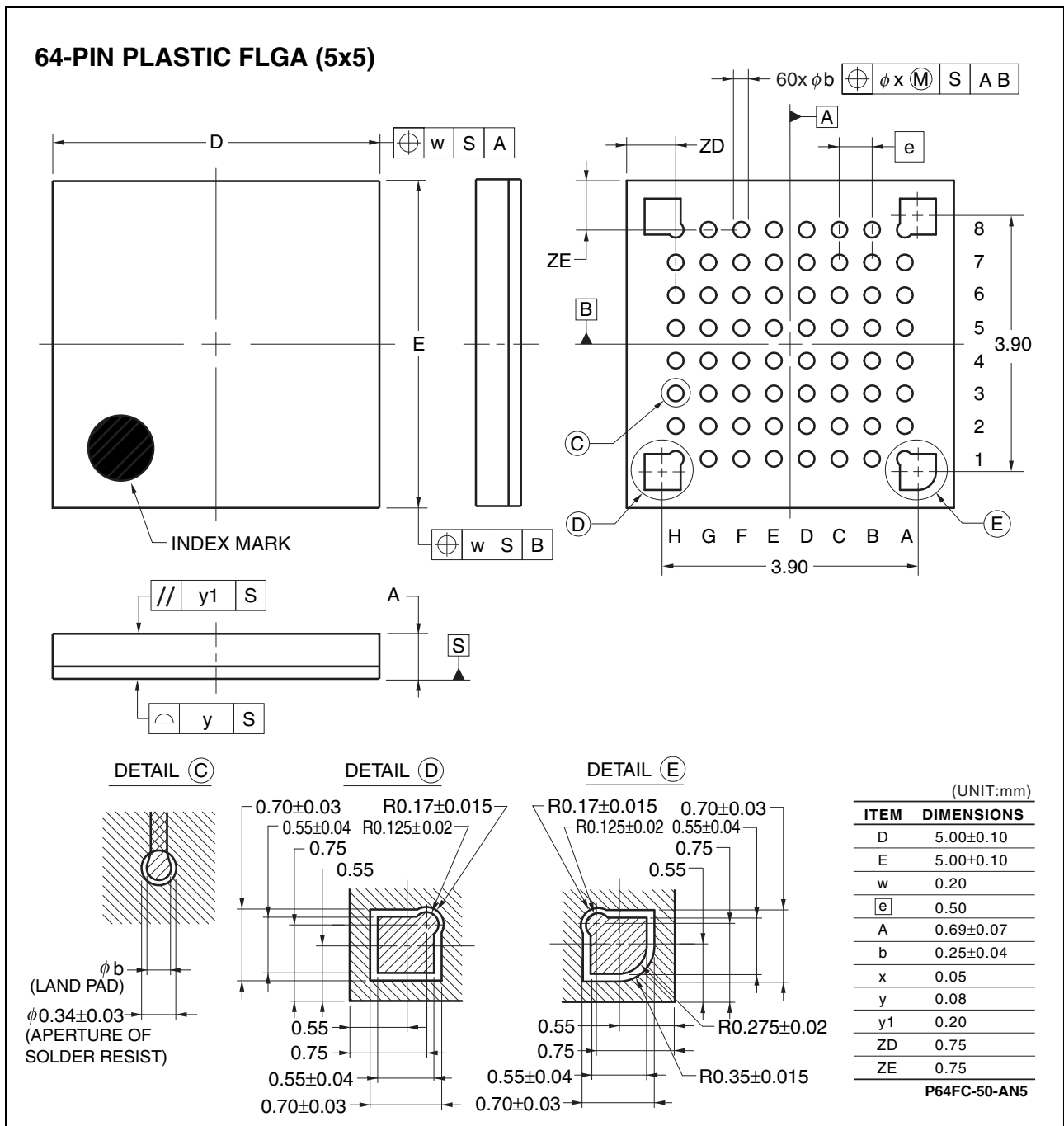
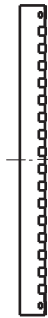
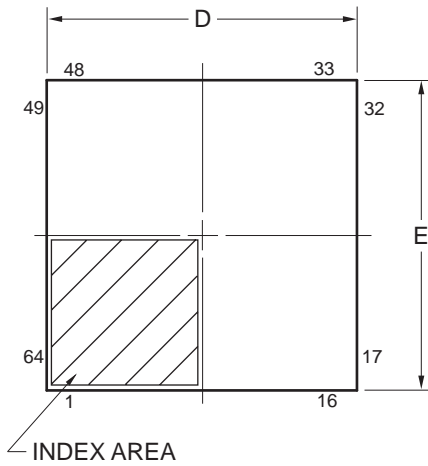
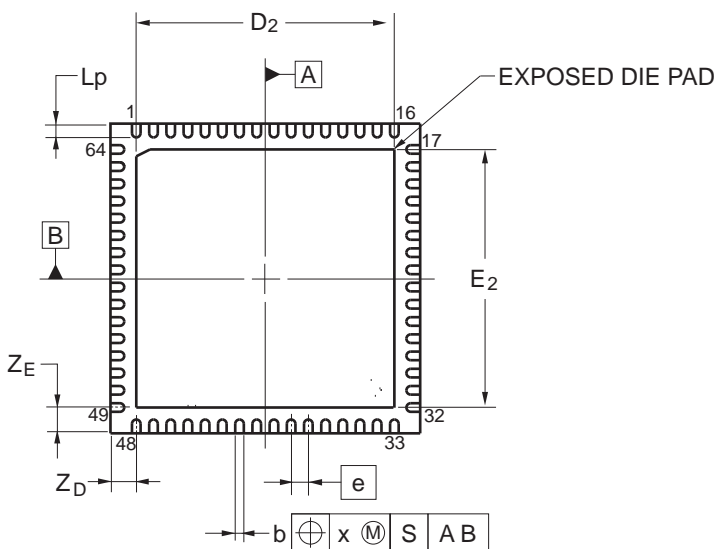
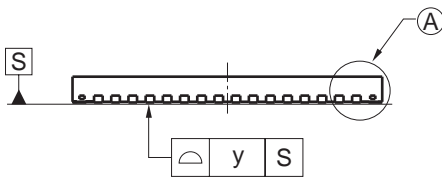
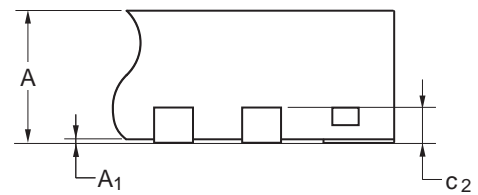


Figure C 64 -Pin WFLGA (PWLG0064KA-A)

JEITA Package code	RENESAS code	Previous code	MASS(TYP.)[g]
P-HWQFN64-9x9-0.50	PWQN0064KC-A	P64K8-50-6B4-5	0.21



DETAIL OF (A) PART



Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	8.95	9.00	9.05
E	8.95	9.00	9.05
A	—	—	0.80
A ₁	0.00	—	—
b	0.18	0.25	0.30
$\text{\textcircled{e}}$	—	0.50	—
L _p	0.30	0.40	0.50
x	—	—	0.05
y	—	—	0.05
Z _D	—	0.75	—
Z _E	—	0.75	—
c ₂	0.15	0.20	0.25
D ₂	—	7.50	—
E ₂	—	7.50	—

Figure D 64 -Pin HWQFN (PWQN0064KC-A)

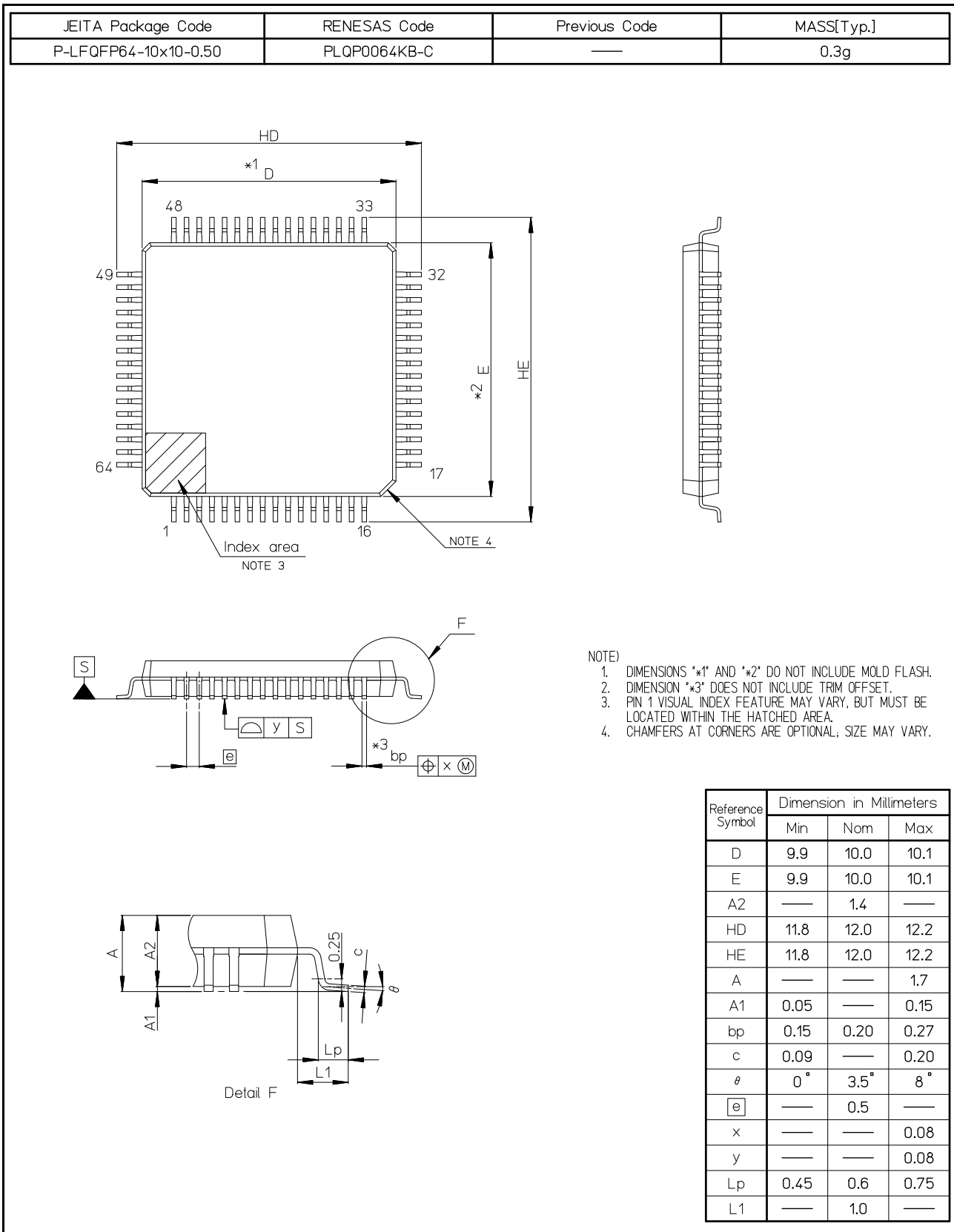
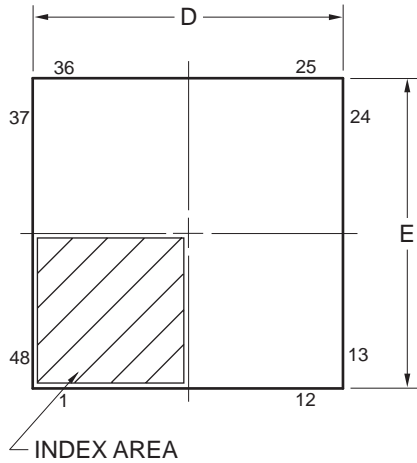
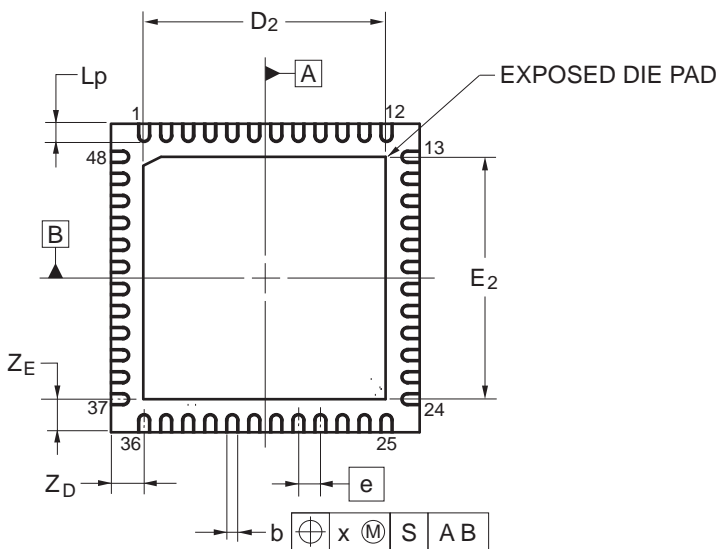
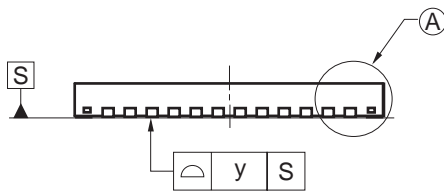
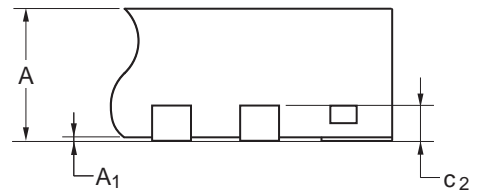


Figure E 64 -Pin LQFP (PLQP0064KB-C)

JEITA Package code	RENESAS code	Previous code	MASS(TYP.)[g]
P-HWQFN48-7x7-0.50	PWQN0048KB-A	48PJN-A P48K8-50-5B4-7	0.13



DETAIL OF (A) PART



Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	6.95	7.00	7.05
E	6.95	7.00	7.05
A	—	—	0.80
A ₁	0.00	—	—
b	0.18	0.25	0.30
e	—	0.50	—
L _p	0.30	0.40	0.50
x	—	—	0.05
y	—	—	0.05
Z _D	—	0.75	—
Z _E	—	0.75	—
c ₂	0.15	0.20	0.25
D ₂	—	5.50	—
E ₂	—	5.50	—

Figure F 48-Pin HWQFN (PWQN0048KB-A)

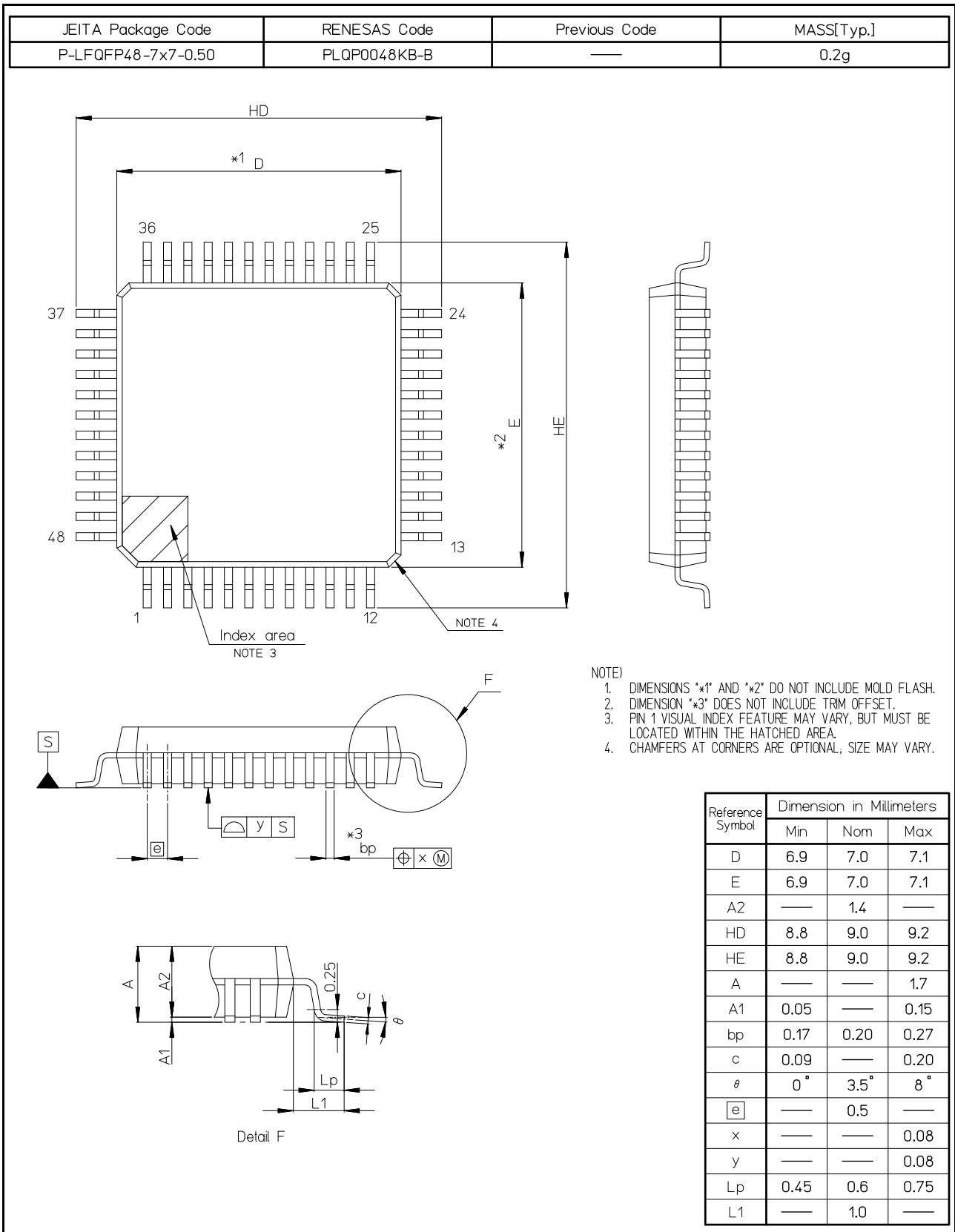


Figure G 48-Pin LQFP (PLQP0048KB-B)

REVISION HISTORY	RX230 Group, RX231 Group Datasheet
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Classifications

- Items with Technical Update document number: Changes according to the corresponding issued Technical Update
- Items without Technical Update document number: Minor changes that do not require Technical Update to be issued

Rev.	Date	Description		Classification
		Page	Summary	
1.00	Jun 24, 2015	—	First edition, issued	
1.10	Oct 30, 2015	1. Overview		
		3	Table 1.1 Outline of Specifications (2/4), changed	
		5	Table 1.1 Outline of Specifications (4/4): SD Host Interface (SDHIA) added	
		6	Table 1.2 Comparison of Functions for Different Packages: RX230 Group added	
		3. Address Space		
		39	Figure 3.1 Memory Map in Each Operating Mode, changed	
		4. I/O Registers		
		67	Table 4.1 List of I/O Registers (Address Order) (25 / 42), changed	TN-RX*-A139A/E
		83	Table 4.1 List of I/O Registers (Address Order) (41 / 42), changed	
		5. Electrical Characteristics		
		85	Table 5.1 Absolute Maximum Ratings, changed	TN-RX*-A137A/E
		86	Table 5.2 Recommended Operating Voltage Conditions, changed	
		87	Table 5.3 DC Characteristics (1), changed	TN-RX*-A137A/E
		88	Table 5.4 DC Characteristics (2), changed	
		88	Table 5.5 DC Characteristics (3), changed	
		89	Table 5.7 DC Characteristics (5), changed	
		91	Figure 5.1 Voltage Dependency in High-Speed Operating Mode (Reference Data), changed	
		92	Figure 5.2 Voltage Dependency in Middle-Speed Operating Mode (Reference Data), changed	
		93	Figure 5.3 Voltage Dependency in Low-Speed Operating Mode (Reference Data), changed	TN-RX*-A137A/E
		94	Table 5.8 DC Characteristics (6), changed Figure 5.4 Voltage Dependency in Software Standby Mode (Reference Data), changed	
		95	Figure 5.5 Temperature Dependency in Software Standby Mode (Reference Data), changed	
		96	Figure 5.6 Temperature Dependency of RTC Operation with VCC Off (Reference Data), changed Table 5.10 DC Characteristics (8): Conditions changed	
		97	Table 5.11 DC Characteristics (9), changed	TN-RX*-A137A/E
		99	Table 5.16 Permissible Output Currents (1), changed	TN-RX*-A137A/E
		100	Table 5.17 Permissible Output Currents (2), changed	
		101	Table 5.18 Output Values of Voltage (1), changed	
		101	Table 5.19 Output Values of Voltage (2), changed	TN-RX*-A137A/E
101	Table 5.20 Output Values of Voltage (3), changed	TN-RX*-A137A/E		
105	Figure 5.13 VOH/VOL and IOH/IOL Voltage Characteristics at Ta = 25°C When High-Drive Output is Selected (Reference Data), changed	TN-RX*-A137A/E		
108	Figure 5.18 VOL and IOL Voltage Characteristics of RIIC Output Pin at Ta = 25°C (Reference Data)	TN-RX*-A137A/E		
110	Table 5.21 Operating Frequency Value (High-Speed Operating Mode) and Table 5.22 Operating Frequency Value (Middle-Speed Operating Mode), changed	TN-RX*-A137A/E		
112	Table 5.26 Clock Timing, changed	TN-RX*-A137A/E		
116	Table 5.27 Reset Timing, changed			
131	Table 5.41 Timing of On-Chip Peripheral Modules (4): Note changed			
132	Table 5.43 Timing of On-Chip Peripheral Modules (6), changed			
138	Figure 5.61 SSI Transmission/Reception Timing (SSICP.SCKP=0), changed	TN-RX*-A137A/E		
139	Figure 5.62 SSI Transmission/Reception Timing (SSICP.SCKP=1), changed	TN-RX*-A137A/E		
142	Figure 5.66 VREFH0 Voltage Range vs. AVCC0, changed			

Rev.	Date	Description		Classification	
		Page	Summary		
1.10	Oct 30, 2015	142	Table 5.45 A/D Conversion Characteristics (1): Conditions and Voltage Range of Analog Input (Max.), changed		
		143	Table 5.46 A/D Conversion Characteristics (2): Conditions changed		
		144	Table 5.47 A/D Conversion Characteristics (3): Conditions changed		
		145	Table 5.48 A/D Conversion Characteristics (4): Conditions changed		
		146	Table 5.49 A/D Conversion Characteristics (5): Conditions changed and Absolute accuracy (Test Conditions) deleted		
		153	Table 5.57 Characteristics of Power-On Reset Circuit and Voltage Detection Circuit (1), changed	TN-RX*-A137A/E	
		154	Table 5.58 Characteristics of Power-On Reset Circuit and Voltage Detection Circuit (2), changed		
		155	Figure 5.73 Power-On Reset Timing and Figure 5.74 Voltage Detection Circuit Timing (Vdet0), changed		
		159	Table 5.62 ROM (Flash Memory for Code Storage) Characteristics (2) High-Speed Operating Mode: Note changed		
		160	Table 5.63 ROM (Flash Memory for Code Storage) Characteristics (3) Middle-Speed Operating Mode: Note changed		
		161	Table 5.65 E2 DataFlash Characteristics (2): high-speed operating mode, Note changed		
		161	Table 5.66 E2 DataFlash Characteristics (3): middle-speed operating mode, Conditions and Note changed		
		163	Figure 5.79 Connecting Capacitors (100 Pins), changed		
		164	Figure 5.80 Connecting Capacitors (64 Pins), changed		
		165	Figure 5.81 Connecting Capacitors (48 Pins), changed		
		Appendix 1. Package Dimensions			
		167	Figure B 100 -Pin LQFP (PLQP0100KB-B), changed	TN-RX*-A137A/E	
		170	Figure E 64 -Pin LQFP (PLQP0064KB-C), changed	TN-RX*-A137A/E	
		172	Figure G 48 -Pin LQFP (PLQP0048KB-B), changed	TN-RX*-A137A/E	

NOTES FOR CMOS DEVICES

- (1) **VOLTAGE APPLICATION WAVEFORM AT INPUT PIN:** Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between VIL (MAX) and VIH (MIN) due to noise, etc., the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between VIL (MAX) and VIH (MIN).
- (2) **HANDLING OF UNUSED INPUT PINS:** Unconnected CMOS device inputs can be cause of malfunction. If an input pin is unconnected, it is possible that an internal input level may be generated due to noise, etc., causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using pull-up or pull-down circuitry. Each unused pin should be connected to VDD or GND via a resistor if there is a possibility that it will be an output pin. All handling related to unused pins must be judged separately for each device and according to related specifications governing the device.
- (3) **PRECAUTION AGAINST ESD:** A strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it when it has occurred. Environmental control must be adequate. When it is dry, a humidifier should be used. It is recommended to avoid using insulators that easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors should be grounded. The operator should be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with mounted semiconductor devices.
- (4) **STATUS BEFORE INITIALIZATION:** Power-on does not necessarily define the initial status of a MOS device. Immediately after the power source is turned ON, devices with reset functions have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. A device is not initialized until the reset signal is received. A reset operation must be executed immediately after power-on for devices with reset functions.
- (5) **POWER ON/OFF SEQUENCE:** In the case of a device that uses different power supplies for the internal operation and external interface, as a rule, switch on the external power supply after switching on the internal power supply. When switching the power supply off, as a rule, switch off the external power supply and then the internal power supply. Use of the reverse power on/off sequences may result in the application of an overvoltage to the internal elements of the device, causing malfunction and degradation of internal elements due to the passage of an abnormal current. The correct power on/off sequence must be judged separately for each device and according to related specifications governing the device.
- (6) **INPUT OF SIGNAL DURING POWER OFF STATE :** Do not input signals or an I/O pull-up power supply while the device is not powered. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Input of signals during the power off state must be judged separately for each device and according to related specifications governing the device.

General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Handling of Unused Pins

Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.

- The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

The state of the product is undefined at the moment when power is supplied.

- The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.

In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

Access to reserved addresses is prohibited.

- The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

- When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

Before changing from one product to another, i.e. to a product with a different part number, confirm that the change will not lead to problems.

- The characteristics of an MPU or MCU in the same group but having a different part number may differ in terms of the internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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Renesas Electronics America Inc.
2801 Scott Boulevard Santa Clara, CA 95050-2549, U.S.A.
Tel: +1-408-588-6000, Fax: +1-408-588-6130

Renesas Electronics Canada Limited
9251 Yonge Street, Suite 8309 Richmond Hill, Ontario Canada L4C 9T3
Tel: +1-905-237-2004

Renesas Electronics Europe Limited
Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K
Tel: +44-1628-585-100, Fax: +44-1628-585-900

Renesas Electronics Europe GmbH
Arcadiastrasse 10, 40472 Düsseldorf, Germany
Tel: +49-211-6503-0, Fax: +49-211-6503-1327

Renesas Electronics (China) Co., Ltd.
Room 1709, Quantum Plaza, No.27 ZhichunLu Haidian District, Beijing 100191, P.R.China
Tel: +86-10-8235-1155, Fax: +86-10-8235-7679

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Unit 301, Tower A, Central Towers, 555 Langao Road, Putuo District, Shanghai, P. R. China 200333
Tel: +86-21-2226-0888, Fax: +86-21-2226-0899

Renesas Electronics Hong Kong Limited
Unit 1601-1611, 16/F., Tower 2, Grand Century Place, 193 Prince Edward Road West, Mongkok, Kowloon, Hong Kong
Tel: +852-2265-6688, Fax: +852-2886-9022

Renesas Electronics Taiwan Co., Ltd.
13F, No. 363, Fu Shing North Road, Taipei 10543, Taiwan
Tel: +886-2-8175-9600, Fax: +886-2-8175-9670

Renesas Electronics Singapore Pte. Ltd.
80 Bendemeer Road, Unit #06-02 Hyflux Innovation Centre, Singapore 339949
Tel: +65-6213-0200, Fax: +65-6213-0300

Renesas Electronics Malaysia Sdn.Bhd.
Unit 1207, Block B, Menara Amcorp, Amcorp Trade Centre, No. 18, Jln Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia
Tel: +60-3-7955-9390, Fax: +60-3-7955-9510

Renesas Electronics India Pvt. Ltd.
No.777C, 100 Feet Road, HAL II Stage, Indiranagar, Bangalore, India
Tel: +91-80-67208700, Fax: +91-80-67208777

Renesas Electronics Korea Co., Ltd.
12F., 234 Teheran-ro, Gangnam-Gu, Seoul, 135-080, Korea
Tel: +82-2-558-3737, Fax: +82-2-558-5141