SAMA5D3 series-EK

User Guide

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Section 1

Introduction 1-1

1.1 Scope 1-1

1.2 Applicable Documents 1-1

Section 2

Kit Contents 2-1

2.1 Deliverables 2-1

2.2 Evaluation Board Specifications 2-3

2.3 Electrostatic Warning 2-3

Section 3

Power Up 3-1

3.1 Power up the Board 3-1

3.2 Sample Code and Technical Support 3-1

Section 4

Evaluation Kit Hardware 4-1

4.1 Introduction 4-1

Section 5

Computer Module (CM) 5-1

5.1 Board Overview 5-1

5.2 Equipment List 5-5

5.2.1 Devices 5-5

5.2.2 Interface Connection 5-5

5.2.3 Configuration Items 5-5

5.2.4 Boot Options 5-6

5.3 Functional Blocks 5-6

5.3.1 Processor 5-6

5.3.2 Clock Circuitry 5-7

5.3.3 Reset Circuitry 5-7

5.3.4 Power Supplies 5-7

5.3.5 Memory 5-11

5.3.6 Serial Peripheral Interface Controller (SPI) 5-14

5.3.7 1-Wire EEPROM 5-16

5.3.8 Tri-Speed Ethernet PHY 5-17

5.3.9 Indicators 5-19

5.3.10 SODIMM200 Interface 5-20

5.3.11 Connectors 5-20

5.4 EMBEST Schematics 5-21

5.5 RONETIX Schematics 5-22

Section 6

Main Board (MB).....6-1
6.1 Main Board Overview..... 6-1
6.1.1 Equipment List..... 6-3
6.1.2 Technical specifications..... 6-3
6.1.3 Devices..... 6-4
6.1.4 Board Interface Connection..... 6-4
6.2 Function Blocks..... 6-5
6.2.1 Processor..... 6-5
6.2.2 Power Supplies..... 6-7
6.2.3 Debug JTAG/ICE and DBGU..... 6-8
6.2.4 USART..... 6-9
6.2.5 USB Ports..... 6-10
6.2.6 Ethernet 10/100 (EMAC) Port..... 6-11
6.2.7 Audio..... 6-13
6.2.8 HDMI Transmitter Interface..... 6-14
6.2.9 1-Wire EEPROM..... 6-15
6.2.10 CAN Bus..... 6-15
6.2.11 Smart DAA..... 6-16
6.2.12 SD/MMC Interface..... 6-17
6.2.13 ZigBee..... 6-18
6.2.14 LED Indicators..... 6-18
6.2.15 Push Button Switches..... 6-18
6.2.16 Analog Reference..... 6-19
6.2.17 Expansion Ports..... 6-20
6.3 Configuration..... 6-22
6.4 PIO Usage and Interface Connectors Details..... 6-23
6.4.1 Power supply..... 6-23
6.4.2 JTAG/ICE Connector..... 6-24
6.4.3 USB Type A Dual Port..... 6-25
6.4.4 USB MicroAB..... 6-26
6.4.5 JTAG OB USB MicroAB..... 6-27
6.4.6 HDMI Connector..... 6-27
6.4.7 RS232 Connector with RTS/CTS Handshake Support..... 6-28
6.4.8 DAA RJ11 Socket (6P4C)..... 6-29
6.4.9 CAN RJ12 Socket (6P6C)..... 6-29
6.4.10 SD/MMC Plus MCI0..... 6-30
6.4.11 MicroSD MCI1..... 6-31
6.4.12 Gigabit Ethernet ETH0 RJ45 Socket J17..... 6-32
6.4.13 Ethernet ETH1 RJ45 Socket J24..... 6-32
6.4.14 ZigBee Socket J10..... 6-32

6.4.15 LCD Socket J21 6-33
6.4.16 LCD/TSC Socket J22 6-34
6.4.17 ISI Socket J11 6-35
6.4.18 PIO Usage 6-36
6.4.19 IO Expansion Port J1 6-41
6.4.20 IO Expansion Port J2 6-42
6.4.21 IO Expansion Port J3 6-43
6.4.22 SODIMM Card Edge Socket 6-44
6.5 Schematics 6-48

Section 7

Optional Display Module (DM) 7-1
7.1 DM Board Overview 7-1
7.1.1 Equipment List 7-2
7.1.2 Function Blocks 7-2
7.1.3 TFT LCD with Touch Panel 7-3
7.1.4 Back Light 7-4
7.1.5 QTouch 7-4
7.1.6 One-Wire 7-5
7.2 Schematics 7-5

Section 8

Troubleshooting and Recommendations 8-1
8.1 Page Intentionally Left Blank 8-1

Section 9

Revision History 9-1
9.1 Revision History 9-1

Section 1

Introduction

1.1 Scope

This User Guide introduces the Evaluation Kit and describes the development and debugging capabilities running on the SAMA5D3 series ARM®-based Embedded MPUs as listed below :

- SAMA5D31
- SAMA5D33
- SAMA5D34
- SAMA5D35

The User Guide pertains to the following Evaluation Kit references:

- SAMA5D31-EK
- SAMA5D33-EK
- SAMA5D34-EK
- SAMA5D35-EK

This guide gives details on the Evaluation Kit and is made up of 9 sections:

- Section 1 includes a photo of the board, device and kit references, applicable documents
- Section 2 describes the kit contents, its main features
- Section 3 provides instructions to power up the Evaluation Kit and describes how to use it.
- Section 4 Evaluation Kit hardware summary
- Section 5 describes the Computer Module (CM)
- Section 6 describes the Main Board (MB)
- Section 7 describes the optional Display Module (DM)
- Section 8 gives troubleshooting recommendations
- Section 9 revision history

1.2 Applicable Documents

Table 1-1. References and Applicable Documents

Title	Comment
SAMA5D3 series Datasheet	Literature number 11121

Section 2

Kit Contents

2.1 Deliverables

The Evaluation Kit includes:

- Boards
  - One SAMA5D3 series-MB (Main Board)
  - One of the four available CPU modules (CM)
    - SAMA5D31-CM
    - SAMA5D33-CM
    - SAMA5D34-CM
    - SAMA5D35-CM
  - One optional Display Module (DM) board 5"_WVGA_R-DM featured in SAMA5D31 /SAMA5D33/ SAMA5D34 kits only
- Power supply
  - One universal input AC/DC power supply with US, Europe and UK plug adapters
  - One 3V Lithium Battery type CR1225
- Cables
  - One micro A/B-type USB cable
  - One RJ45 crossed cable
- A Welcome Letter

Figure 2-1. Unpacked SAMA5D3 series-EK

Unpack and inspect the kit carefully. Contact your local Atmel® distributor, should you have issues concerning the contents of the kit.

2.2 Evaluation Board Specifications

Table 2-1. Evaluation Kit Specifications

Characteristic	Specifications
Clock speed	Up to 536 MHz PCK, up to 166 MHz MCK
Ports	10/100/1000 Ethernet, USB, RS232, JTAG, CAN, Audio, HDMI, SD card
Board supply voltage	5V DC from connector
Temperature: operating storage	 0°C to +60°C -40°C to +85°C
Relative humidity	0 to 90% (non condensing)
Dimensions: MB (Main Board) CM (Computer Module) DM (Display Module)	 165 * 135 * 20 mm 67.60 * (40 to 47) * 5 mm 135 * 80 * 6 mm
RoHS status	Compliant
Board Identification	SAMA5D31-EK, SAMA5D33-EK, SAMA5D34-EK, SAMA5D35-EK.

2.3 Electrostatic Warning

WARNING: ESD-Sensitive Electronic Equipment!

The Evaluation Kit is shipped in a protective anti-static package. The board system must not be subjected to high electrostatic potentials.

We strongly recommend using a grounding strap or similar ESD protective device when handling the board in hostile ESD environments (offices with synthetic carpet, for example). Avoid touching the component pins or any other metallic element on the board.

Section 3

Power Up

3.1 Power up the Board

Unpack the board taking care to avoid electrostatic discharge. Unpack the power supply, select the right power plug adapter corresponding to that of your country, and insert it in the power supply.

Connect the power supply DC connector to the board and plug the power supply to an AC power plug.

The board LCD should light up and display a welcome page. Then, click or touch icons displayed on the screen and enjoy the demo (the red ones need to be replaced by demo software).

3.2 Sample Code and Technical Support

After boot up, you can run some sample code or your own application on the development kit. You can download sample code and get technical support from the Atmel website:

http://www.atmel.com/products/at91/

Linux software and demos can be found on linux4sam website:

http://www.at91.com/linux4sam/bin/view/Linux4SAM/SAMA5D3xDemo

Section 4

Evaluation Kit Hardware

4.1 Introduction

The Atmel SAMA5D3 series Evaluation Kit is a fully-featured evaluation platform for the Atmel SAMA5D3 series microcontroller. The evaluation kit allows users to extensively evaluate, prototype and create application-specific designs.

The Atmel SAMA5D3 series Evaluation Kit is a new platform architecture based on a Main Board, five Computer Modules equipped with a SAMA5D3 series processor and an optional Display Module which provides a maximum of flexibility regarding its usage.

The SAMA5D3 series Evaluation Kit consists of three boards:

- The Computer Module board (CM), is a single-board-computer that integrates all the core components and is mounted onto an application specific main board (MB). The Computer Module have specified pinouts based on the SODIMM200 connector. It provides the functional requirements for an embedded application. These functions include, but are not limited to, graphics, audio, mass storage, network and multiple serial and USB ports. A single SODIMM200 connector provides the main board interface to carry all the I/O signals to and from the Computer Module.
- The Main Board (MB) provides all the interface connectors required to attach the system to the application specific peripherals. This versatility allows the designer to create a densely packed solution, which results in a more reliable product while simplifying system integration.
- The Display Module board (DM) integrates LCD, TouchScreen and Qtouch® technology

Table 4-1. Features Provided on the Evaluation Kit:

Feature	D31	D33	D34	D35
CAN0			X	X
CAN1			X	X
GMAC		X	X	X
EMAC	X			X
HSMCI1	X	X	X	X
HSMCI2		X	X	X
LCDC	X	X	X	
UART0	X			X
UART1	X			X
ISI	X	X	X	X
SHA	X	X	X	X
AES	X	X	X	X
TDES	X	X	X	X
TC1	X	X	X	X

Section 5

Computer Module (CM)

5.1 Board Overview

The CM (CPU Module) board is the heart of the system. It connects to the Main Board through a SO-DIMM200 interface. It carries the SAMA5D3 series processor and external memories. The CM board serves as a minimal CPU sub-system. All the 4 processors SAMA5D31/SAMA5D33/SAMA5D34/SAMA5D35 share the same CM circuitry with minor configuration settings.

The CM connects to a carrier board containing its connectors, power supply and any expansion I/O, through a standard gold-plated SODIMM 200-pin connection.

Note: There are four CM boards from two different manufacturers. The four processors are implemented as shown in Table 5-1 below:

Table 5-1. CM Board Implementation

Manufacturer & Module Kind	SAMA5D31-CM	SAMA5D33-CM	SAMA5D34-CM	SAMA5D35-CM
EMBEST	X		X	
RONETIX		X		X

The four CM boards share the same circuitry design with different designator information and PCB lay-outs. The circuitry reference in this guide, for common design parts, refers to schematics from SAMA5D3 series-CM (mfg2). All the other schematics are provided in the Section 5.4 ”EMBEST Schematics” on page 5-21 and Section 5.5 ”RONETIX Schematics” on page 5-22.

Figure 5-1. CM from EMBEST

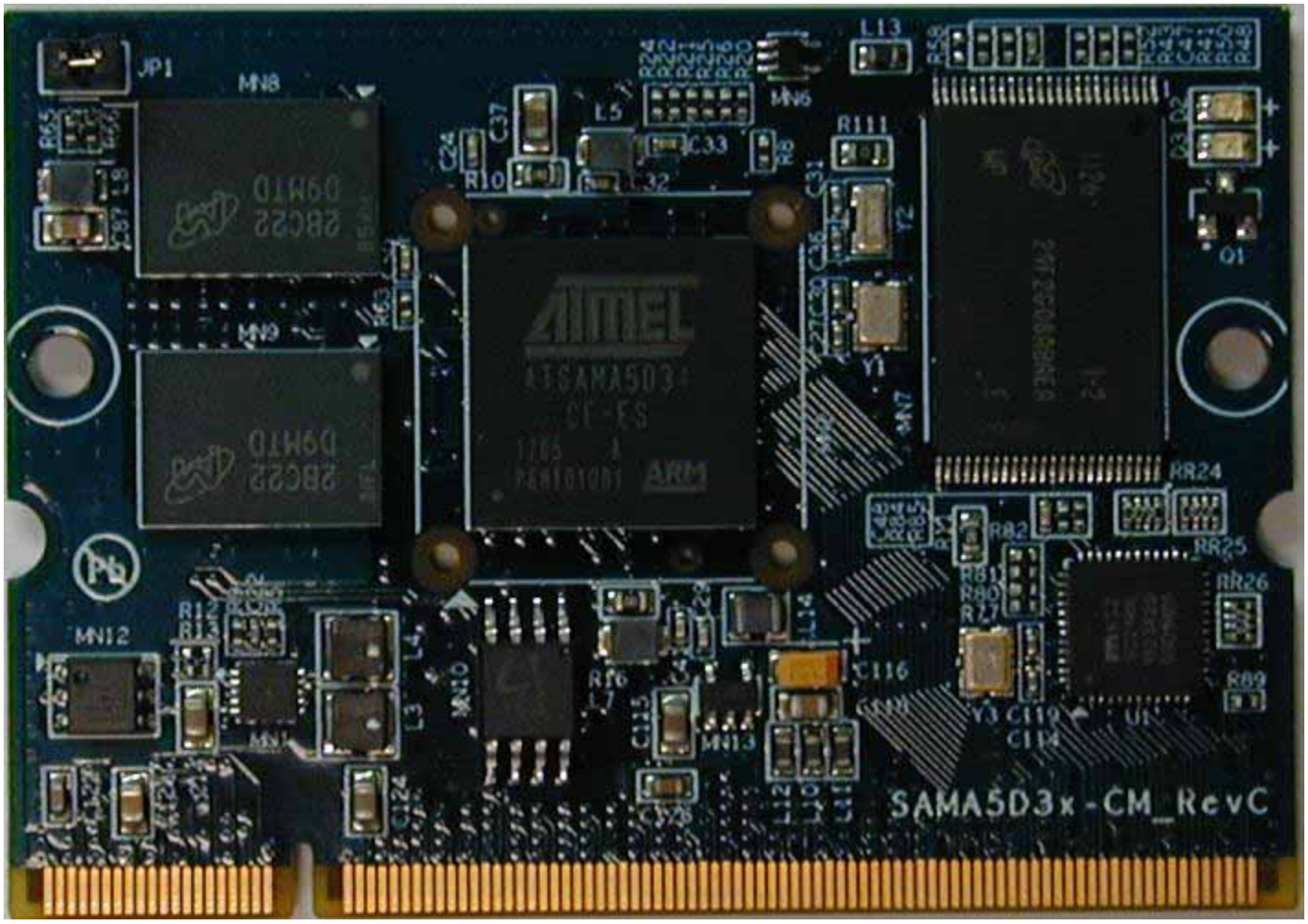


Figure 5-2. CM from RONETIX

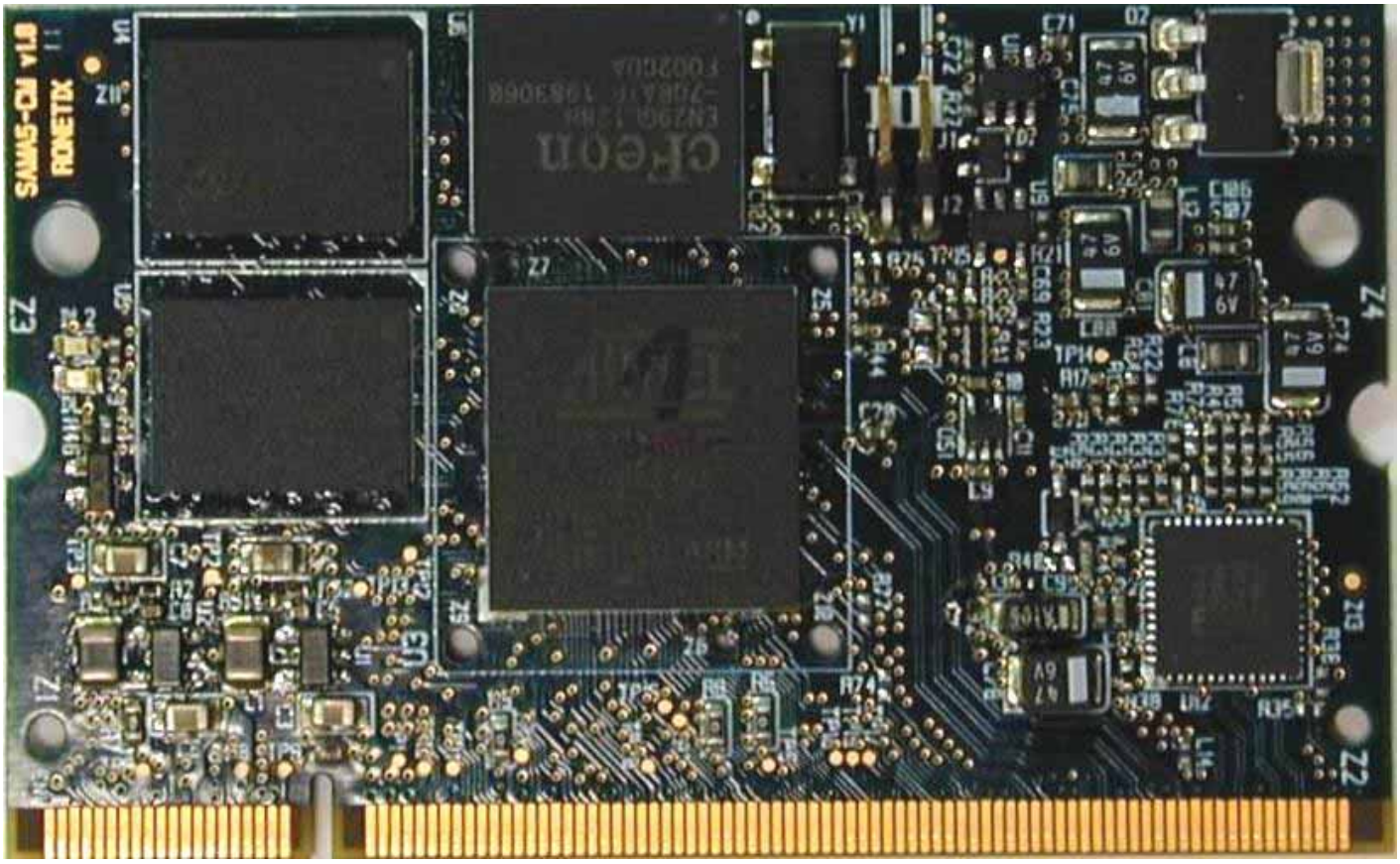
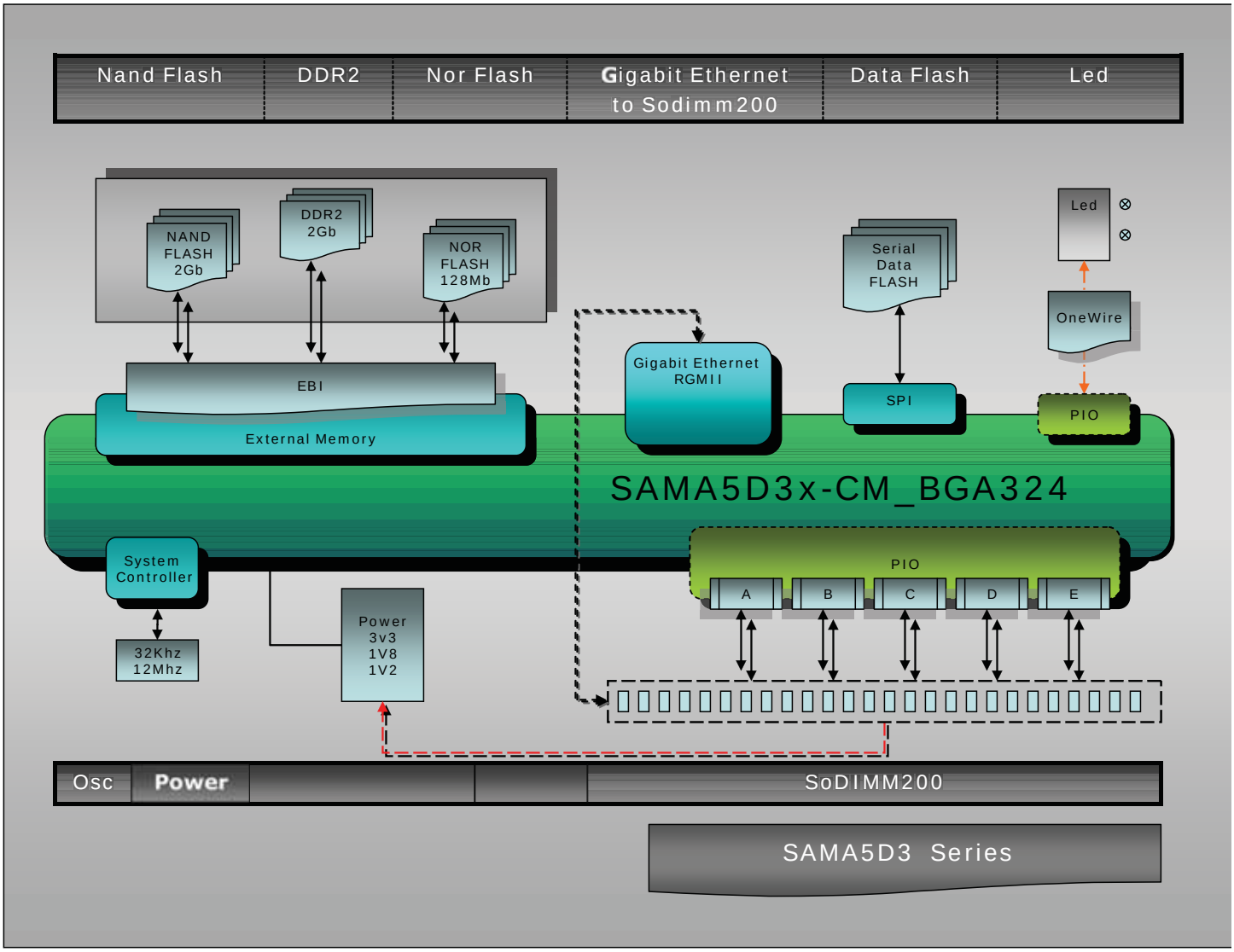


Figure 5-3. Board Architecture



Note: Different interfaces on the main board share the same connections to the CPU module. Therefore the actual usage depends on the CPU module featured in your evaluation kit.

5.2 Equipment List

The CM board is built around a Cortex A5-based microcontroller (BGA 324 package) with external memory and Gigabit Ethernet PHYsical Layer Transceiver.

5.2.1 Devices

Table 5-2. CM Board Specifications

Characteristic	Specifications
PCB	CPU Module (10 layers)
Dimensions in mm: (L x W x H)	 67.60 *(40 to 47) * 5 max
Processor	SAMA5D31, SAMA5D33, SAMA5D34, and SAMA5D35 (324-ball BGA package)
Clock speed	12 MHz crystal 32.768 KHz
Memory	2 x DDR2 2 Gb 16 Meg x 16 x 8 banks 1 x SLC NAND Flash 2/4Gb 8-bit data 1 x optional NOR 128 Mb 16-bit data
On-board I/O Ports	One Serial EEPROM SPI One 1-Wire EEPROM DS2431 One user power red LED and one user blue LED One Gigabit Ethernet PHY
Connector	SODIMM200
Board supply voltage	3.3V from SODIMM200 connector On-board power regulation
Temperature: - operating - storage	 0°C to +60°C -40°C to +85°C
Relative humidity	0 to 90% (non condensing)
RoHS status	Compliant
Board Identification Silkscreen top	SAMA5D31-CM, SAMA5D33-CM, SAMA5D34-CM, SAMA5D35-CM.

5.2.2 Interface Connection

- SODIMM200 card edge interface

5.2.3 Configuration Items

- Dual ON/OFF switch for NAND flash and SPI data flash Chip Select connection

5.2.4 Boot Options

The following table lists all the supported boot options.

Table 5-3. Boot Options

Boot Mode	Boot Device	Type	Note
BMS OPEN	Embedded ROM Boot	ROM Boot - SPI0, NPCS0 - SD/MMC MCI0, MCI1 - NAND Flash - SPI0, NPCS1 - TWI0	Default boot on embedded ROM
BMS CLOSE	NOR Flash	On-board NOR Flash using NCS0	Boot on external NOR Flash memory

5.2.4.1 Boot Configuration

In order to use SAM-BA® boot, the NAND flash and SPI data flash must be deselected.

The pushbutton PB4 (CS boot disable) in association with the PB RST allows to disable these components during the reset and access to the ROMBoot.

5.3 Functional Blocks

5.3.1 Processor

The CM board is equipped with an Atmel ARM-based embedded MPU, as listed below, in a BGA324-ball BGA package.

The four devices share an identical footprint. All four share the CM board PCB with minor configuration differences.

The four devices are:

- SAMA5D31
- SAMA5D33
- SAMA5D34
- SAMA5D35

.As different interfaces can be defined using the same pins, it depends on the actual configuration of the CPU as to which function(s) are in fact available to the Evaluation Kit board.

The Atmel SAMA5D3 series is a high-performance, power-efficient embedded MPU based on the ARM® Cortex™-A5 processor, achieving 536 MHz with power consumption levels below 0.5 mW in low-power mode. The device features a floating point unit for high-precision computing and accelerated data processing, and a high data bandwidth architecture. It integrates advanced user interface and connectivity peripherals and security features.

The SAMA5D3 series features an internal multi-layer bus architecture associated with 39 DMA channels to sustain the high bandwidth required by the processor and the high-speed peripherals. The device offers support for DDR2/LPDDR/LPDDR2 and MLC NAND Flash memory with 24-bit ECC.

The comprehensive peripheral set includes an LCD controller with overlays for hardware-accelerated image composition, a touchscreen interface and a CMOS sensor interface. Connectivity peripherals include Gigabit EMAC with IEEE1588, 10/100 EMAC, multiple CAN, UART, SPI and I2C. With its secure boot mechanism,

hardware accelerated engines for encryption (AES, TDES) and hash function (SHA), the SAMA5D3 ensures anti-cloning, code protection and secure external data transfers.

Please refer to Section 2.2 ”Evaluation Board Specifications” on page 2-3 for details.

The processor runs at frequencies up to 536 MHz for the core and up to 166 MHz for the system bus.

5.3.2 Clock Circuitry

The CM includes 3 clock sources:

- Two clocks are alternatives for the SAMA5D3 series processor main clock
- One crystal oscillator is used for the Ethernet RGMII chip

Table 5-4. Main Components Associated with the Clock Systems

Qty	Description	Component Assignment
1	Crystal for Internal Clock, 12 MHz	Y1
1	Crystal for RTC Clock, 32.768 kHz	Y2
1	Oscillator for Ethernet Clock RGMII, 25 MHz	Y3

5.3.3 Reset Circuitry

The reset sources for CM board are:

- Power on reset
- Pushbutton reset (Pushbutton is equipped on Main Board)
- JTAG reset from an in-circuit emulator (JTAG interface is equipped on MB)

5.3.4 Power Supplies

The CM board is driven by +3.3V input power rail from MB board through the SODIMM200 connector. The CM board embeds all necessary power rails required for the microprocessor.

When additional voltages are required, they are generated on board from the 3.3V supply (power source is a linear regulator or a switching regulator). The detailed power supply requirements for given modules are specified within the corresponding product documentation.

The following table summarizes the power specifications.

Table 5-5. Supply Group Configuration

Nominal	Name	Powers	Component
3.0V	VDDBU	the Slow Clock oscillator, the internal 32K RC, the internal 12M RC and a part of the System Controller	From VBAT 3V, SODIMM200 connector
3.3V	VDDIOP0	a part of Peripherals I/O lines	From Main 3.3V, SODIMM200 connector
3.3V	VDDIOP1	a part of Peripherals I/O lines	From Main 3.3V, SODIMM200 connector
3.3V	VDDUTMII	the USB device and host UTMI + interface	From Main 3.3V, SODIMM200 connector
3.3V	VDDOSC	the Main Oscillator cells	From Main 3.3V, SODIMM200 connector

Table 5-5. Supply Group Configuration

Nominal	Name	Powers	Component
3.3V	VDDANA	the Analog to Digital Converter	From Main 3.3V, SODIMM200 connector
1.2V	VDDCORE	the core, including the processor, the embedded memories and the peripherals	Regulator on-board
1.2V	VDDUTMIC	The USB device and Host UTMI + core	Regulator on-board
1.2V	VDDPLLA	The PLLA cell	Regulator on-board
1.8V	VDDIODDR	DDR2 interfaces I/O Lines	Regulator on-board
1.8V	VDDIOM	NAND, NOR Flash and SMC interface I/O lines	Regulator on-board
3.0V to 3.3V	ADVREF	ADC Reference voltage	From ADVREF, SODIMM200 connector
2.5V	VDDFUSE	Fuse box for programming	Regulator on-board

Figure 5-4. EMBEST Power Supply

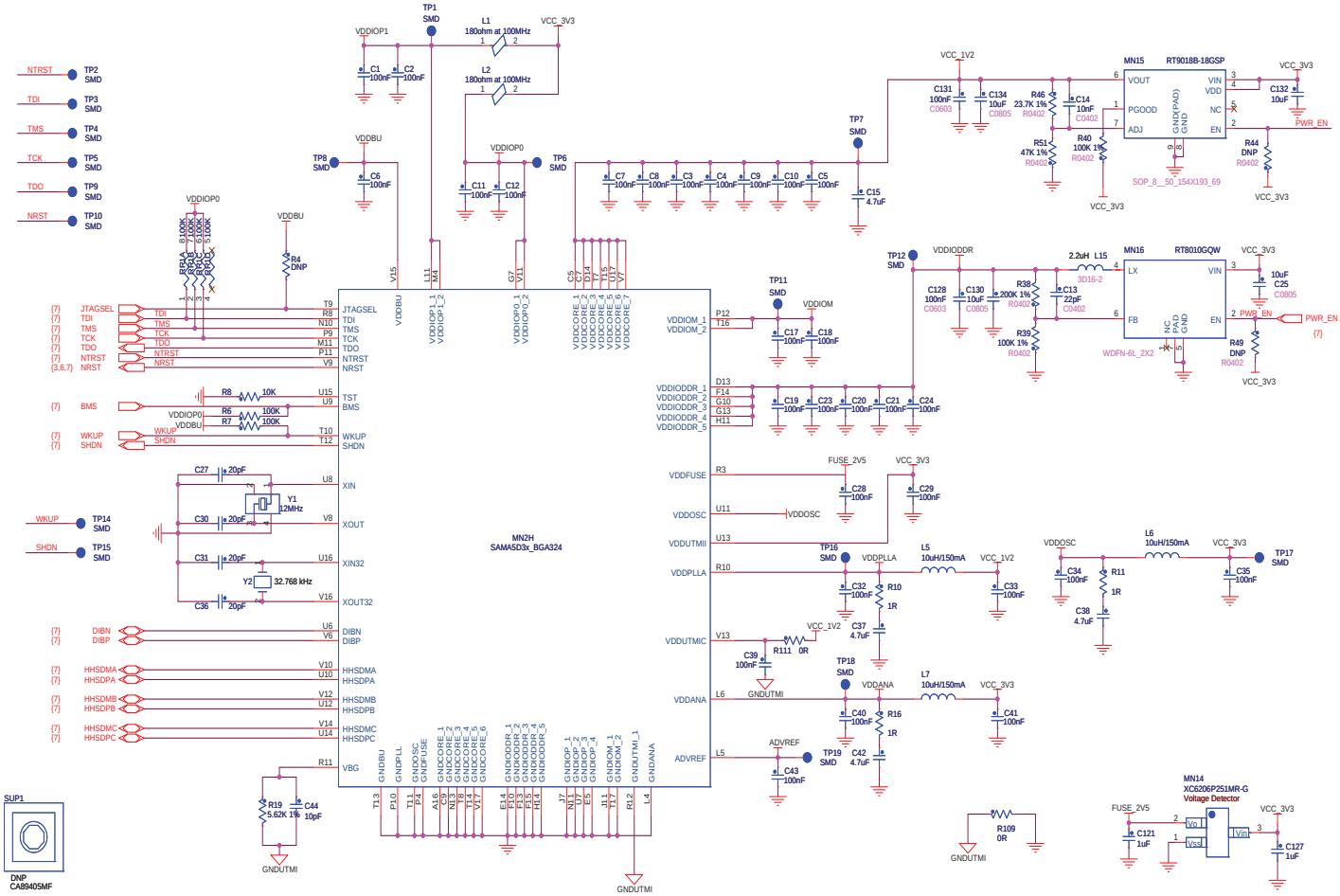


Figure 5-5. RONETIX Power Supply

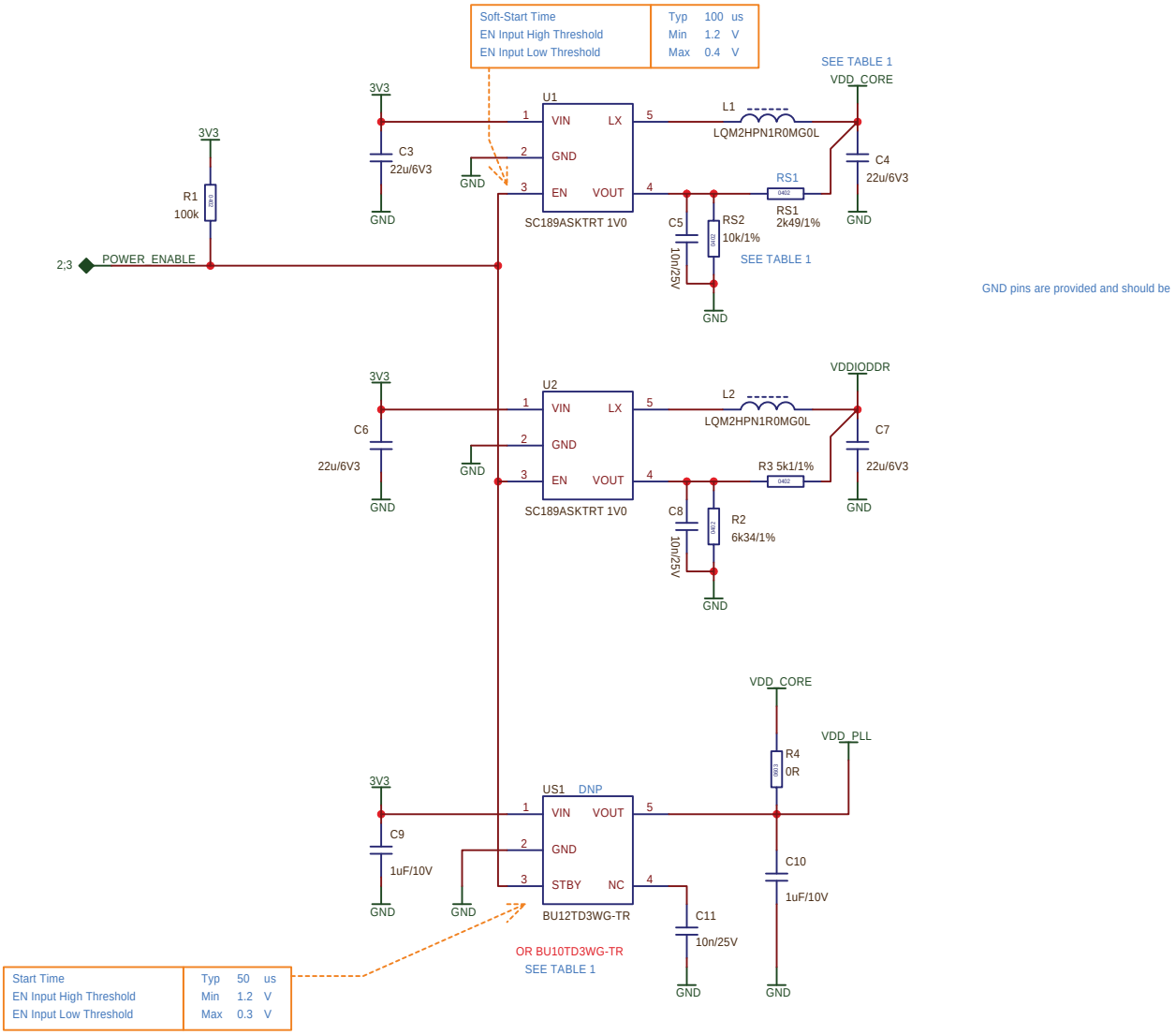
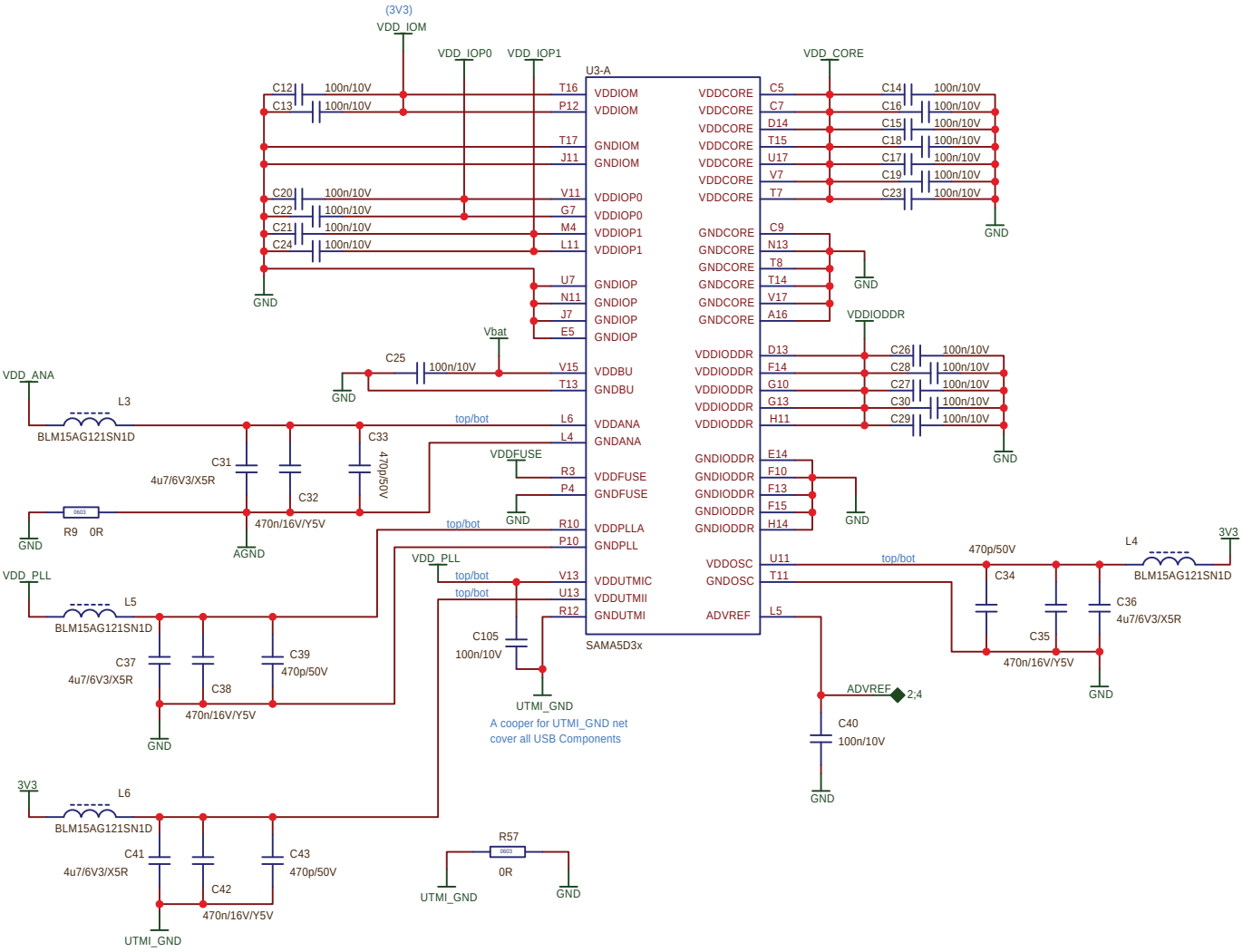


Figure 5-6. RONETIX Power Supply (Continued)



5.3.5 Memory

5.3.5.1 Memory Organization

The SAMA5D3 series processor features a DDR/SDR memory interface and an External Bus Interface (EBI) to permit interfacing to a wide range of external memories and to almost any kind of parallel peripheral.

5.3.5.2 Resources allocation.

This section describes the memory devices that equip the SAMA5D3 series-CM board.

- Two SDRAM/DDR2 used as main system memory. MT47H128M16 - 2 Gb - 16 Meg x 16 x 8 banks, the board provides up to 2 Gb on-board, soldered DDR2 SDRAM. The memory bus is 32 bits wide and operates with up to 166 MHz.

Figure 5-7. EMBEST DDR2 Memory

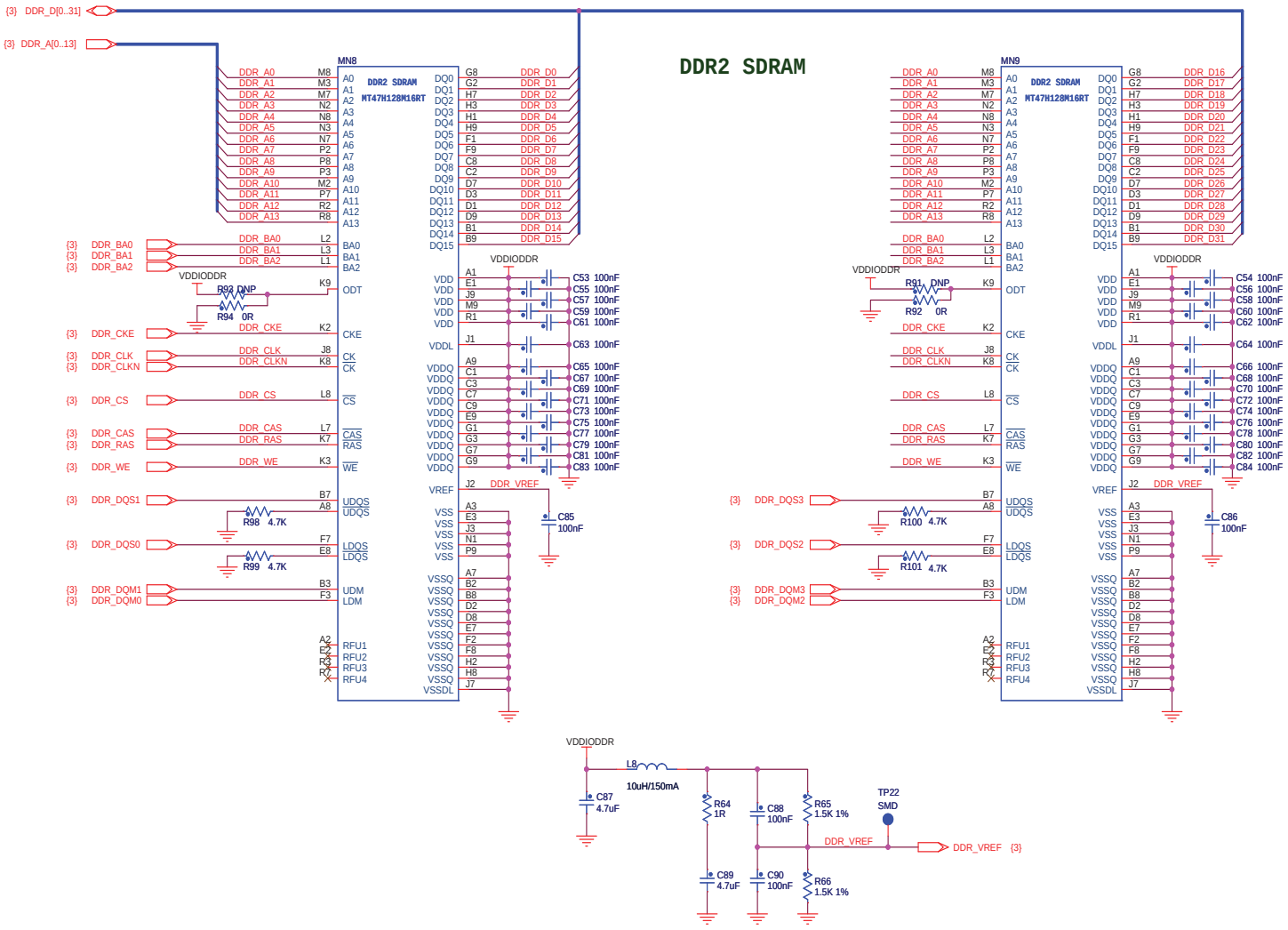
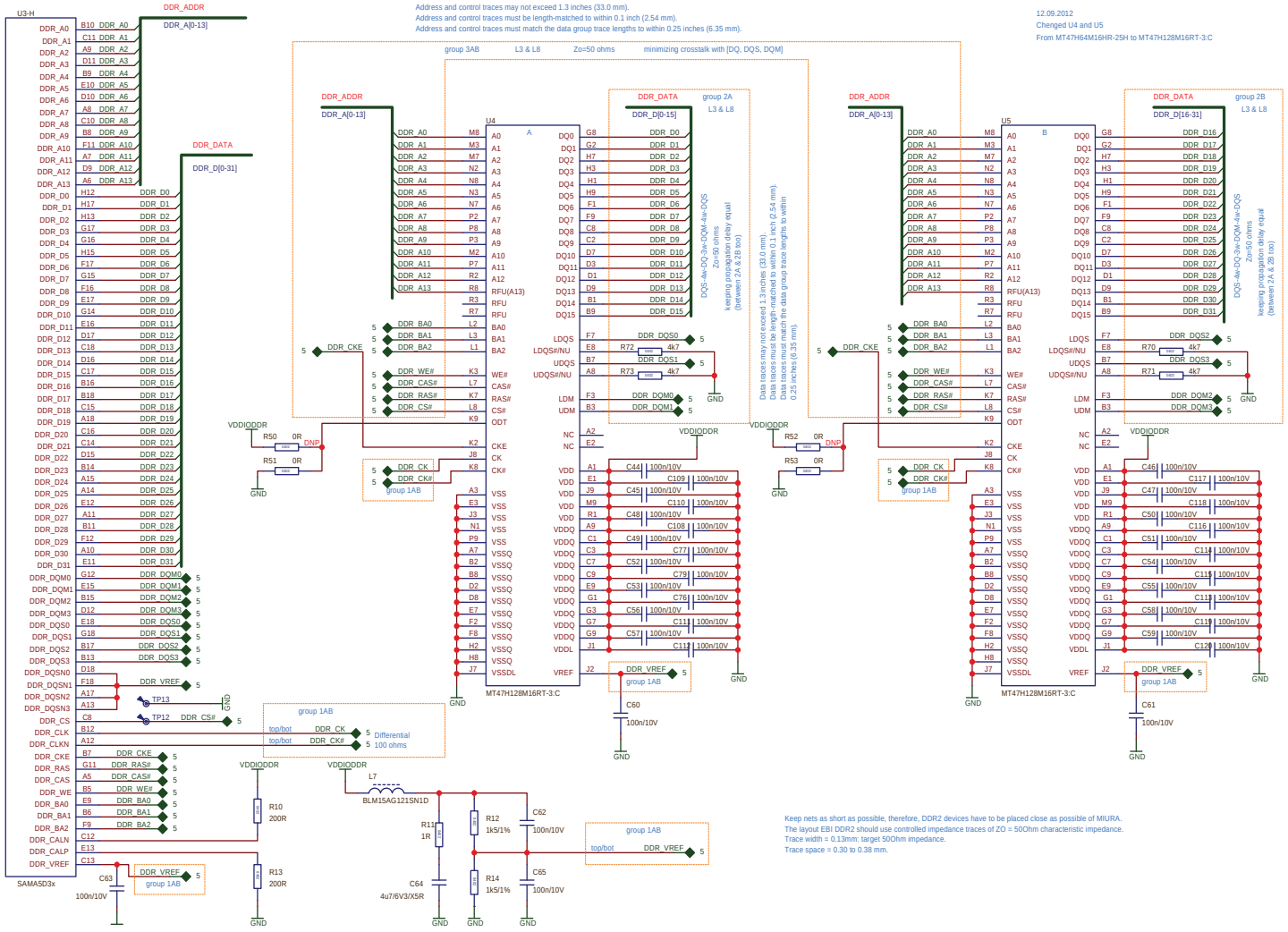


Figure 5-8. RONETIX DDR2 Memory



- One NAND Flash: NAND is connected to the processor. Maximum size is 256 Mbytes.
- One NOR Flash (optional, not populated): NOR Flash is 16 bits wide. Maximum size is 128 Mbytes.

Figure 5-9. EMBEST External Memory

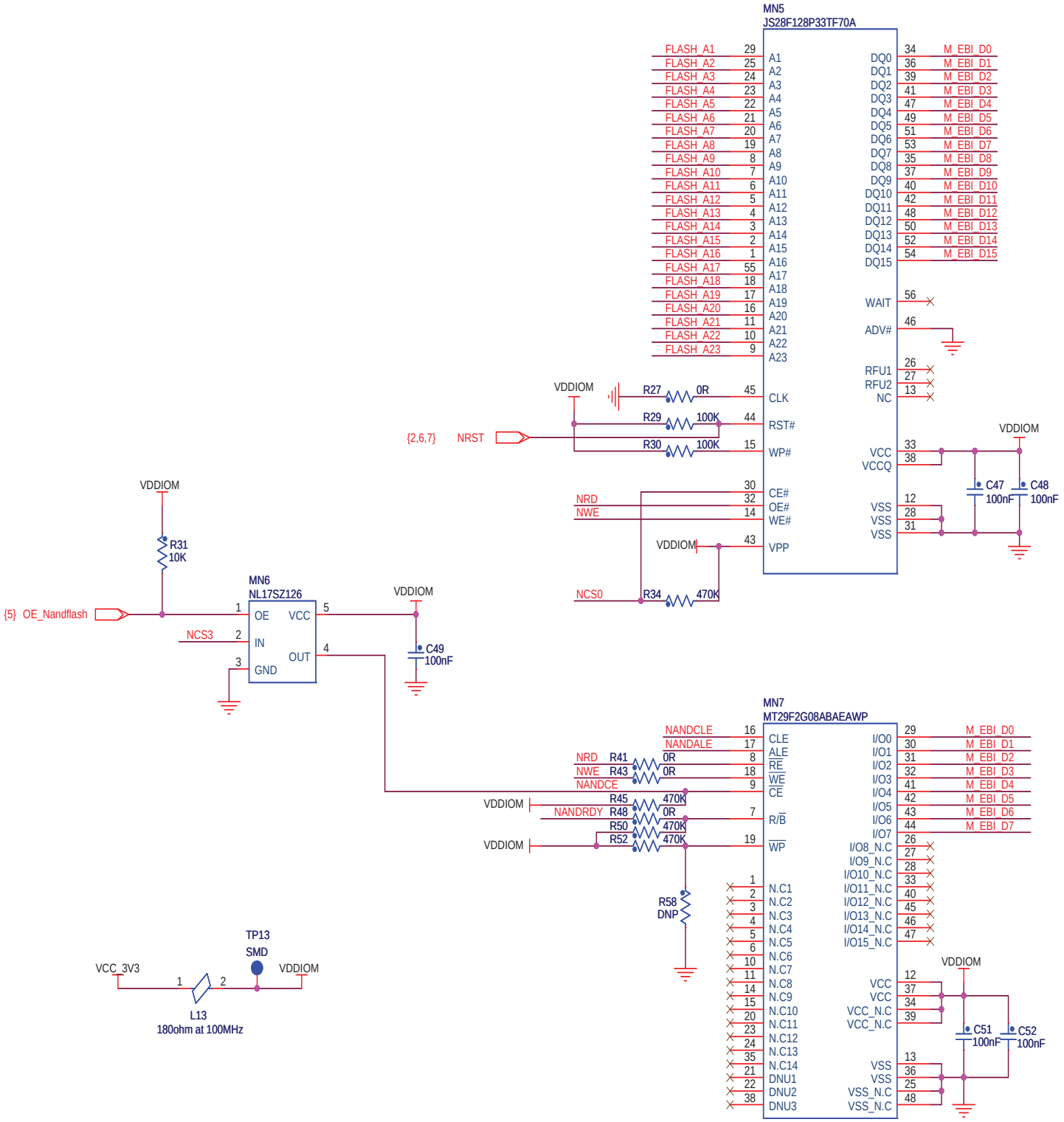
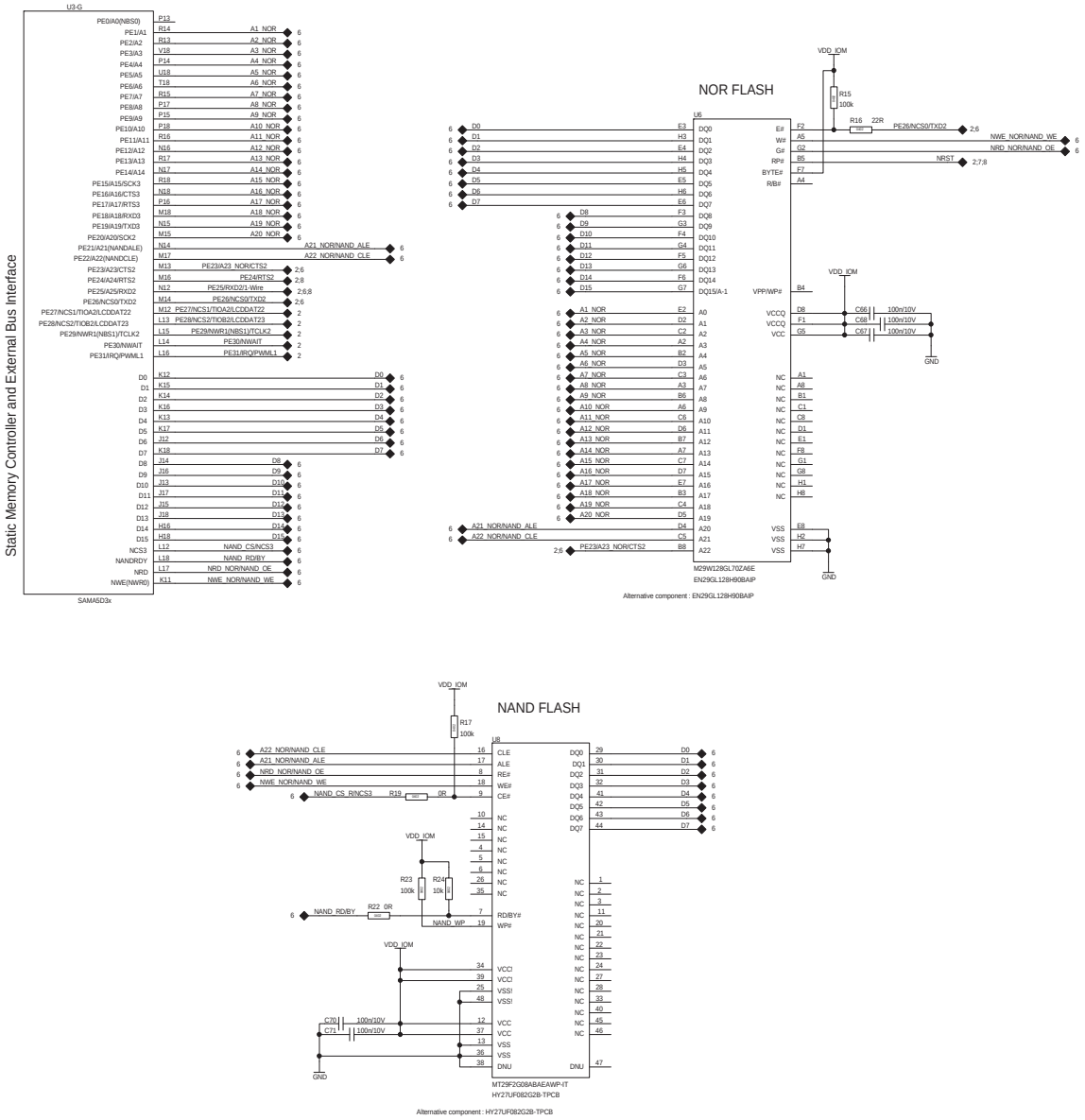


Figure 5-10. RONETIX External Memory



5.3.6 Serial Peripheral Interface Controller (SPI)

The SAMA5D3 series processor provides two high-speed Serial Peripheral Interface (SPI) controllers. One port is used to interface with the on-board serial DataFlash®.

There are four main signals used in the SPI interface: Clock, Data In, Data Out, and Chip Select. The Serial Peripheral Interface (SPI) is a serial interface similar to the IIC bus interface but with three primary differences:

- it operates at a higher speed,
- separate transmit and receive data lines,
- device access is chip-select based instead of address based.

Figure 5-11. EMBEST Serial DataFlash on SPI

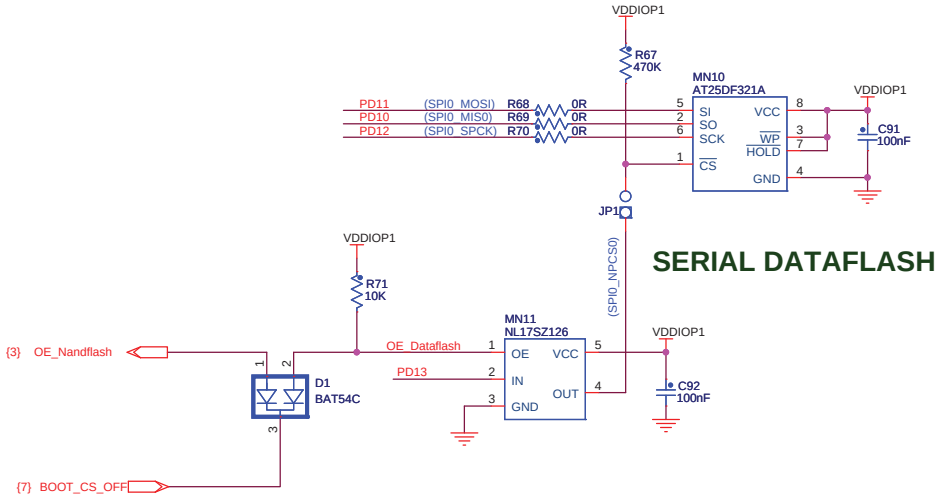
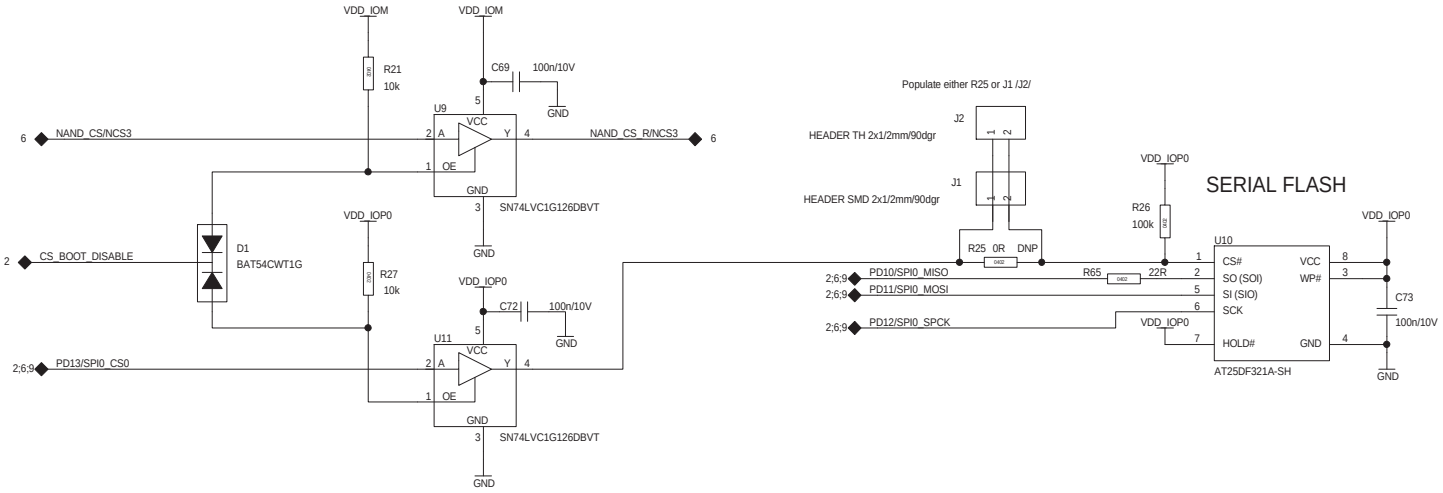


Figure 5-12. RONETIX Serial DataFlash on SPI



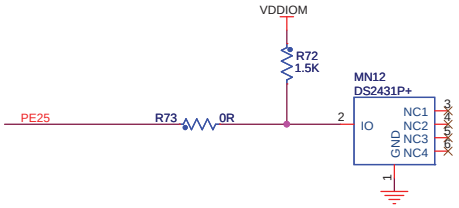
5.3.7 1-Wire EEPROM

The SAMA5D3 series-CM board uses 1-Wire device as "soft label" to store the information such as chip type, manufacture name, production date, etc.

Only page 1 is used. Be careful not to modify the information contained in this page.

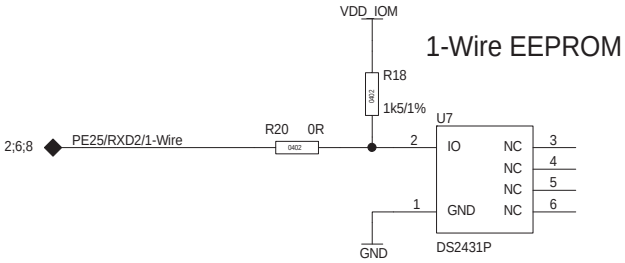
Pages 2 to n remain free for the user.

Figure 5-13. EMBEST 1-Wire EEPROM



1-WIRE EEPROM

Figure 5-14. RONETIX 1-Wire EEPROM



5.3.8 Tri-Speed Ethernet PHY

The SAMA5D3 series-CM board is equipped with a MICREL PHY devices (MICREL KSZ9021/31) operating at 10/100/1000 Mbps. The board supports RGMII interface mode. The Ethernet interface consists of 4 pairs of low voltage differential pair signals designated from GRX± and GTx± plus control signals for link activity indicators. These signals can be used to connect to a 10/100/1000 BaseT RJ45 connector integrated on the main board.

For more information about the Ethernet controller device, refer to the MICREL KSZ89021RN controller manufacturer's datasheet.

Figure 5-15. EMBEST GEthernet ETH0

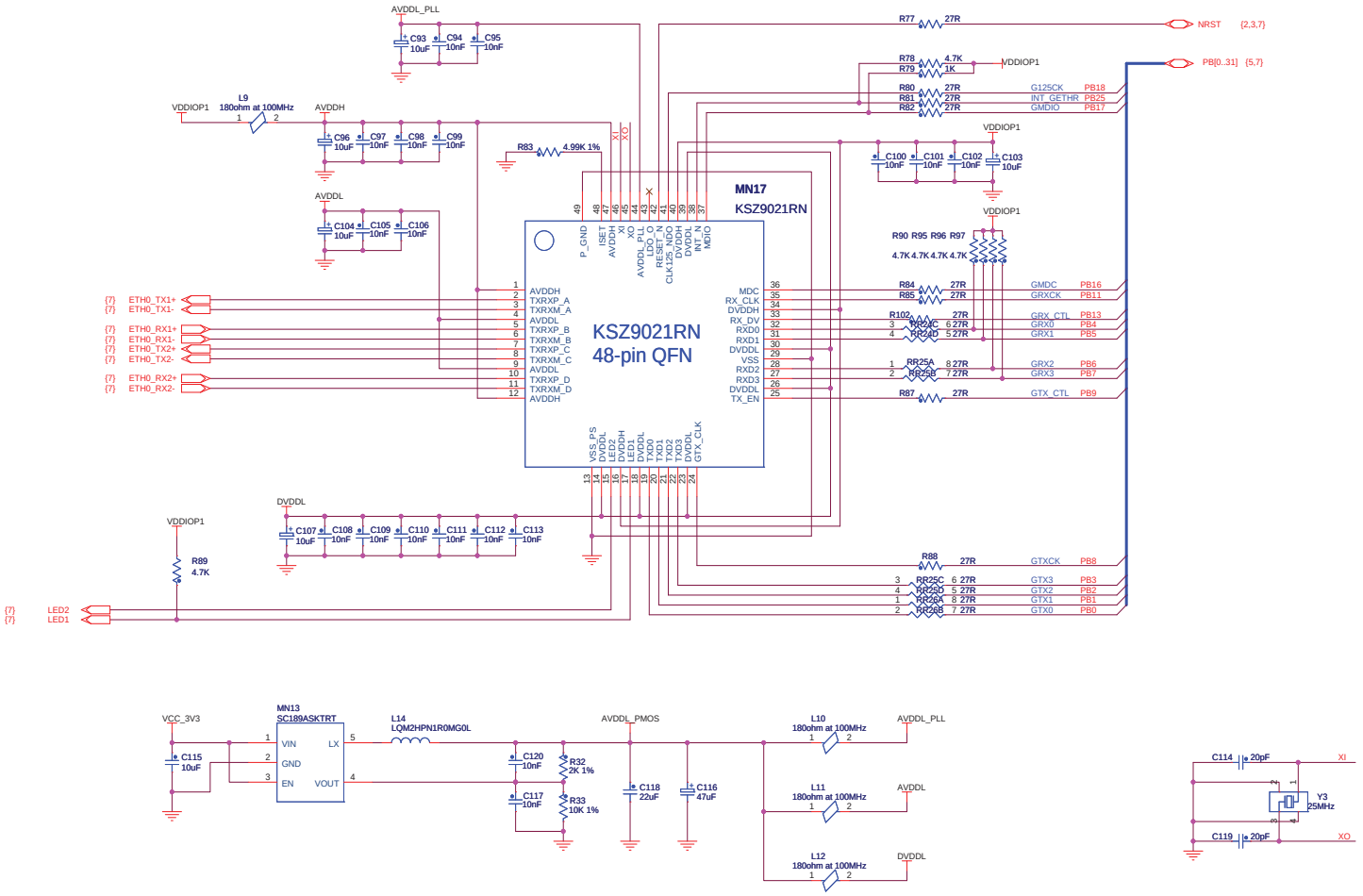
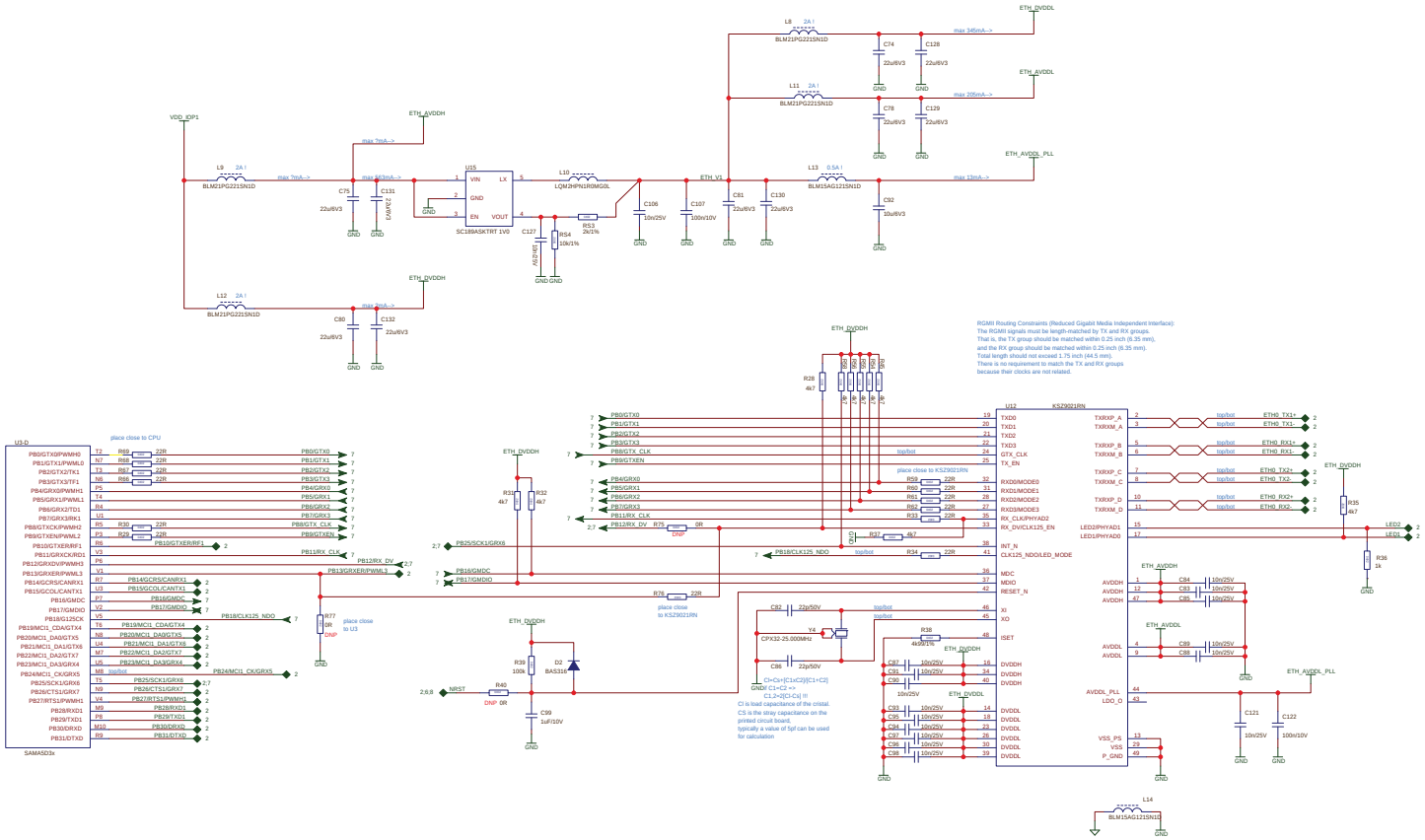


Figure 5-16. RONETIX GEthernet ETH0



5.3.9 Indicators

There are two LEDs on the SAMA5D3 series-CM board that can be controlled by the user.

The red LED provides an indication that power is supplied to the board and is controlled via software.

The blue LED is controlled via GPIO pins.

Figure 5-17. EMBEST LED Indicators

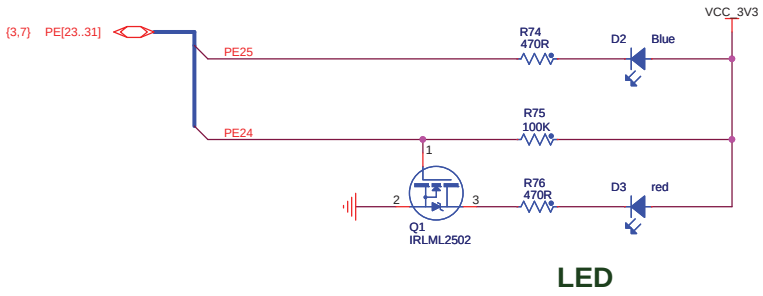
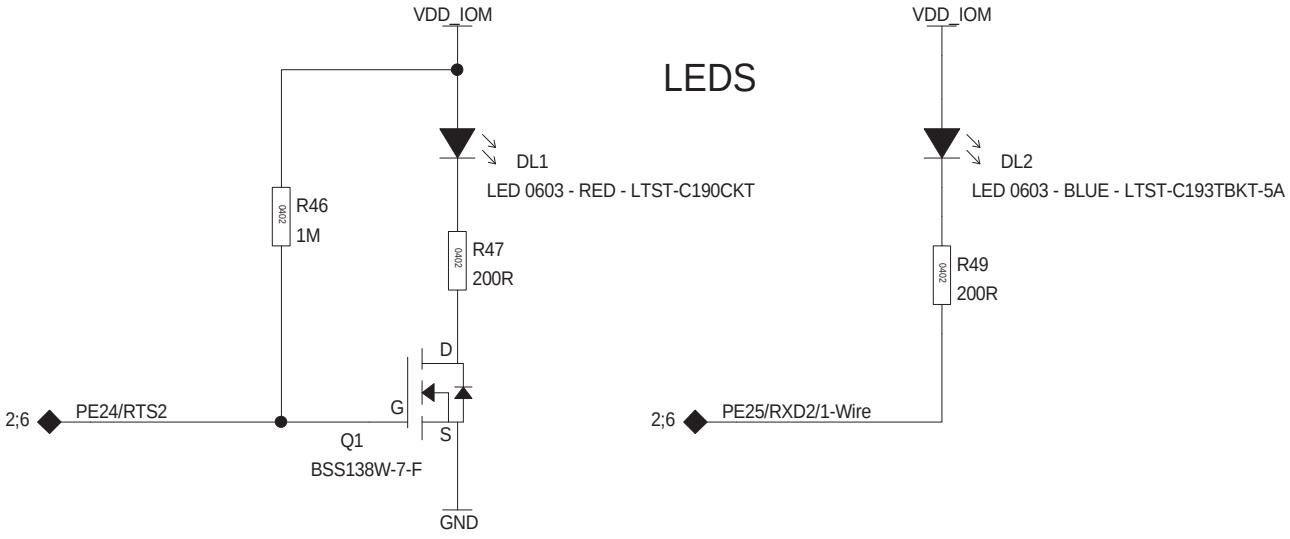


Figure 5-18. RONETIX LED Indicators



5.3.10 SODIMM200 Interface

The SAMA5D3 series-CM board uses SODIMM200 card edge connector to interface with the MB board.

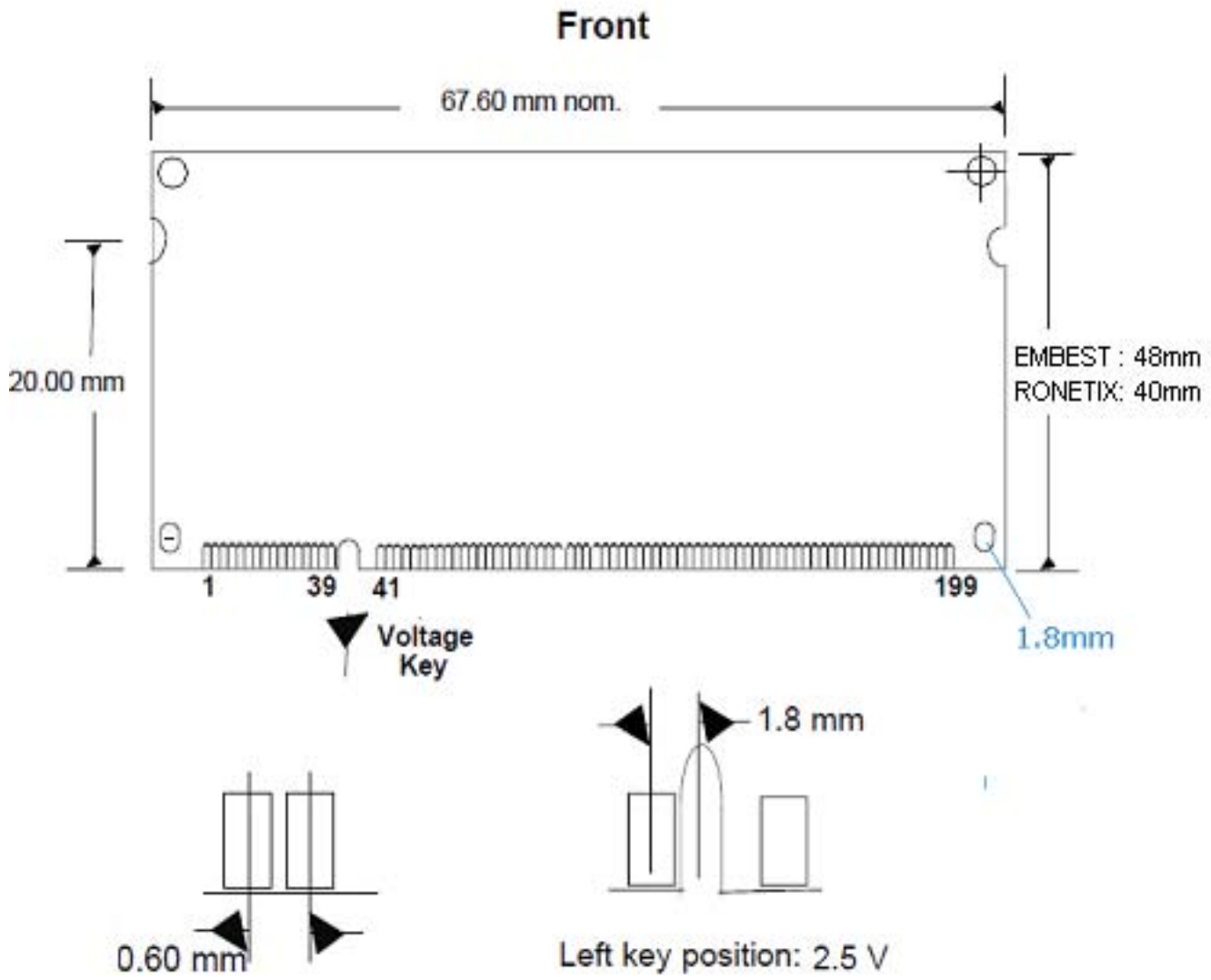
Please refer to Figure 6-44 on page 6-44

5.3.11 Connectors

The diagram below shows the mechanical dimensions of the SAMA5D3 series-CM Module outline and the mounting holes.

Figure 5-19 reference Simplified Mechanical Drawing with Keying Position 2.5V.

Figure 5-19. CM Board Dimensions

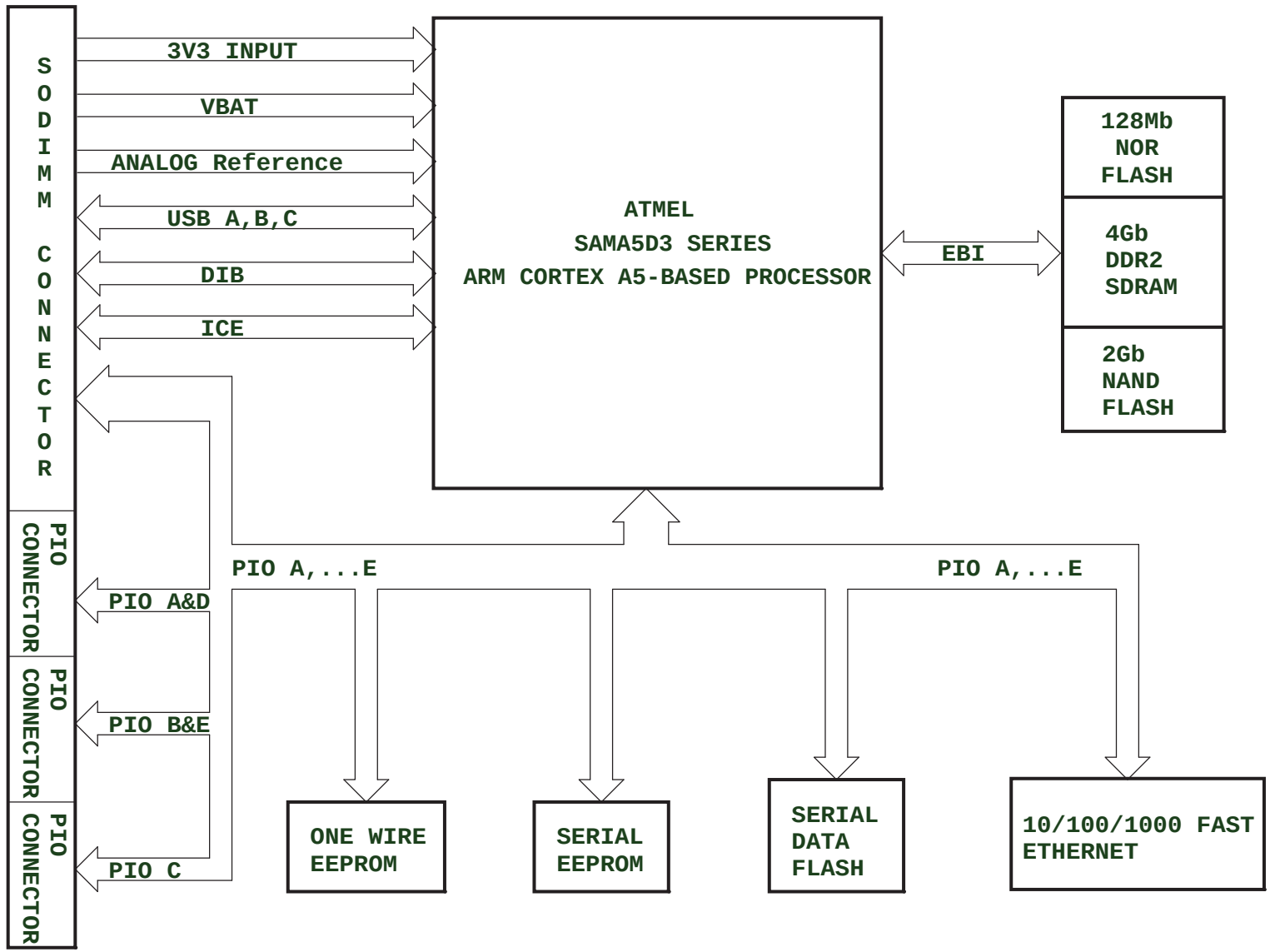


Holes for mounting screws on carrier board.

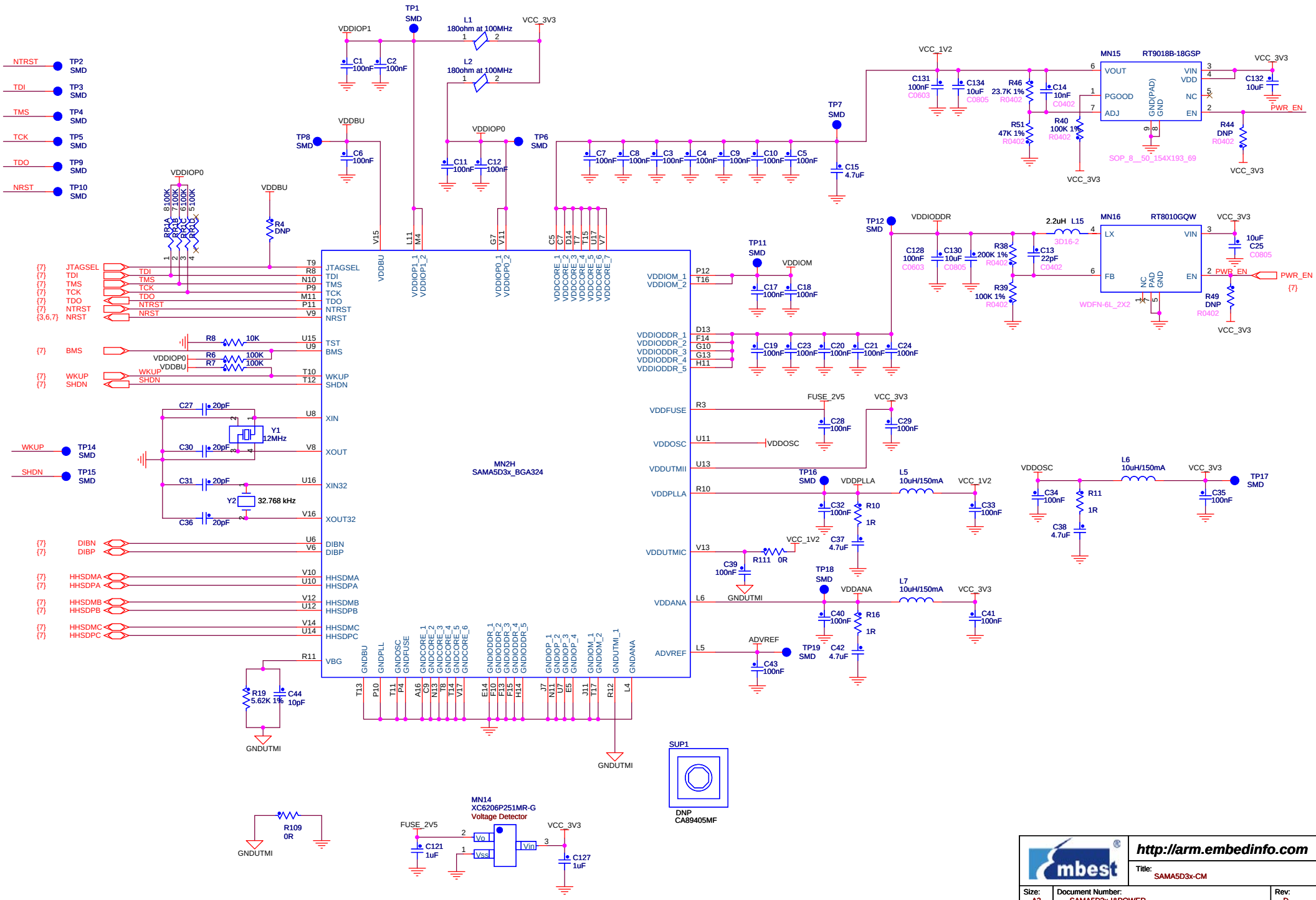
5.4 EMBEST Schematics

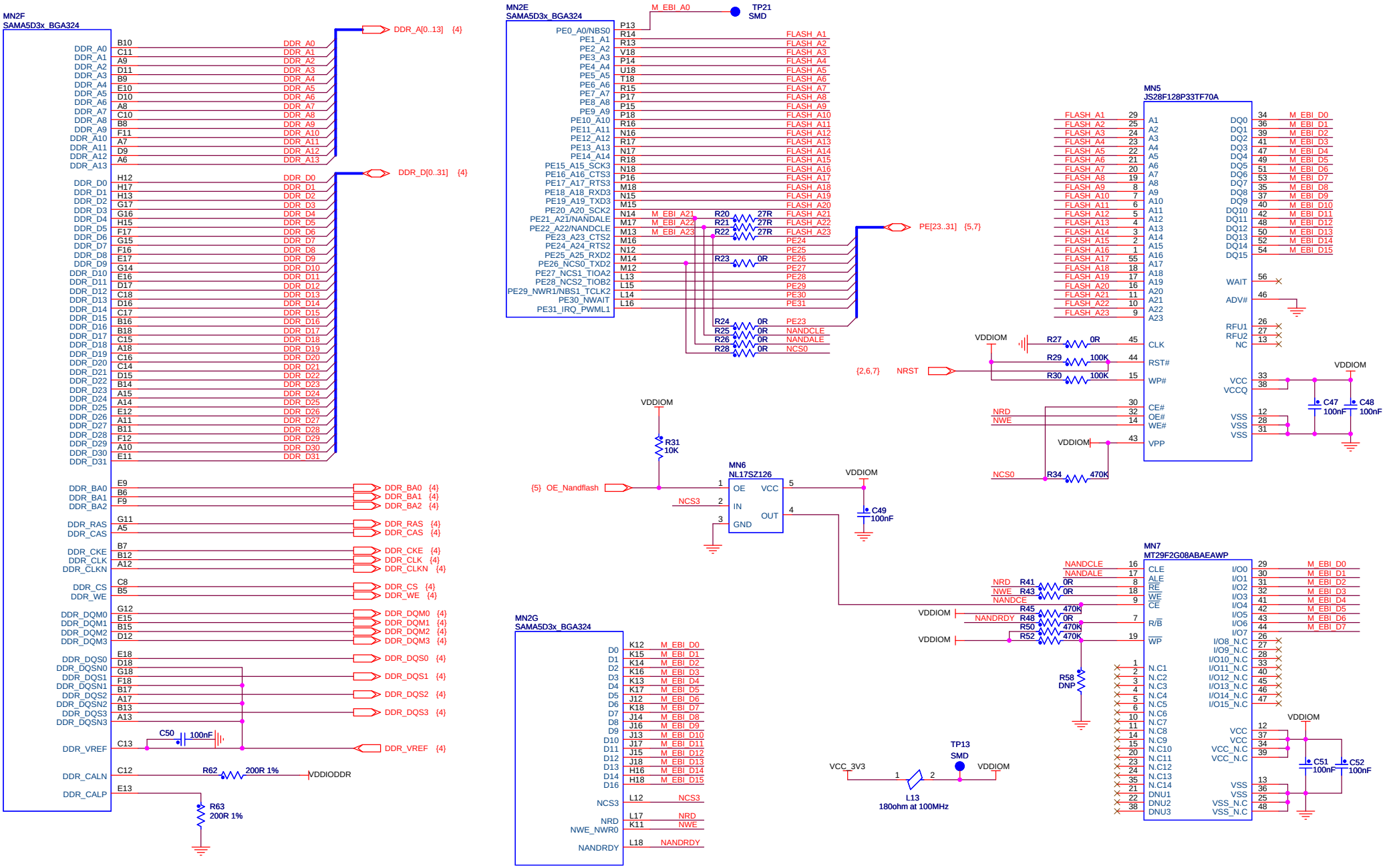
This section contains the following schematics:

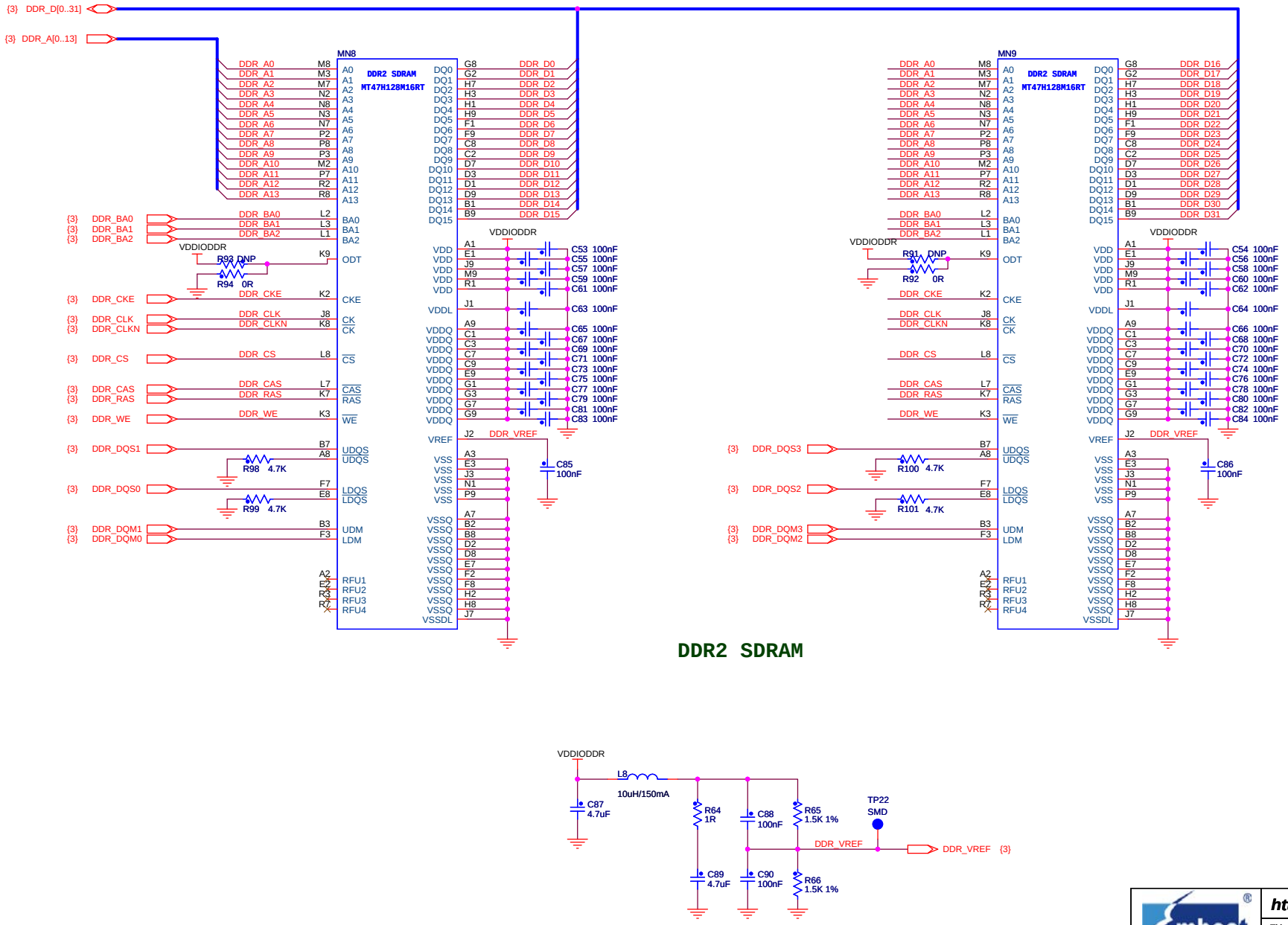
- Block Diagram
- SAMA5D3x Power
- SAMA5D3x NOR and NAND
- 4 Gb DDR2
- SAMA5D3x Dataflash, 1-wire, LED
- Ethernet
- 200-pin SODIMM



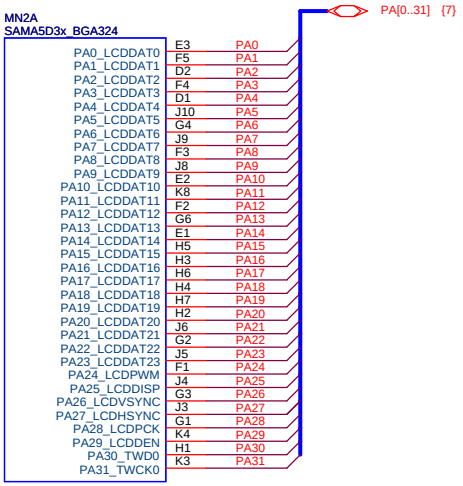
http://arm.embedinfo.com		
Title: SAMA5D3x-CM		
Size: A3	Document Number: BLOCK DIAGRAM	Rev: D
Draw By: Zhu Xueliang	Date: Monday, September 17, 2012	Sheet: 1 of 7

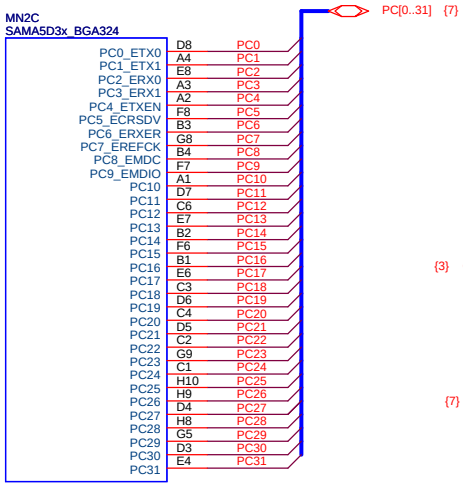

MN2H
SAMA5D3x_BGA324
MN14
XC6206P251MR-G
Voltage Detector
MN15
RT9018B-18GSP
MN16
RT8010GQW
SUP1
DNP
CA89405MF
http://arm.embedinfo.com
Title:
SAMA5D3x-CM
Size: A3
Document Number:
SAMA5D3x-I&POWER
Rev: D
Draw By: Zhu Xueliang
Date: Friday, September 21, 2012
Sheet: 2 of 7

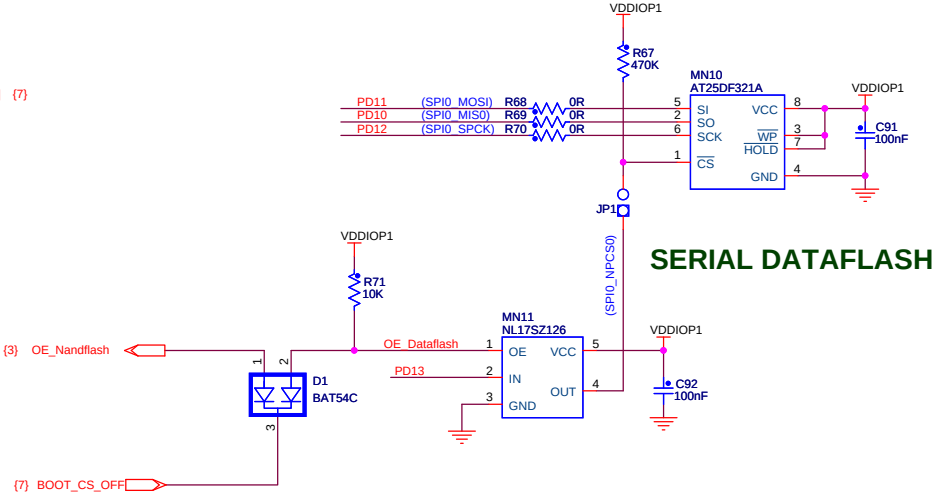

MN2F
SAMA5D3x_BGA324
DDR_A[0..13] {4}
DDR_D[0..31] {4}
MN2E
SAMA5D3x_BGA324
M_EBI_A0
TP21
SMD
PE[23..31] {5,7}
MN5
JS28F128P33TF70A
{2,6,7} NRST
VDDIOM
MN6
NL17SZ126
{5} OE_Nandflash
NCS3
MN7
MT29F2G08ABAEAWP
MN2G
SAMA5D3x_BGA324
TP13
SMD
VCC_3V3
L13
180ohm at 100MHz
C50 100nF
R62 200R 1%
VDDIODDR
R63 200R 1%
R31 10K
C49 100nF
C47 100nF
C48 100nF
C51 100nF
C52 100nF
R58 DNP
http://arm.embedinfo.com
Title: SAMA5D3x-CM
Size: A3
Document Number: SAMA5D3x-II&NOR&NAND
Rev: D
Draw By: Zhu Xueliang
Date: Wednesday, September 19, 2012
Sheet: 3 of 7

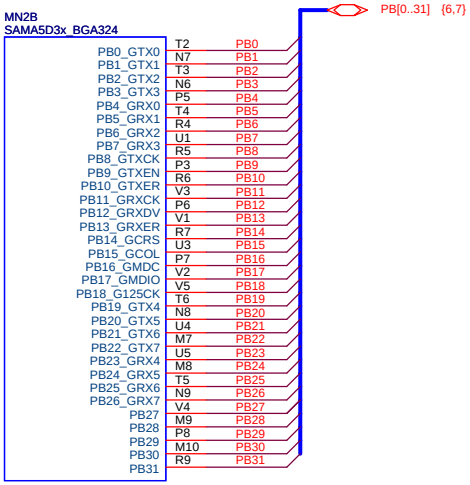


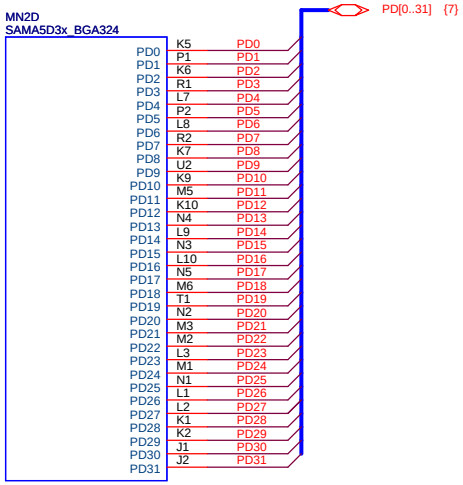
http://arm.embedinfo.com		
Title: SAMA5D3x-CM		
Size: A3	Document Number: 4Gb DDR2	Rev: D
Draw By: Zhu Xueliang	Date: Wednesday, September 19, 2012	Sheet: 4 of 7

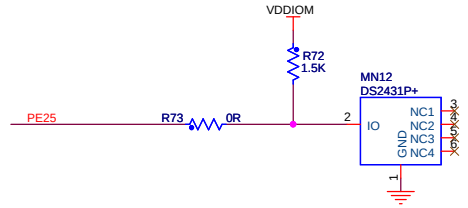


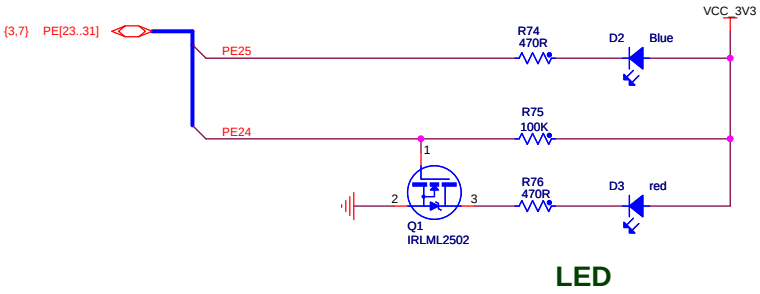




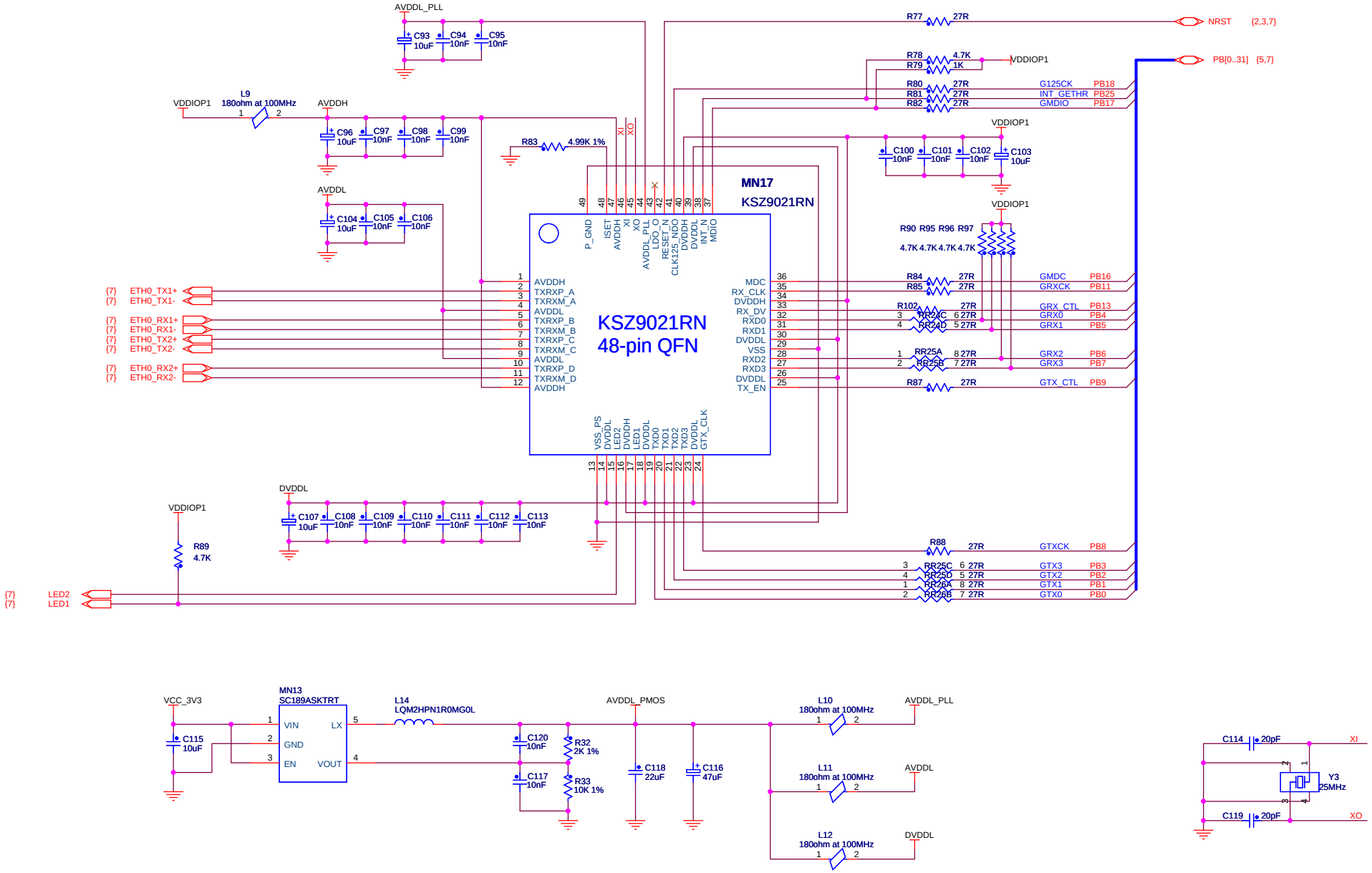




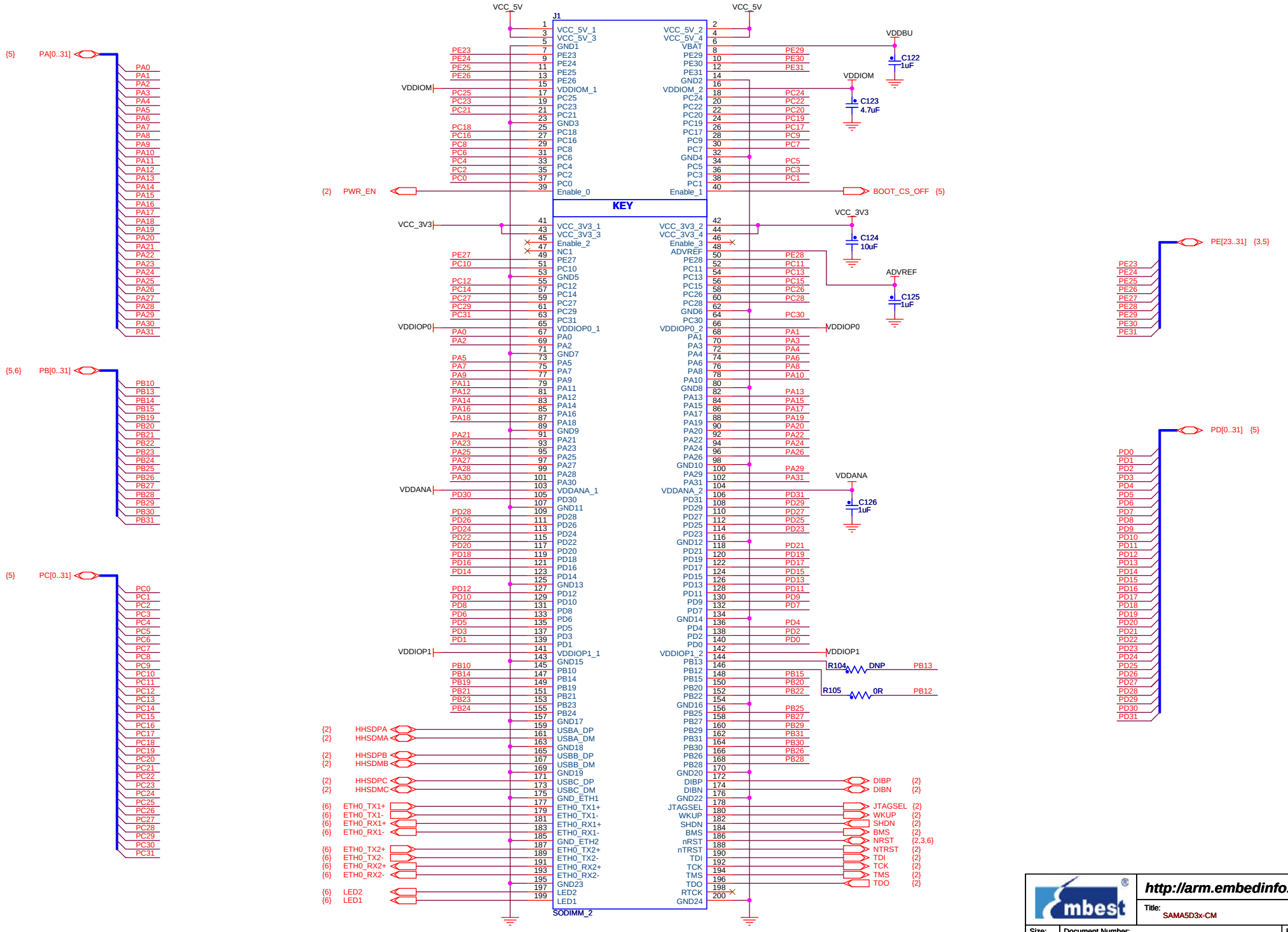




http://arm.embedinfo.com		
Title: SAMA5D3x-CM		
Size: A3	Document Number: SAMA5D3x-II&DATAFLASH&1-WIRE,LED	Rev: D
Draw By: Zhu Xueliang	Date: Wednesday, September 19, 2012	Sheet: 5 of 7



embest	http://arm.embedinfo.com	
Title: SAMA5D3x-CM		
Size: A3	Document Number: ETHERNET	Rev: D
Draw By: Zhu Xueliang	Date: Friday, September 21, 2012	Sheet: 6 of 7



	http://arm.embedinfo.com		
Title: SAMA5D3x-CM			
Size: A3	Document Number: 200-PIN SODIMM		Rev: D
Draw By: Zhu Xueliang	Date: Monday, September 17, 2012		Sheet: 7 of 7

5.5 RONETIX Schematics

This section contains the following schematics:

- Main Sheet
- SODIMM 200
- Power Supply
- CPU Power Supply
- DDR2 interface
- FI: NAND, NOR, Serial, I2C, 1-wire
- Ethernet
- USB, JTAG, LEDs
- Bus Interface

SCHEMATICS: SAMA5D3x-CM

SHEET #	SHEET NAME
1	MAIN
2	SODIM200
3	POWER SUPPLY
4	CPU-POWER SUPPLY
5	DDR2 INTERFACE
6	FI: NAND/NOR/SERIAL/I2C/1-WIRE
7	ETHERNET
8	USB/JTAG/LEDS
9	BUS INTERFACE

DATE:	DESCRIPTION	REVISION	STATUS
15.03.2012	SAMA5D3x-CM v2.0	2.0	OPEN
20.09.2012	SAMA5D3x-CM v2.0	2.0	CLOSE

Changes Rev2.0

1. SoDIMM200 change:
   * PB13 pin 144 with 0R DNP
   * PB12 pin 146 with 0R populated

2. VDD_CORE from 1.20V to 1.25V
3. US1 - From TPS71712DCKR to BU12TD3WG-TR and attribute DNP
4. Replaced Q2 with U15 SC189ASKTRT 1V0
5. Q1 from BSS138W(SOT323) to BSS138(SOT23)
6. C74 - from 47uF Tant to 22uF 0805
   Added - C128 22uF 0805
   C78 - from 47uF Tant to 22uF 0805
   Added - C129 22uF 0805
   C81 - from 47uF Tant to 22uF 0805
   Added - C130 22uF 0805
   C75 - from 47uF Tant to 22uF 0805
   Added - C131 22uF 0805
   C80 - from 47uF Tant to 22uF 0805
   Added - C132 22uF 0805
   C92 - from 10u Tant to 10u 0805

7. R4 - Changed attribute Note from DNP to "empty"
8. Y1 changed to CM200C-32.768KDZF-UT
9. U6 changed to EN29GL128H-70BAIP
10. U8 changed to HY27UF082G2B-TPCB

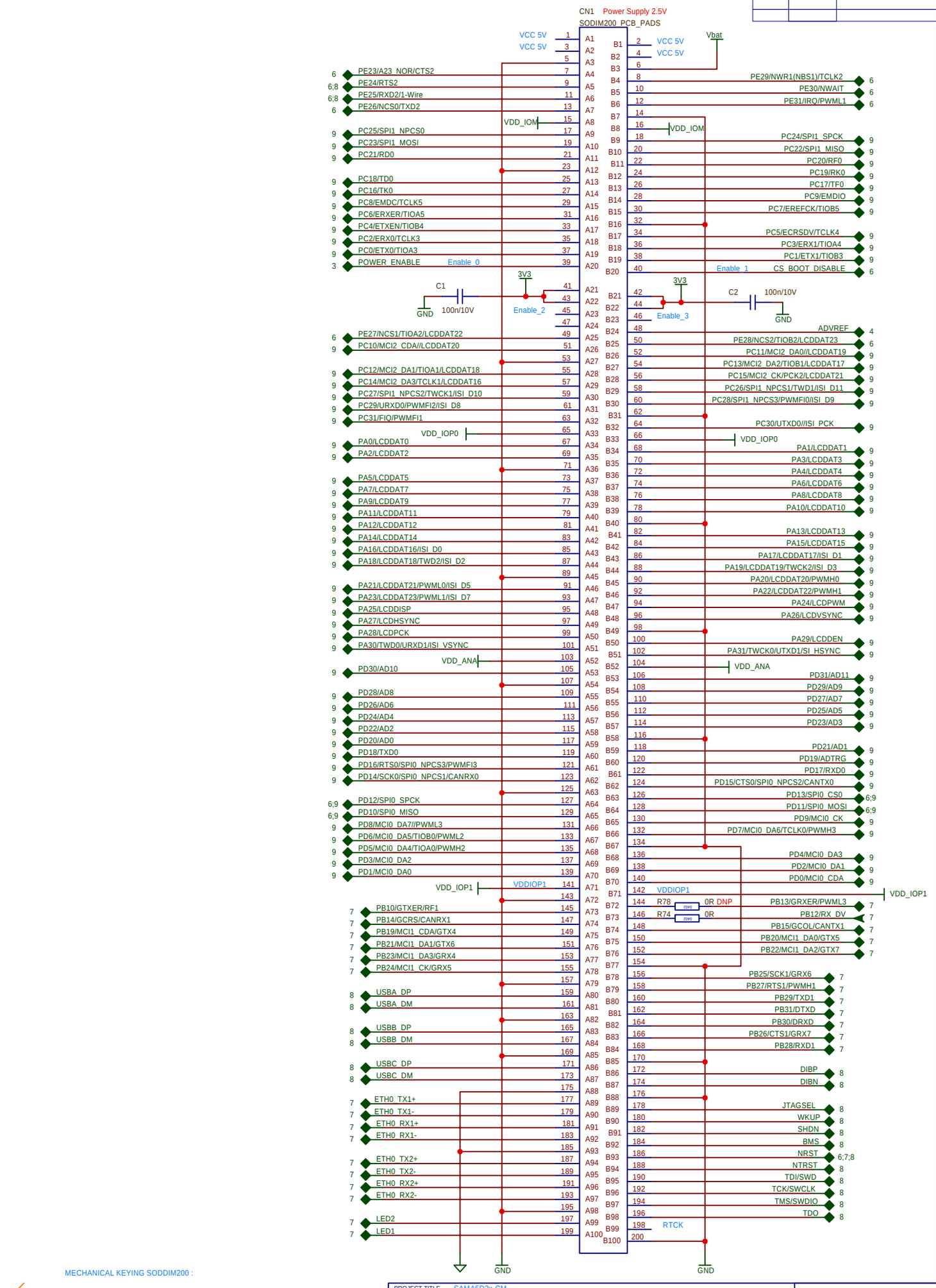
Mechanical

- Z6 Drill No plated 0.85mm
- Z7 Drill No plated 0.85mm
- Z5 Drill No plated 1.65mm
- Z8 Drill No plated 1.65mm
- Z9 Drill No plated 1.65mm
- Z10 Drill No plated 1.65mm
- Z1 Drill No plated 1.8 mm
- Z2 Drill No plated 1.8 mm
- Z11 Passer 0.7 mm
- Z12 Passer 0.7 mm
- Z13 Passer 0.7 mm
- Z14 Passer 0.7 mm
- Z3 Drill No plated 3.2 mm
- Z4 Drill No plated 3.2 mm

Note: To each Signal Reference have one or more digits.
These are the numbers of sheets
to which is connected this signal.

PROJECT TITLE	SAMA5D3x-CM				
SHEET TITLE	MAIN				
FILE	SAMA5D3x-CM v2.0f.scm			SHEET NO 1 OF 9	
SIZE	REV	DATE	DESCRIPTION FILE	DROWN	
A4		20.9.2012		ISSUED	

RONETIX development tool www.ronetix.at



MECHANICAL KEYING SODDIM200 :

Power Supply 2.5V -> distance between pin 39 and center notch = 1.80mm

Power Supply 1.8V -> distance between pin 39 and center notch = 2.70mm

PROJECT TITLE	SAMA5D3x-CM				
SHEET TITLE	SODIM200				
FILE	SAMA5D3x-CM v2.0f.scm			SHEET NO 2 OF 9	
SIZE	REV	DATE	DESCRIPTION FILE	DROWN	
A4		20.9.2012		ISSUED	

RONETIX development tool www.ronetix.at

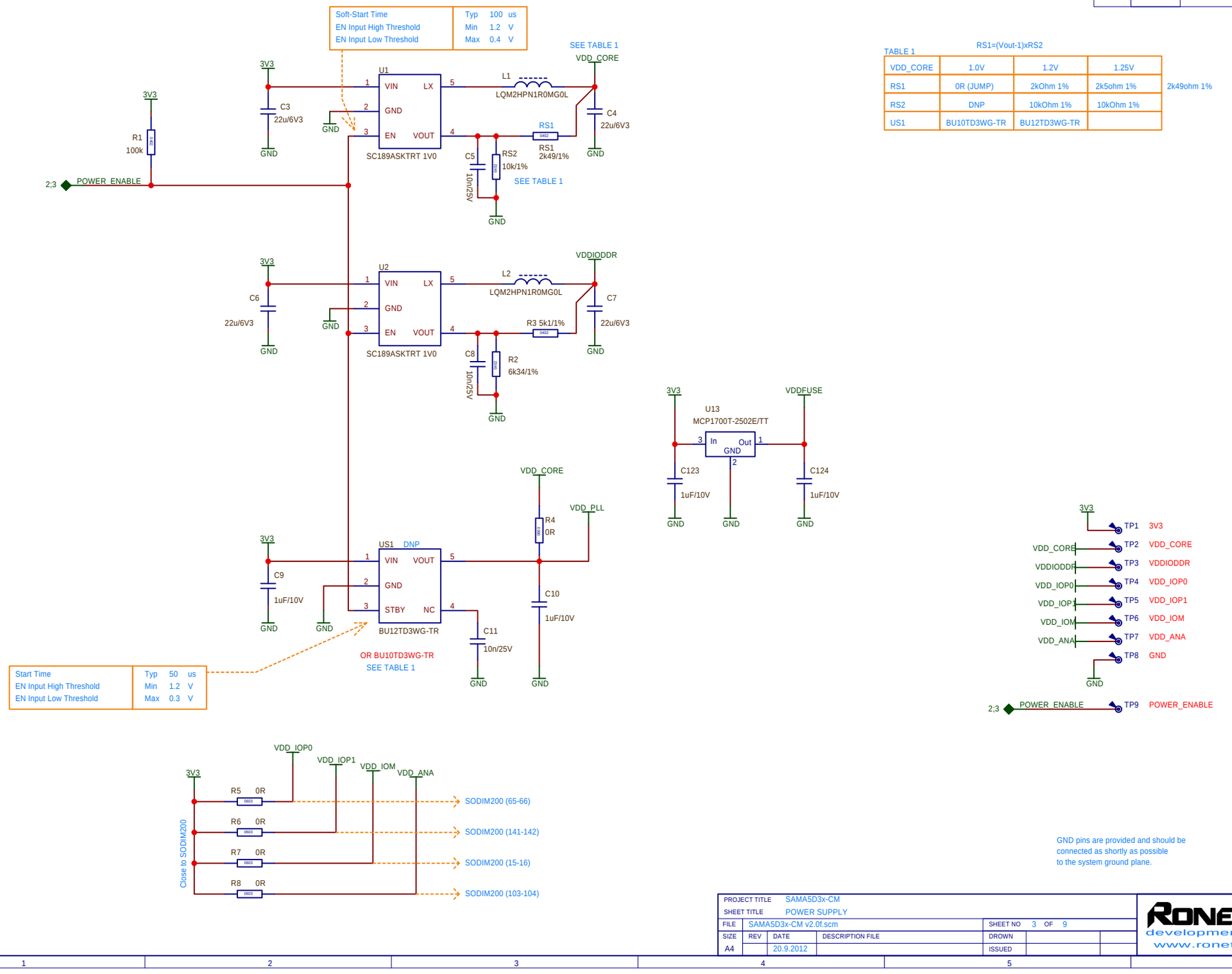
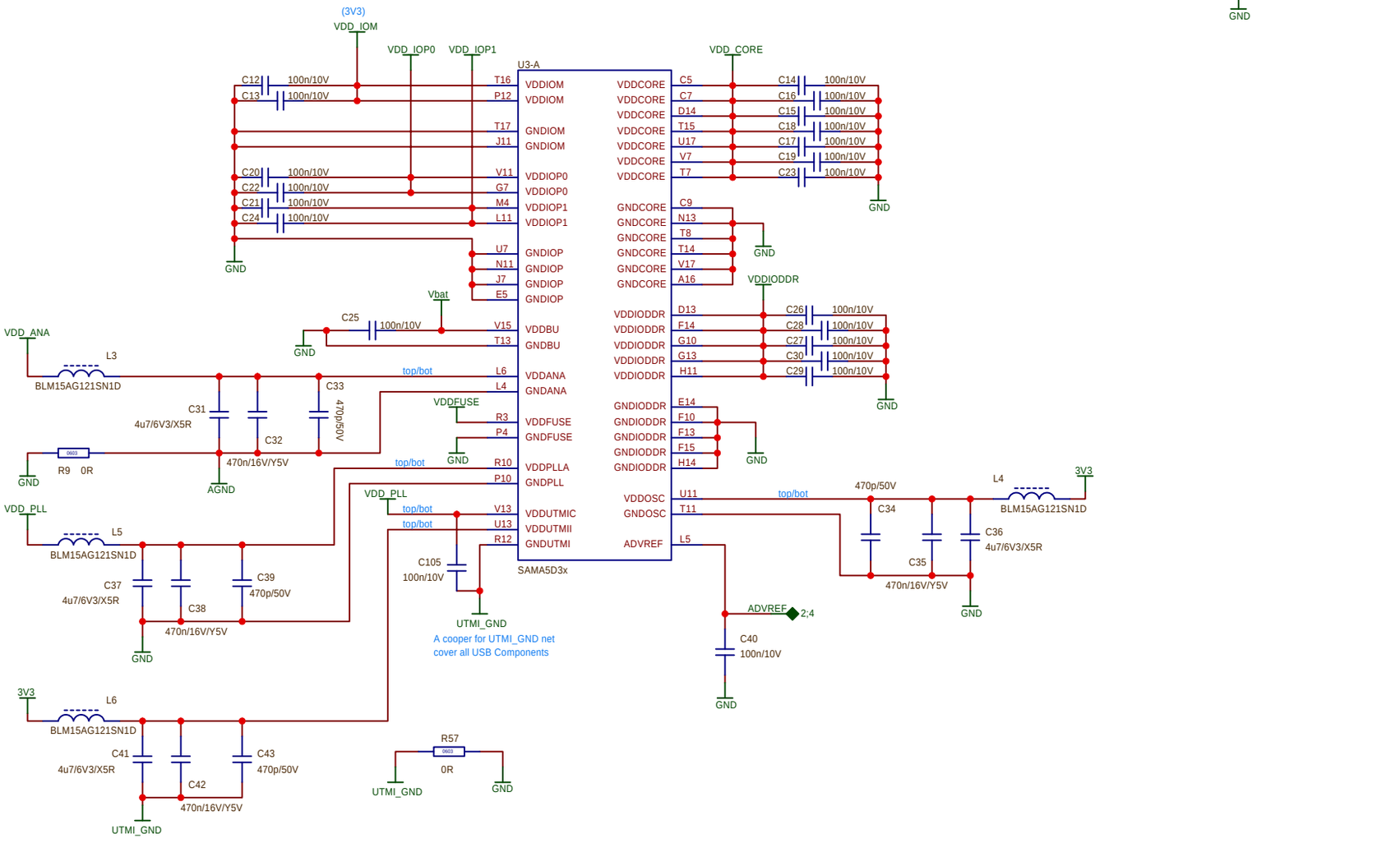


TABLE 1 — RS1=(Vout-1)xRS2

VDD_CORE	1.0V	1.2V	1.25V	
RS1	0R (JUMP)	2kOhm 1%	2k5ohm 1%	2k49ohm 1%
RS2	DNP	10kOhm 1%	10kOhm 1%	
US1	BU10TD3WG-TR	BU12TD3WG-TR		

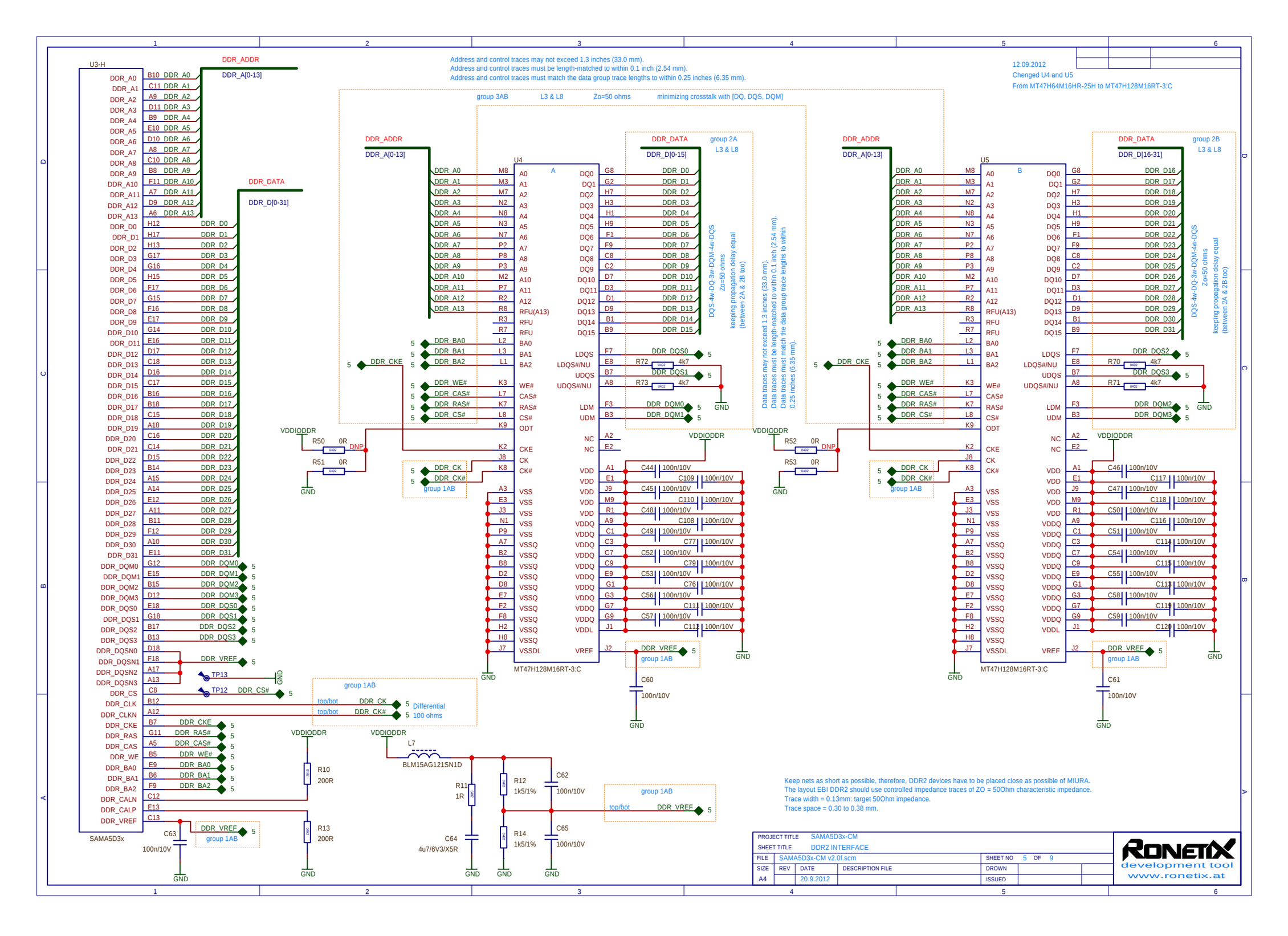
PROJECT TITLE	SAMA5D3x-CM				
SHEET TITLE	POWER SUPPLY				
FILE	SAMA5D3x-CM v2.0f.scm			SHEET NO 3 OF 9	
SIZE	REV	DATE	DESCRIPTION FILE	DROWN	
A4		20.9.2012		ISSUED	

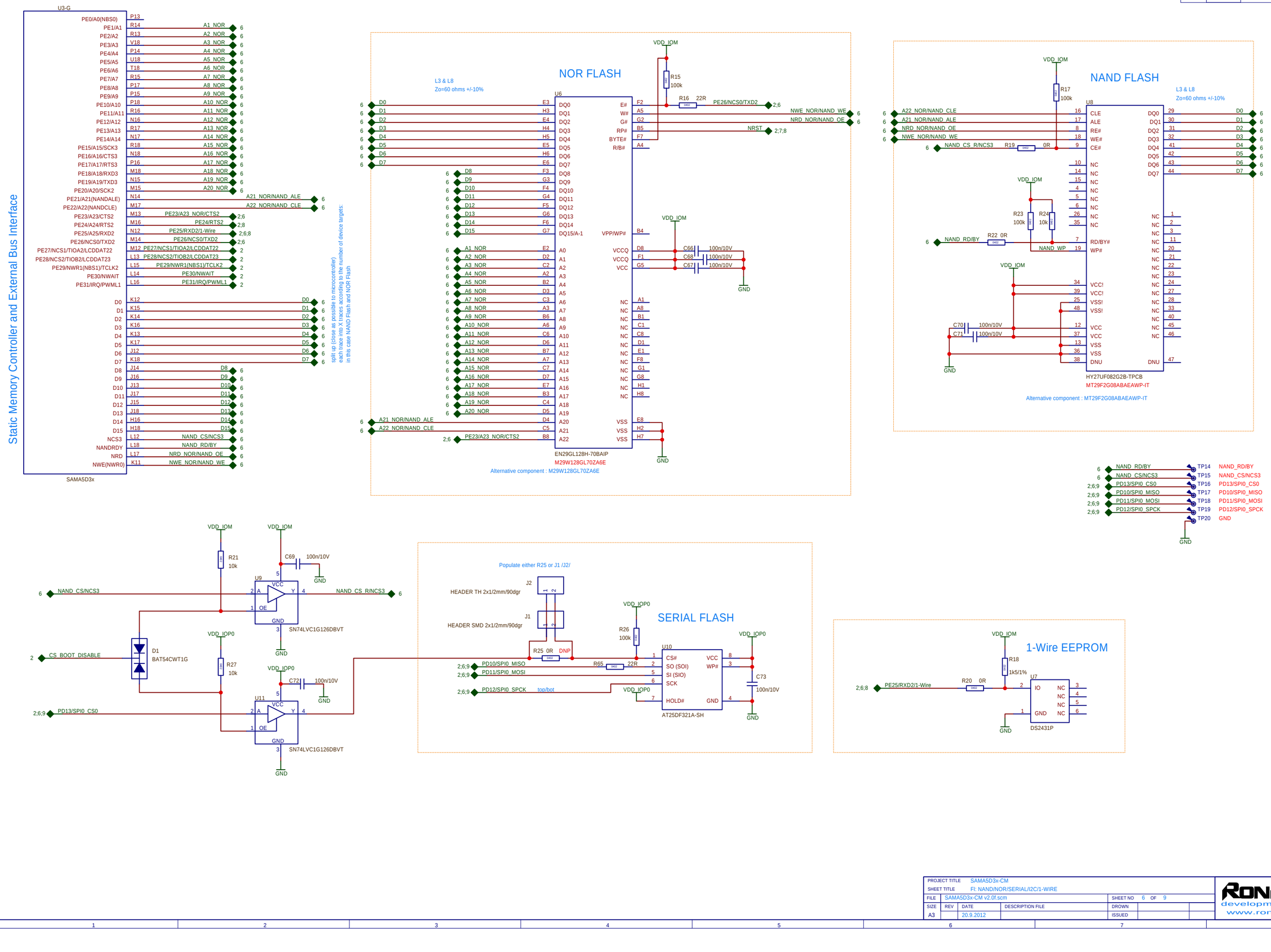
RONETIX development tool www.ronetix.at

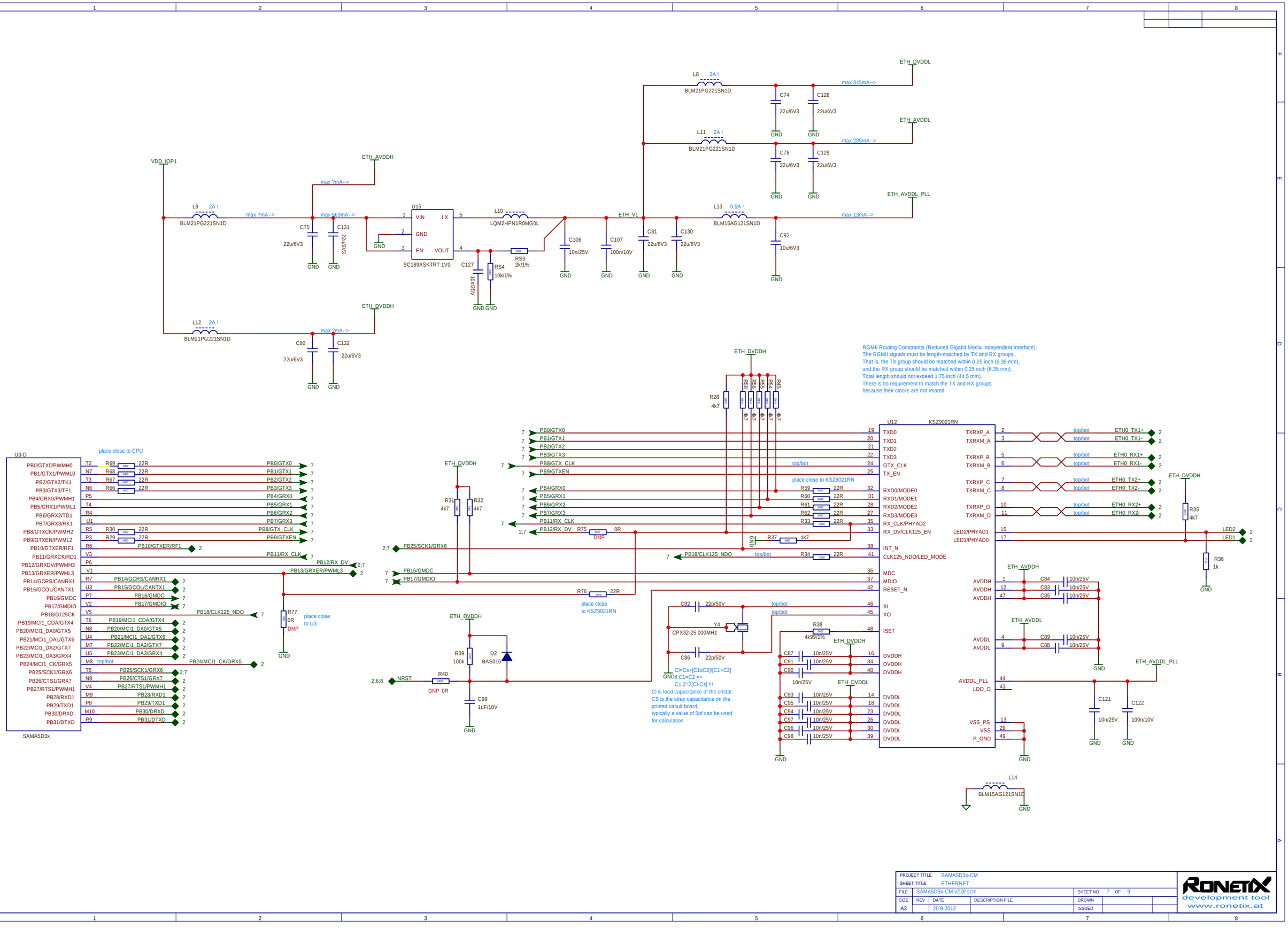


PROJECT TITLE	SAMA5D3x-CM						
SHEET TITLE	CPU-POWER SUPPLY						
FILE	SAMA5D3x-CM v2.0f.scm				SHEET NO	4 OF 9	
SIZE	REV	DATE	DESCRIPTION FILE		DROWN		
A4		20.9.2012			ISSUED		

RONETIX development tool www.ronetix.at


Address and control traces may not exceed 1.3 inches (33.0 mm).
Address and control traces must be length-matched to within 0.1 inch (2.54 mm).
Address and control traces must match the data group trace lengths to within 0.25 inches (6.35 mm).
12.09.2012
Chenged U4 and U5
From MT47H64M16HR-25H to MT47H128M16RT-3:C
group 3AB L3 & L8 Zo=50 ohms minimizing crosstalk with [DQ, DQS, DQM]
U3-H
SAMA5D3x
DDR_ADDR
DDR_A[0-13]
DDR_DATA
DDR_D[0-31]
U4
U5
MT47H128M16RT-3:C
DDR_D[0-15]
DDR_D[16-31]
group 2A L3 & L8
group 2B L3 & L8
DQS-4w-DQ-3w-DQM-4w-DQS Zo=50 ohms keeping propagation delay equal (between 2A & 2B too)
Data traces may not exceed 1.3 inches (33.0 mm). Data traces must be length-matched to within 0.1 inch (2.54 mm). Data traces must match the data group trace lengths to within 0.25 inches (6.35 mm).
group 1AB
top/bot
Differential 100 ohms
VDDIODDR
DNP
TP13
TP12
L7
BLM15AG121SN1D
C60
C61
C62
C63
C64
C65
R10 200R
R11 1R
R12 1k5/1%
R13 200R
R14 1k5/1%
100n/10V
4u7/6V3/X5R
GND
Keep nets as short as possible, therefore, DDR2 devices have to be placed close as possible of MIURA.
The layout EBI DDR2 should use controlled impedance traces of ZO = 50Ohm characteristic impedance.
Trace width = 0.13mm: target 50Ohm impedance.
Trace space = 0.30 to 0.38 mm.
PROJECT TITLE SAMA5D3x-CM
SHEET TITLE DDR2 INTERFACE
FILE SAMA5D3x-CM v2.0f.scm
SHEET NO 5 OF 9
SIZE A4
REV
DATE 20.9.2012
DESCRIPTION FILE
DROWN
ISSUED
RONETIX development tool www.ronetix.at


Static Memory Controller and External Bus Interface
U3-G
SAMA5D3x
NOR FLASH
L3 & L8
Zo=60 ohms +/-10%
U6
EN29GL128H-70BAIP
M29W128GL70ZA6E
Alternative component : M29W128GL70ZA6E
split up (close as possible to microcontroller)
each trace into X traces according to the number of device targets:
in this case NAND Flash and NOR Flash
NAND FLASH
L3 & L8
Zo=60 ohms +/-10%
U8
HY27UF082G2B-TPCB
MT29F2G08ABAEAWP-IT
Alternative component : MT29F2G08ABAEAWP-IT
SERIAL FLASH
Populate either R25 or J1 /J2/
HEADER TH 2x1/2mm/90dgr
HEADER SMD 2x1/2mm/90dgr
top/bot
U10
AT25DF321A-SH
1-Wire EEPROM
U7
DS2431P
SN74LVC1G126DBVT
BAT54CWT1G
TP14 NAND_RD/BY
TP15 NAND_CS/NCS3
TP16 PD13/SPI0_CS0
TP17 PD10/SPI0_MISO
TP18 PD11/SPI0_MOSI
TP19 PD12/SPI0_SPCK
TP20 GND
PROJECT TITLE SAMA5D3x-CM
SHEET TITLE FI: NAND/NOR/SERIAL/I2C/1-WIRE
FILE SAMA5D3x-CM v2.0f.scm
SHEET NO 6 OF 9
SIZE A3
REV
DATE 20.9.2012
DESCRIPTION FILE
DROWN
ISSUED
RONETIX
development tool
www.ronetix.at


VDD_IOP1
ETH_AVDDH
ETH_DVDDL
ETH_AVDDL
ETH_AVDDL_PLL
ETH_DVDDH
ETH_V1
L8 2A ! BLM21PG221SN1D
L9 2A ! BLM21PG221SN1D
L10 LQM2HPN1R0MG0L
L11 2A ! BLM21PG221SN1D
L12 2A ! BLM21PG221SN1D
L13 0.5A ! BLM15AG121SN1D
max 345mA-->
max 205mA-->
max ?mA-->
max 563mA-->
max 13mA-->
C74 22u/6V3
C128 22u/6V3
C78 22u/6V3
C129 22u/6V3
C75 22u/6V3
C131 22u/6V3
C80 22u/6V3
C132 22u/6V3
C106 10n/25V
C107 100n/10V
C81 22u/6V3
C130 22u/6V3
C92 10u/6V3
C127 10n/25V
RS3 2k/1%
RS4 10k/1%
U15
VIN
LX
GND
EN
VOUT
SC189ASKTRT 1V0
GND
U3-D
SAMA5D3x
place close to CPU
PB0/GTX0/PWMH0
PB1/GTX1/PWML0
PB2/GTX2/TK1
PB3/GTX3/TF1
PB4/GRX0/PWMH1
PB5/GRX1/PWML1
PB6/GRX2/TD1
PB7/GRX3/RK1
PB8/GTXCK/PWMH2
PB9/GTXEN/PWML2
PB10/GTXER/RF1
PB11/GRXCK/RD1
PB12/GRXDV/PWMH3
PB13/GRXER/PWML3
PB14/GCRS/CANRX1
PB15/GCOL/CANTX1
PB16/GMDC
PB17/GMDIO
PB18/G125CK
PB19/MCI1_CDA/GTX4
PB20/MCI1_DA0/GTX5
PB21/MCI1_DA1/GTX6
PB22/MCI1_DA2/GTX7
PB23/MCI1_DA3/GRX4
PB24/MCI1_CK/GRX5
PB25/SCK1/GRX6
PB26/CTS1/GRX7
PB27/RTS1/PWMH1
PB28/RXD1
PB29/TXD1
PB30/DRXD
PB31/DTXD
PB18/CLK125_NDO
PB24/MCI1_CK/GRX5
R69 22R
R68 22R
R67 22R
R66 22R
R30 22R
R29 22R
R77 0R DNP
place close to U3
top/bot
RGMII Routing Constraints (Reduced Gigabit Media Independent Interface):
The RGMII signals must be length-matched by TX and RX groups.
That is, the TX group should be matched within 0.25 inch (6.35 mm),
and the RX group should be matched within 0.25 inch (6.35 mm).
Total length should not exceed 1.75 inch (44.5 mm).
There is no requirement to match the TX and RX groups
because their clocks are not related.
R28 4k7
R58 4k7
R55 4k7
R56 4k7
R54 4k7
R45 4k7
U12 KSZ9021RN
PB0/GTX0
PB1/GTX1
PB2/GTX2
PB3/GTX3
PB8/GTX_CLK
PB9/GTXEN
PB4/GRX0
PB5/GRX1
PB6/GRX2
PB7/GRX3
PB11/RX_CLK
PB12/RX_DV
PB25/SCK1/GRX6
PB16/GMDC
PB17/GMDIO
PB18/CLK125_NDO
TXD0
TXD1
TXD2
TXD3
GTX_CLK
TX_EN
RXD0/MODE0
RXD1/MODE1
RXD2/MODE2
RXD3/MODE3
RX_CLK/PHYAD2
RX_DV/CLK125_EN
INT_N
CLK125_NDO/LED_MODE
MDC
MDIO
RESET_N
XI
XO
ISET
DVDDH
DVDDL
VSS
P_GND
place close to KSZ9021RN
R59 22R
R60 22R
R61 22R
R62 22R
R33 22R
R34 22R
R37 4k7
R75 0R DNP
R76 22R
TXRXP_A
TXRXM_A
TXRXP_B
TXRXM_B
TXRXP_C
TXRXM_C
TXRXP_D
TXRXM_D
LED2/PHYAD1
LED1/PHYAD0
ETH0_TX1+
ETH0_TX1-
ETH0_RX1+
ETH0_RX1-
ETH0_TX2+
ETH0_TX2-
ETH0_RX2+
ETH0_RX2-
LED2
LED1
R35 4k7
R36 1k
AVDDH
AVDDL
AVDDL_PLL
LDO_O
C84 10n/25V
C83 10n/25V
C85 10n/25V
C89 10n/25V
C88 10n/25V
C121 10n/25V
C122 100n/10V
R31 4k7
R32 4k7
R39 100k
D2 BAS316
R40 DNP 0R
NRST
C99 1uF/10V
C82 22p/50V
C86 22p/50V
Y4 CPX32-25.000MHz
R38 4k99/1%
C87 10n/25V
C91 10n/25V
C90 10n/25V
C93 10n/25V
C95 10n/25V
C94 10n/25V
C97 10n/25V
C96 10n/25V
C98 10n/25V
CL=Cs+[C1xC2]/[C1+C2]
if C1=C2 =>
C1,2=2[Cl-Cs] !!!
Cl is load capacitance of the cristal.
CS is the stray capacitance on the
printed circuit board,
typically a value of 5pf can be used
for calculation
L14 BLM15AG121SN1D
PROJECT TITLE SAMA5D3x-CM
SHEET TITLE ETHERNET
FILE SAMA5D3x-CM v2.0f.scm
SHEET NO 7 OF 9
SIZE A3
REV
DATE 20.9.2012
DESCRIPTION FILE
DROWN
ISSUED
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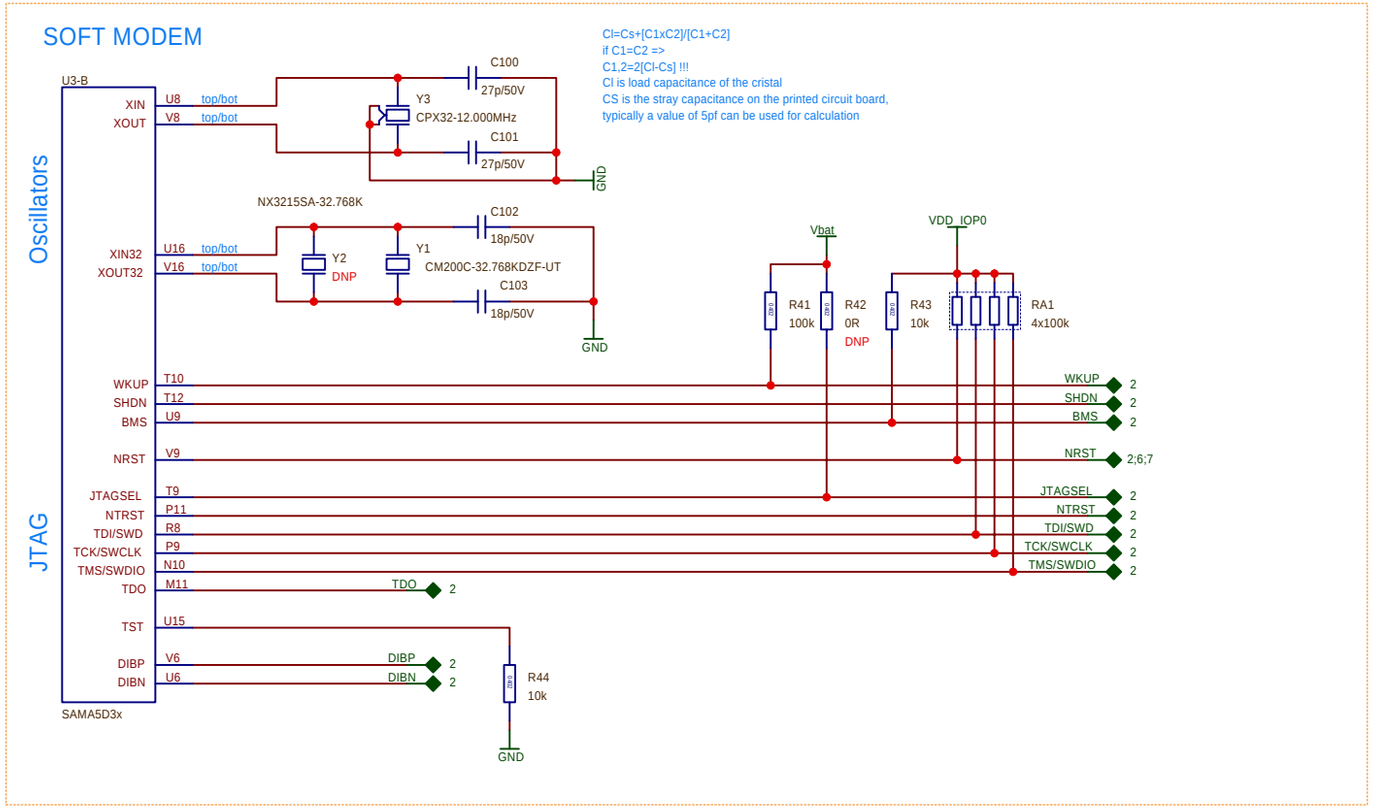

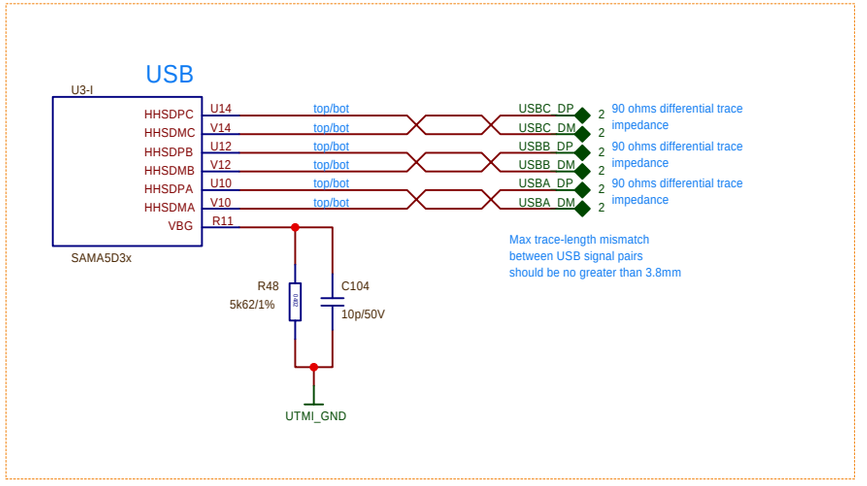

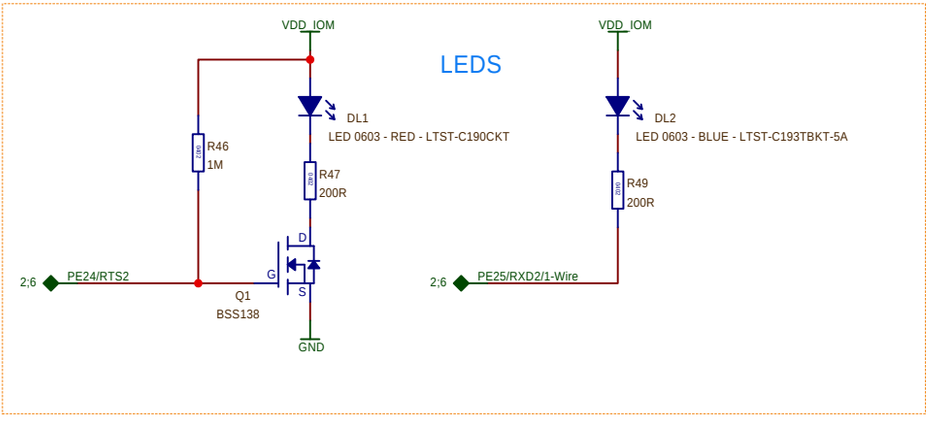

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SHEET TITLE	USB/JTAG/LEDS				
FILE	SAMA5D3x-CM v2.0f.scm			SHEET NO 8 OF 9	
SIZE	REV	DATE	DESCRIPTION FILE	DROWN	
A4		20.9.2012		ISSUED	

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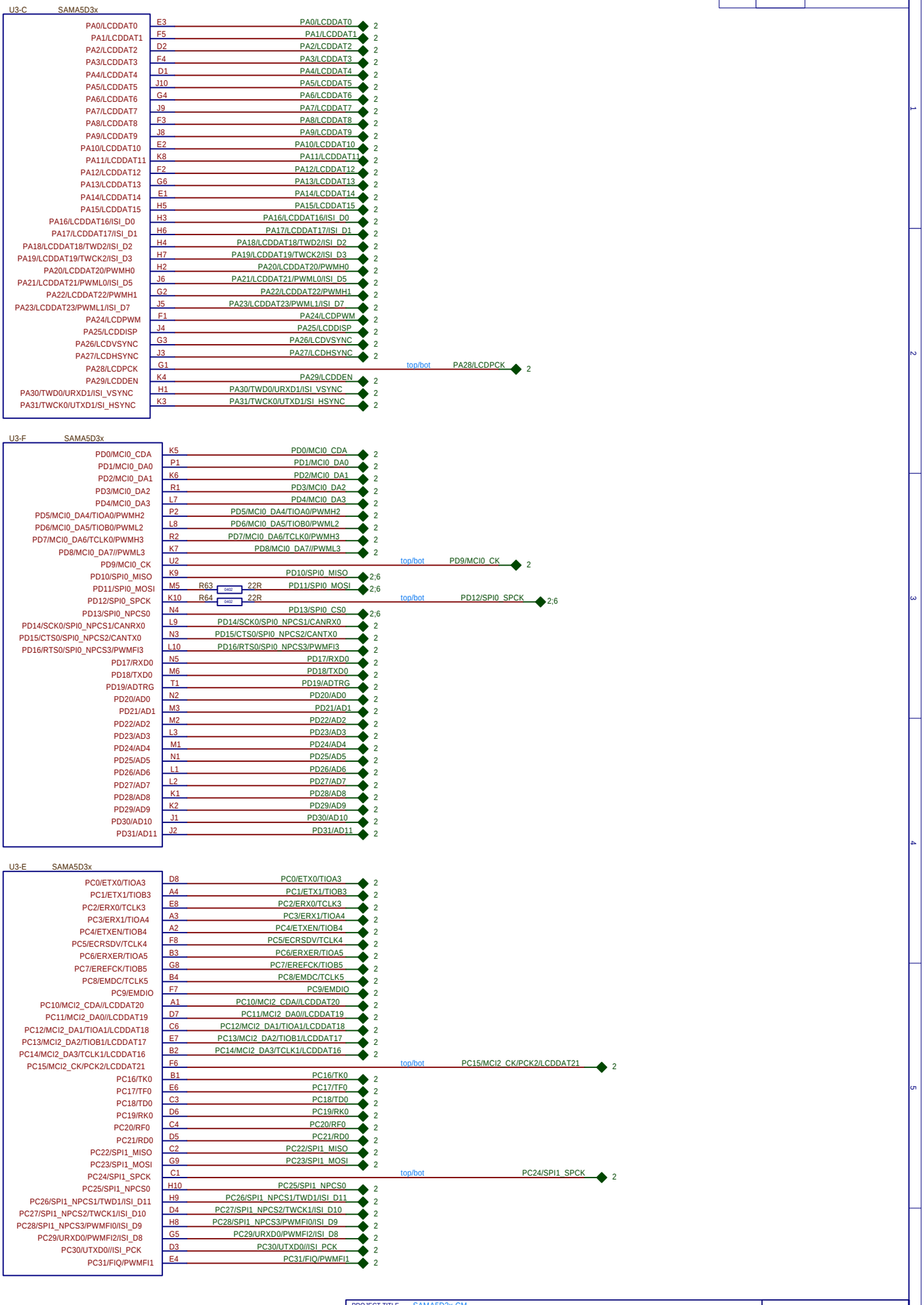
U3-C SAMA5D3x
PA0/LCDDAT0 E3 PA0/LCDDAT0 2
PA1/LCDDAT1 F5 PA1/LCDDAT1 2
PA2/LCDDAT2 D2 PA2/LCDDAT2 2
PA3/LCDDAT3 F4 PA3/LCDDAT3 2
PA4/LCDDAT4 D1 PA4/LCDDAT4 2
PA5/LCDDAT5 J10 PA5/LCDDAT5 2
PA6/LCDDAT6 G4 PA6/LCDDAT6 2
PA7/LCDDAT7 J9 PA7/LCDDAT7 2
PA8/LCDDAT8 F3 PA8/LCDDAT8 2
PA9/LCDDAT9 J8 PA9/LCDDAT9 2
PA10/LCDDAT10 E2 PA10/LCDDAT10 2
PA11/LCDDAT11 K8 PA11/LCDDAT11 2
PA12/LCDDAT12 F2 PA12/LCDDAT12 2
PA13/LCDDAT13 G6 PA13/LCDDAT13 2
PA14/LCDDAT14 E1 PA14/LCDDAT14 2
PA15/LCDDAT15 H5 PA15/LCDDAT15 2
PA16/LCDDAT16/ISI_D0 H3 PA16/LCDDAT16/ISI_D0 2
PA17/LCDDAT17/ISI_D1 H6 PA17/LCDDAT17/ISI_D1 2
PA18/LCDDAT18/TWD2/ISI_D2 H4 PA18/LCDDAT18/TWD2/ISI_D2 2
PA19/LCDDAT19/TWCK2/ISI_D3 H7 PA19/LCDDAT19/TWCK2/ISI_D3 2
PA20/LCDDAT20/PWMH0 H2 PA20/LCDDAT20/PWMH0 2
PA21/LCDDAT21/PWML0/ISI_D5 J6 PA21/LCDDAT21/PWML0/ISI_D5 2
PA22/LCDDAT22/PWMH1 G2 PA22/LCDDAT22/PWMH1 2
PA23/LCDDAT23/PWML1/ISI_D7 J5 PA23/LCDDAT23/PWML1/ISI_D7 2
PA24/LCDPWM F1 PA24/LCDPWM 2
PA25/LCDDISP J4 PA25/LCDDISP 2
PA26/LCDVSYNC G3 PA26/LCDVSYNC 2
PA27/LCDHSYNC J3 PA27/LCDHSYNC 2
PA28/LCDPCK G1 top/bot PA28/LCDPCK 2
PA29/LCDDEN K4 PA29/LCDDEN 2
PA30/TWD0/URXD1/ISI_VSYNC H1 PA30/TWD0/URXD1/ISI_VSYNC 2
PA31/TWCK0/UTXD1/SI_HSYNC K3 PA31/TWCK0/UTXD1/SI_HSYNC 2
U3-F SAMA5D3x
PD0/MCI0_CDA K5 PD0/MCI0_CDA 2
PD1/MCI0_DA0 P1 PD1/MCI0_DA0 2
PD2/MCI0_DA1 K6 PD2/MCI0_DA1 2
PD3/MCI0_DA2 R1 PD3/MCI0_DA2 2
PD4/MCI0_DA3 L7 PD4/MCI0_DA3 2
PD5/MCI0_DA4/TIOA0/PWMH2 P2 PD5/MCI0_DA4/TIOA0/PWMH2 2
PD6/MCI0_DA5/TIOB0/PWML2 L8 PD6/MCI0_DA5/TIOB0/PWML2 2
PD7/MCI0_DA6/TCLK0/PWMH3 R2 PD7/MCI0_DA6/TCLK0/PWMH3 2
PD8/MCI0_DA7//PWML3 K7 PD8/MCI0_DA7//PWML3 2
PD9/MCI0_CK U2 top/bot PD9/MCI0_CK 2
PD10/SPI0_MISO K9 PD10/SPI0_MISO 2;6
PD11/SPI0_MOSI M5 R63 0402 22R PD11/SPI0_MOSI 2;6
PD12/SPI0_SPCK K10 R64 0402 22R top/bot PD12/SPI0_SPCK 2;6
PD13/SPI0_NPCS0 N4 PD13/SPI0_CS0 2;6
PD14/SCK0/SPI0_NPCS1/CANRX0 L9 PD14/SCK0/SPI0_NPCS1/CANRX0 2
PD15/CTS0/SPI0_NPCS2/CANTX0 N3 PD15/CTS0/SPI0_NPCS2/CANTX0 2
PD16/RTS0/SPI0_NPCS3/PWMFI3 L10 PD16/RTS0/SPI0_NPCS3/PWMFI3 2
PD17/RXD0 N5 PD17/RXD0 2
PD18/TXD0 M6 PD18/TXD0 2
PD19/ADTRG T1 PD19/ADTRG 2
PD20/AD0 N2 PD20/AD0 2
PD21/AD1 M3 PD21/AD1 2
PD22/AD2 M2 PD22/AD2 2
PD23/AD3 L3 PD23/AD3 2
PD24/AD4 M1 PD24/AD4 2
PD25/AD5 N1 PD25/AD5 2
PD26/AD6 L1 PD26/AD6 2
PD27/AD7 L2 PD27/AD7 2
PD28/AD8 K1 PD28/AD8 2
PD29/AD9 K2 PD29/AD9 2
PD30/AD10 J1 PD30/AD10 2
PD31/AD11 J2 PD31/AD11 2
U3-E SAMA5D3x
PC0/ETX0/TIOA3 D8 PC0/ETX0/TIOA3 2
PC1/ETX1/TIOB3 A4 PC1/ETX1/TIOB3 2
PC2/ERX0/TCLK3 E8 PC2/ERX0/TCLK3 2
PC3/ERX1/TIOA4 A3 PC3/ERX1/TIOA4 2
PC4/ETXEN/TIOB4 A2 PC4/ETXEN/TIOB4 2
PC5/ECRSDV/TCLK4 F8 PC5/ECRSDV/TCLK4 2
PC6/ERXER/TIOA5 B3 PC6/ERXER/TIOA5 2
PC7/EREFCK/TIOB5 G8 PC7/EREFCK/TIOB5 2
PC8/EMDC/TCLK5 B4 PC8/EMDC/TCLK5 2
PC9/EMDIO F7 PC9/EMDIO 2
PC10/MCI2_CDA//LCDDAT20 A1 PC10/MCI2_CDA//LCDDAT20 2
PC11/MCI2_DA0//LCDDAT19 D7 PC11/MCI2_DA0//LCDDAT19 2
PC12/MCI2_DA1/TIOA1/LCDDAT18 C6 PC12/MCI2_DA1/TIOA1/LCDDAT18 2
PC13/MCI2_DA2/TIOB1/LCDDAT17 E7 PC13/MCI2_DA2/TIOB1/LCDDAT17 2
PC14/MCI2_DA3/TCLK1/LCDDAT16 B2 PC14/MCI2_DA3/TCLK1/LCDDAT16 2
PC15/MCI2_CK/PCK2/LCDDAT21 F6 top/bot PC15/MCI2_CK/PCK2/LCDDAT21 2
PC16/TK0 B1 PC16/TK0 2
PC17/TF0 E6 PC17/TF0 2
PC18/TD0 C3 PC18/TD0 2
PC19/RK0 D6 PC19/RK0 2
PC20/RF0 C4 PC20/RF0 2
PC21/RD0 D5 PC21/RD0 2
PC22/SPI1_MISO C2 PC22/SPI1_MISO 2
PC23/SPI1_MOSI G9 PC23/SPI1_MOSI 2
PC24/SPI1_SPCK C1 top/bot PC24/SPI1_SPCK 2
PC25/SPI1_NPCS0 H10 PC25/SPI1_NPCS0 2
PC26/SPI1_NPCS1/TWD1/ISI_D11 H9 PC26/SPI1_NPCS1/TWD1/ISI_D11 2
PC27/SPI1_NPCS2/TWCK1/ISI_D10 D4 PC27/SPI1_NPCS2/TWCK1/ISI_D10 2
PC28/SPI1_NPCS3/PWMFI0/ISI_D9 H8 PC28/SPI1_NPCS3/PWMFI0/ISI_D9 2
PC29/URXD0/PWMFI2/ISI_D8 G5 PC29/URXD0/PWMFI2/ISI_D8 2
PC30/UTXD0//ISI_PCK D3 PC30/UTXD0//ISI_PCK 2
PC31/FIQ/PWMFI1 E4 PC31/FIQ/PWMFI1 2
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SHEET TITLE BUS INTERFACE
FILE SAMA5D3x-CM v2.0f.scm
SHEET NO 9 OF 9
SIZE A4
REV
DATE 20.9.2012
DESCRIPTION FILE
DROWN
ISSUED
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Section 6

Main Board (MB)

6.1 Main Board Overview

The SAMA5D3 series-MB board serves as the main board that carries the CPU module. It features all necessary peripheral devices and interfaces for processor evaluation.

Figure 6-1. Main Board Top View

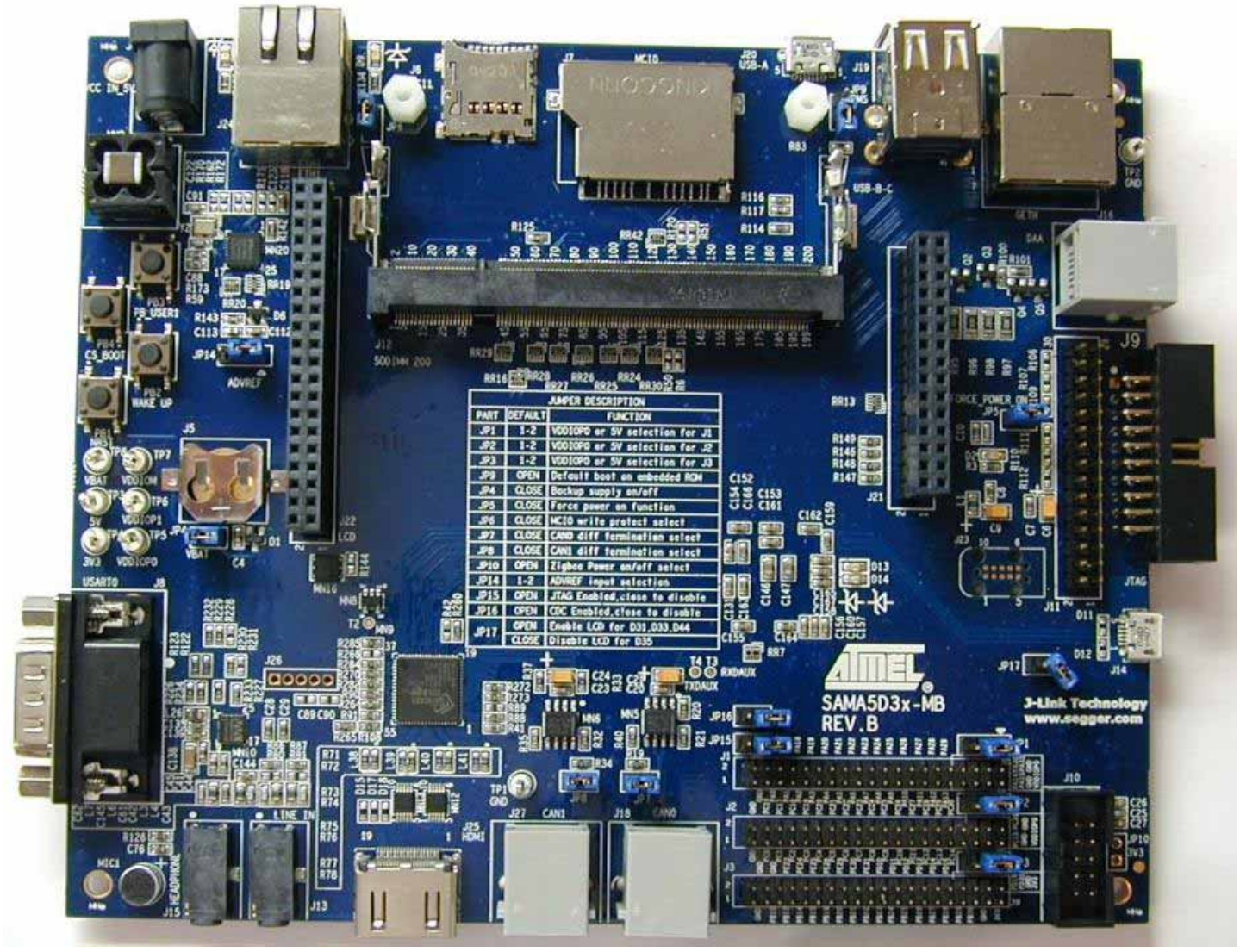
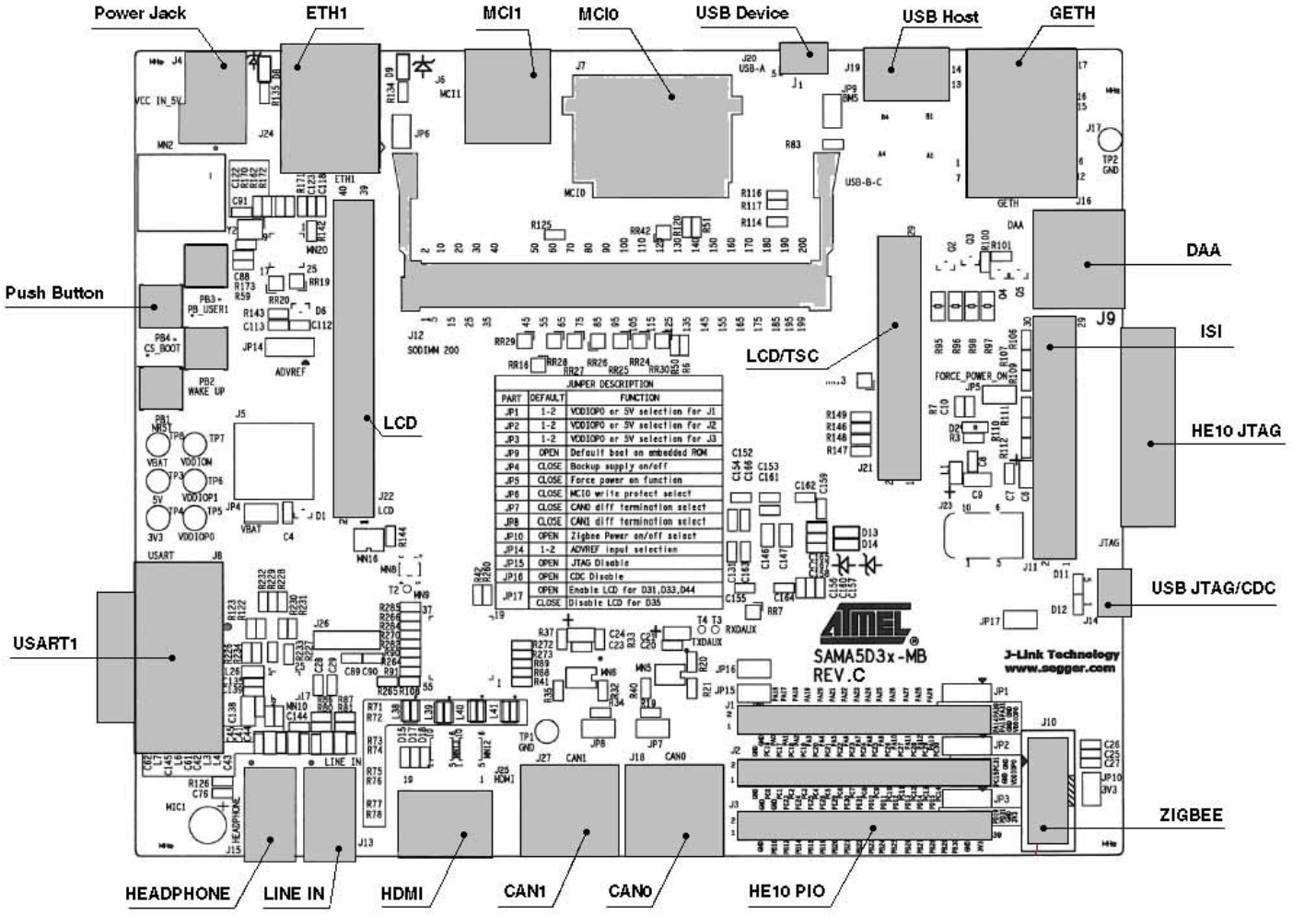


Figure 6-2. MB Board Layout Commented



6.1.1 Equipment List

The SAMA5D3 series-MB is a full featured mother board .

Due to the embedded module concept this baseboard can be used with every available SAMA5D3 series-CM CPU module.

6.1.2 Technical specifications

Table 6-1. MB Technical Specifications

Characteristic	Specifications
Supported Module	All SAMA5D3 series computer modules
Expansion Slots	One 200-pin SODIMM socket
Mass Storage Interface	Two High Speed memory card Hosts (eMMC 4.3 and SD 2.0) 1 x SD card slot 1 x mini SD card slot
I/O	3 x 20 pin header 1 x 20 + 1 x 15 pin header LCD connector 1 x 10 pin header ISI connector (Image Sensor) One 1-Wire EEPROM DS28EC20 One power LED
Communication	1 x Gigabit Ethernet 1 x 10/100 MHz Ethernet 2 x USB Host High Speed 2.0 1 x USB Host/Device High Speed 2.0 1 x USARTs, 1 x DBGU 2 x CAN connectors 1 x 10 pin header ZigBee connector 1 x Smart DAA (Softmodem interface)
Sound	Wolfson's 8904 Mic in, Headphone out signals
Video	1 x HDMI
LCD	LCD TFT Controller with overlay, alpha-blending, rotation, scaling and color space conversion
ISI	ITU-R BT. 601/656 Image Sensor Interface
Debug	1 x On board SAM-ICE 1 x Bridge USB/UART DBGU
CMOS Battery	On Board Lithium Battery for CMOS backup
Power	System power: +5V DC +/-5% Backup: +1.65V to 3.6V DC
Temperature: operating storage	 0°C to +60°C -40°C to +85°C
Dimensions	165 * 135 * 20 mm

Note: Some of the features mentioned in the above feature summary table are optional. Check the article number of your module and compare it to the option information list on Table 4-1 on page 4-1 of this user's guide to determine which options are available with your particular module.

6.1.3 Devices

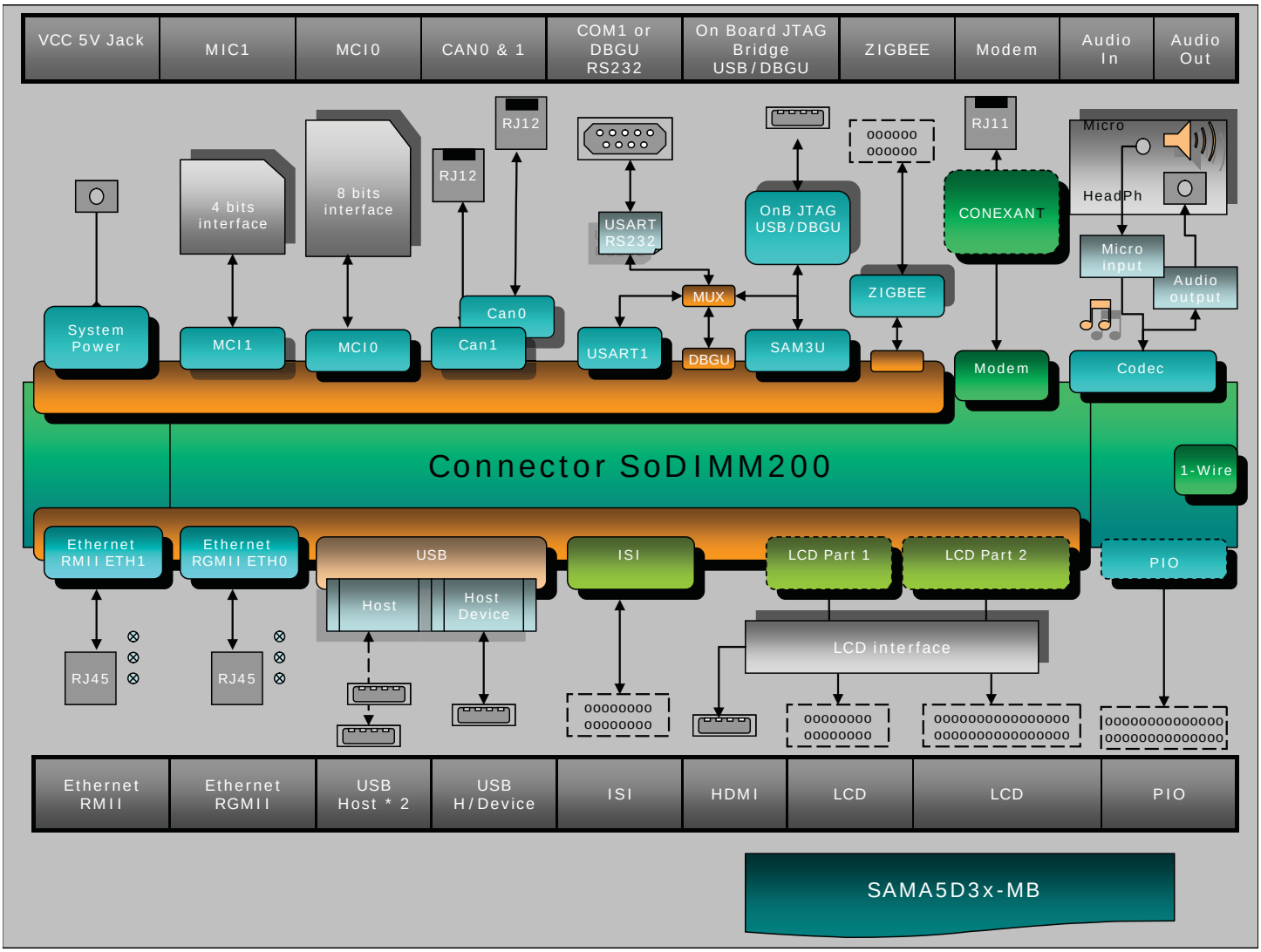
List of the MB board peripherals:

- Two EMAC PHY
- One audio CODEC
- Two high speed MCI card interfaces
- Two CAN transceivers
- One RS232 port with level translator features USART1
- One smart DAA port
- Two USB host port
- One USB host/device port
- On-board power regulation
- LCD/ISI extension interface
- HDMI interface
- ZigBee® interface
- One-wire device

6.1.4 Board Interface Connection

- Main power supply (J4)
- 200 positions socket (as defined in SODIMM 200), 0.6mm pitch (J12)
- USB A Host/Device, support USB host/device using a type micro AB connector (J20)
- USB B Host, support USB host using a type A connector (J19, upper)
- USB C Host, support USB host using a type A connector (J19, lower)
- USB-to-serial bridge on DBGU, and JTAG-OB functionality (J14)
- USART1 (RX, TX, RTS, CTS) connected to a 9-way male RS232 connector (J8)
- JTAG, 20 pin IDC connector (J9)
- MicroSD connector (J6)
- SD/MMC connector (J7)
- Gigabit Ethernet ETH0 (J17)
- Ethernet ETH1 (J24)
- Headphone (J15), line (J13)
- Image sensor connector (J11)
- HDMI connector (J25)
- Expansion connector with all LCD controller signals for DM board connection (QTouch, TFT LCD display with Touch Screen and backlight (J21, J22))
- DAA connecter RJ11 6P4C type (J16)
- CAN bus connectors RJ12 6P6C type (J18, J27)
- ZigBee connector (J10)
- Battery socket (J5)
- Three expansion connectors with PIO signals (J1, J2, J3)
- Test points; various test points are located throughout the board

Figure 6-3. MB Architecture

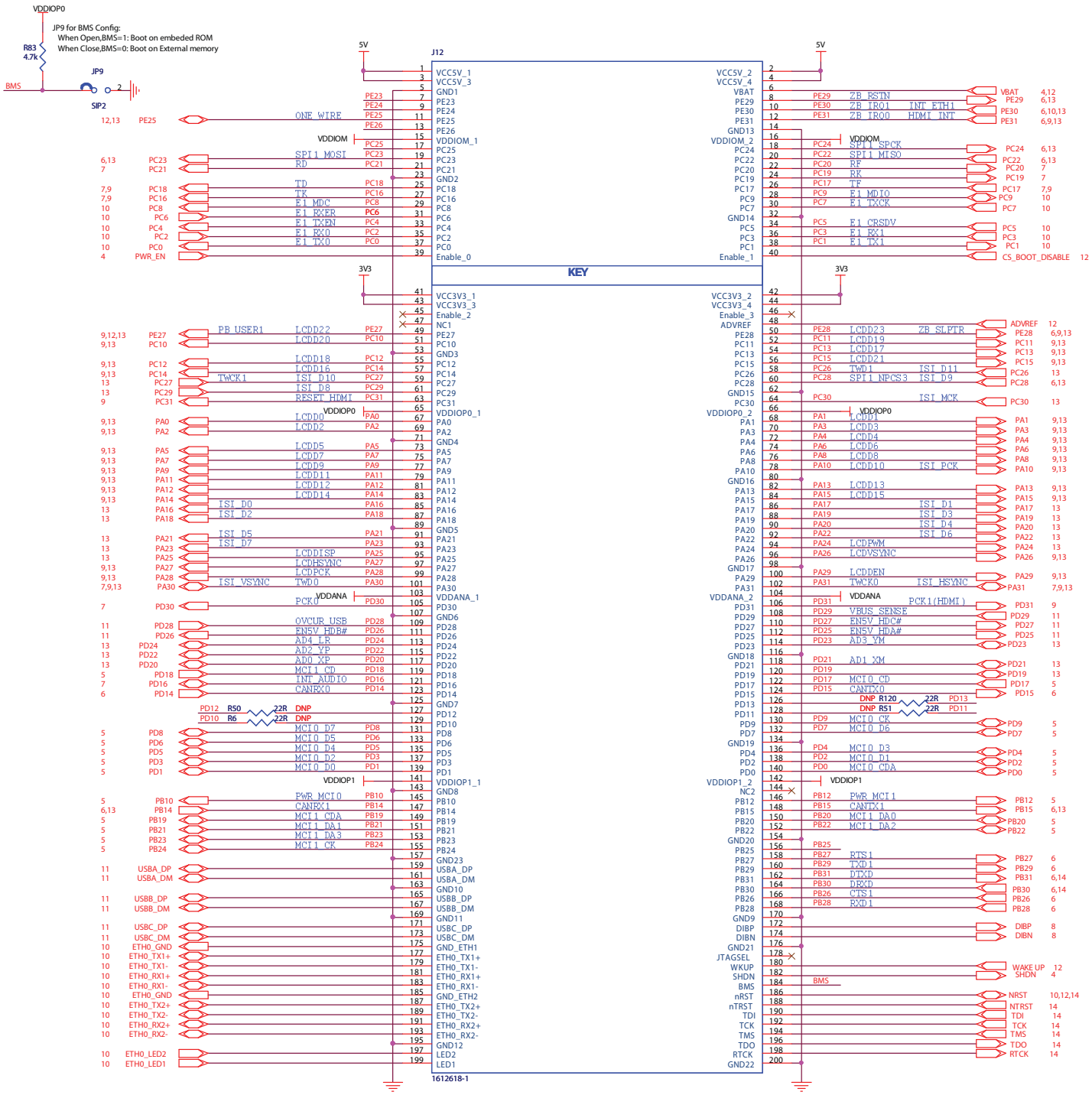


6.2 Function Blocks

6.2.1 Processor

The SAMA5D3 series-MB board may be used with any of the SAMA5D31/D33/D34/D35 CPU Modules.

Figure 6-4. SODIMM Interface on MB



6.2.2 Power Supplies

The SAMA5D3 series-MB board is supplied with a simple external 5 VCC power supply.

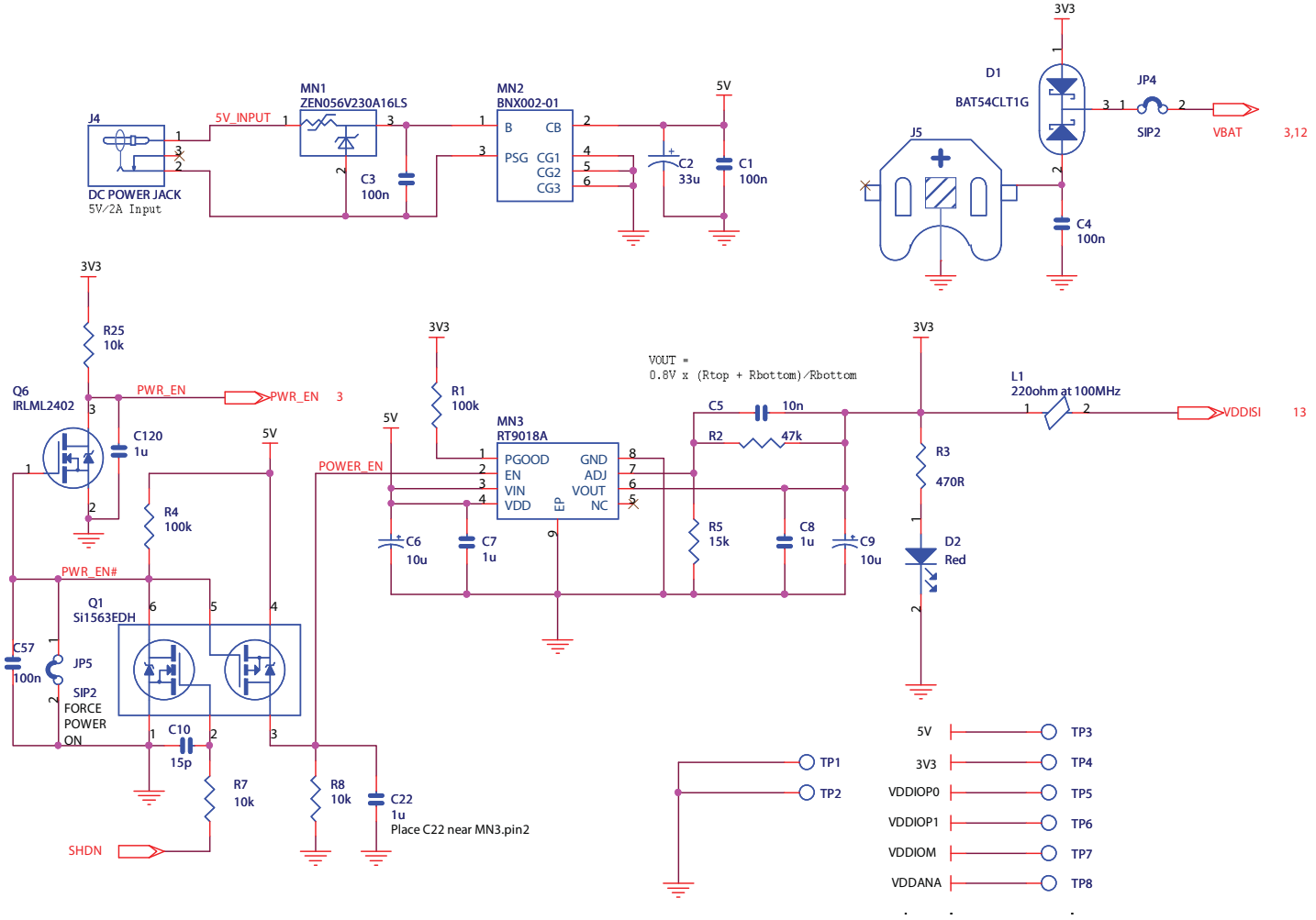
The SAMA5D3 series-MB Board features one adjustable LDO. It accepts DC in 5V power and outputs a regulated +3.3V to most other circuits on the board through four 3.3V rails.

6.2.2.1 Supply Group Configuration

This LDO is enabled through a dual FET scheme. The processor can assert SHDN (which is a VDDBU powered I/O) to shut down the LDO to enter the so called backup mode. The regulators on CM board are also shut down by the action of the SHDN signal.

If the 3V battery is mounted on J5, both CM and MB board can be woken up by action on the BP2 button, which drives the WKUP signal, (also a VDDBU powered I/O).

Figure 6-5. MB Power Management



6.2.3 Debug JTAG/ICE and DBGU

The Main Board embeds a SEGGER J-Link-on-Board based on an ATSAM3U4C LQFP100.

This processor provides the functions of JTAG and bridge USB/Serial DBGU port.

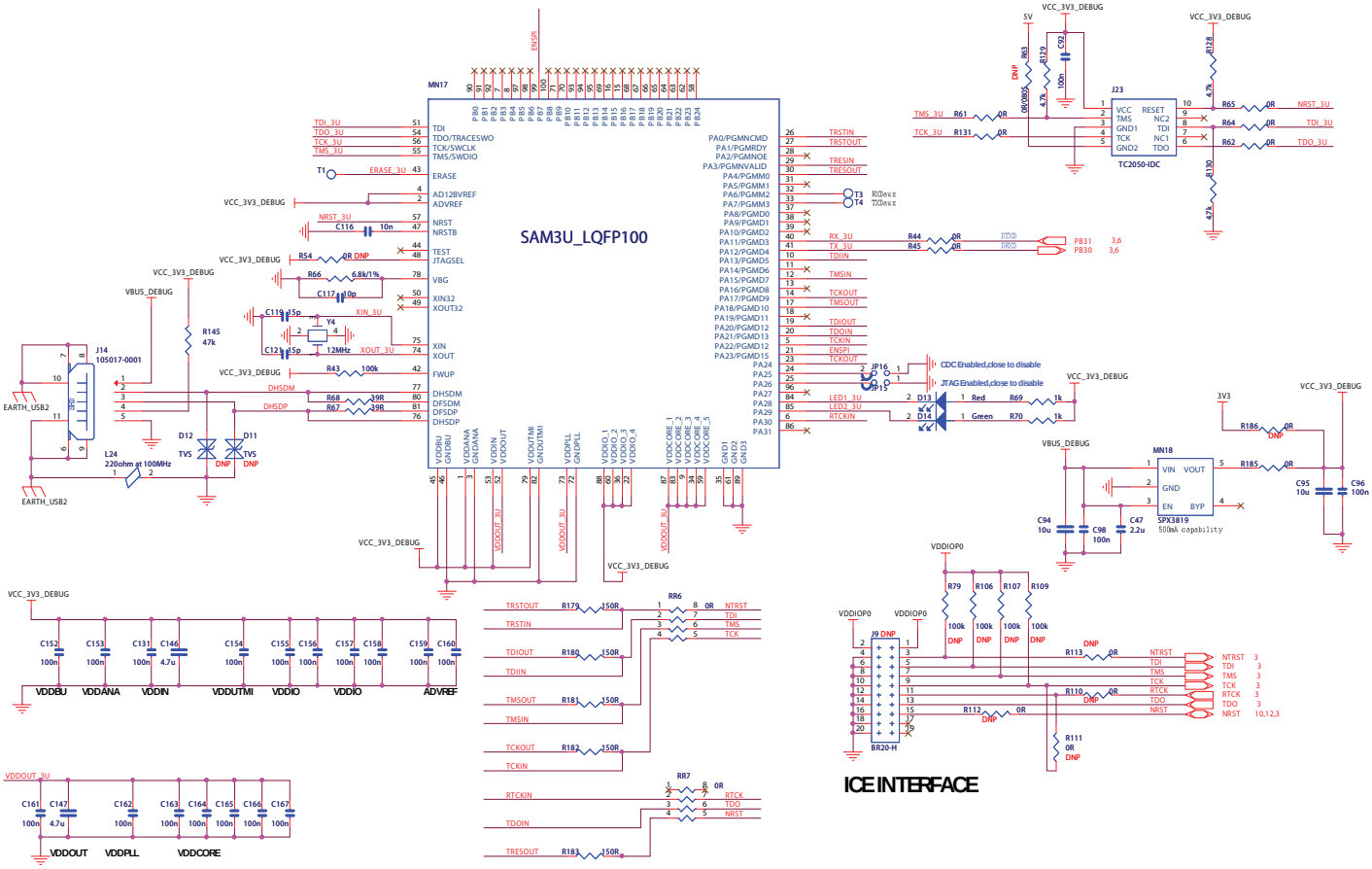
The J-Link-OB-ATSAM3U4C was designed in order to provide a low-cost, space-saving and onboard alternative to the general J-Link.

J-Link-OB-ATSAM3U4C supports the following target interfaces:

- JTAG
- DBGU

An optional 20 pin header is provided on the board to allow for the JTAG connection. In order to use this functionality RR6, RR7 should be removed and JP15 on.

Figure 6-6. MB JTAG-OB



6.2.3.1 Disabling J-Link-OB-SAM3U128

The J-Link-OB-ATSAM3U4C may be disabled by Jumper JP15 (PA26, pin 25 of the ATSAM3U4C CPU).

- Jumper not fitted: J-Link-OB-ATSAM3U4C is enabled and fully functional
- Jumper fitted: J-Link-OB-ATSAM3U4C is disabled

The pin uses internal pull-up (so if JP15 is not required, simply leave the pin on the J-Link-OB-ATSAM3U4C open), jumper shortens to ground. If J-Link is disabled, serial COM port via CDC is still functional.

Disabling the jumper is not required to use the external debugger since target interface (JTAG/SWD) remains disabled until first target communication takes place.

6.2.3.2 Hardware UART via CDC

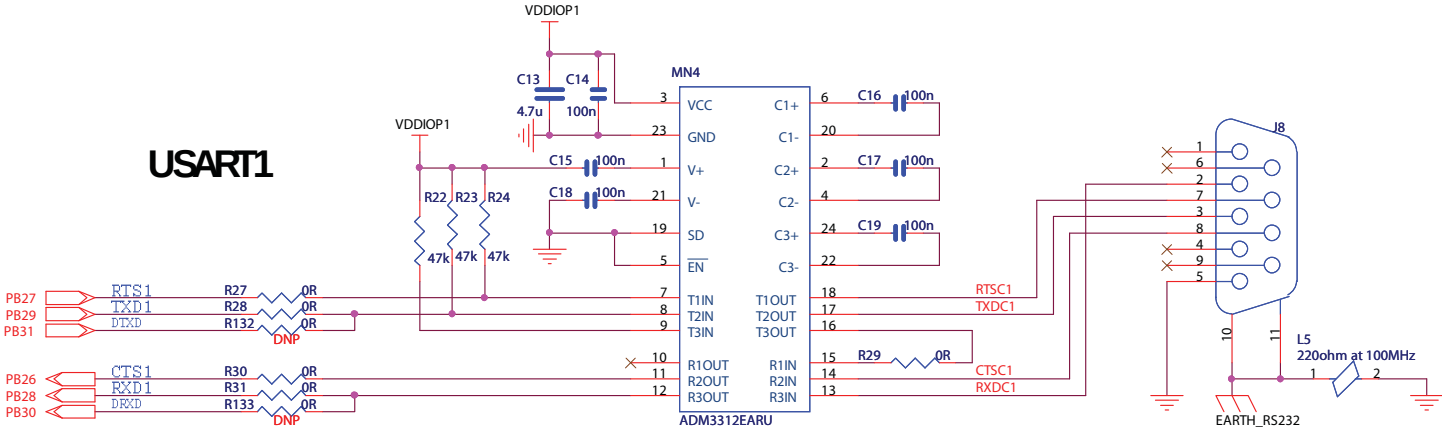
J-Link-OB-ATSAM3U4C comes with an additional hardware UART that is accessible from a host via CDC which allows terminal communication with the target device. This feature is enabled only if a certain port (CDC disabled, PA25, pin 24 on J-Link-OB-ATSAM3U4C) is NOT connected to ground (open).

- Jumper JP16 not fitted: CDC is enabled
- Jumper JP16 fitted : CDC is disabled

6.2.4 USART

The USART1 is used as a user serial communication port. This USART is buffered with an RS-232 Transceiver (TXD, RXD and handshake CTS/RTS control) and connected to the DB-9 male socket. The software must assign the appropriate PIO pins to enable the USART function.

Figure 6-7. USART1 Com Port



6.2.5 USB Ports

The SAMA5D3 series-MB features three USB communication ports:

Port A	Host High Speed (EHCI) and Full Speed (OHCI) multiplexed with USB Device High Speed Micro AB connector, J20
Port B	Host High Speed (EHCI) and Full Speed (OHCI) standard type A connector, J19 upper port
Port C	Host Full Speed (OHCI) only standard type A connector, J19 lower port

All three USB host ports are equipped with 500 mA high-side power switch for self-powered and bus-powered applications. The USB device port feature VBUS inserts detection function through the resistor ladder R138 and R139.

Refer to the embedded MPU product datasheet for detailed programming information. For datasheet reference numbers and titles, see Section 1.2 ”Applicable Documents” on page 1-1.

Figure 6-8. USB Port A

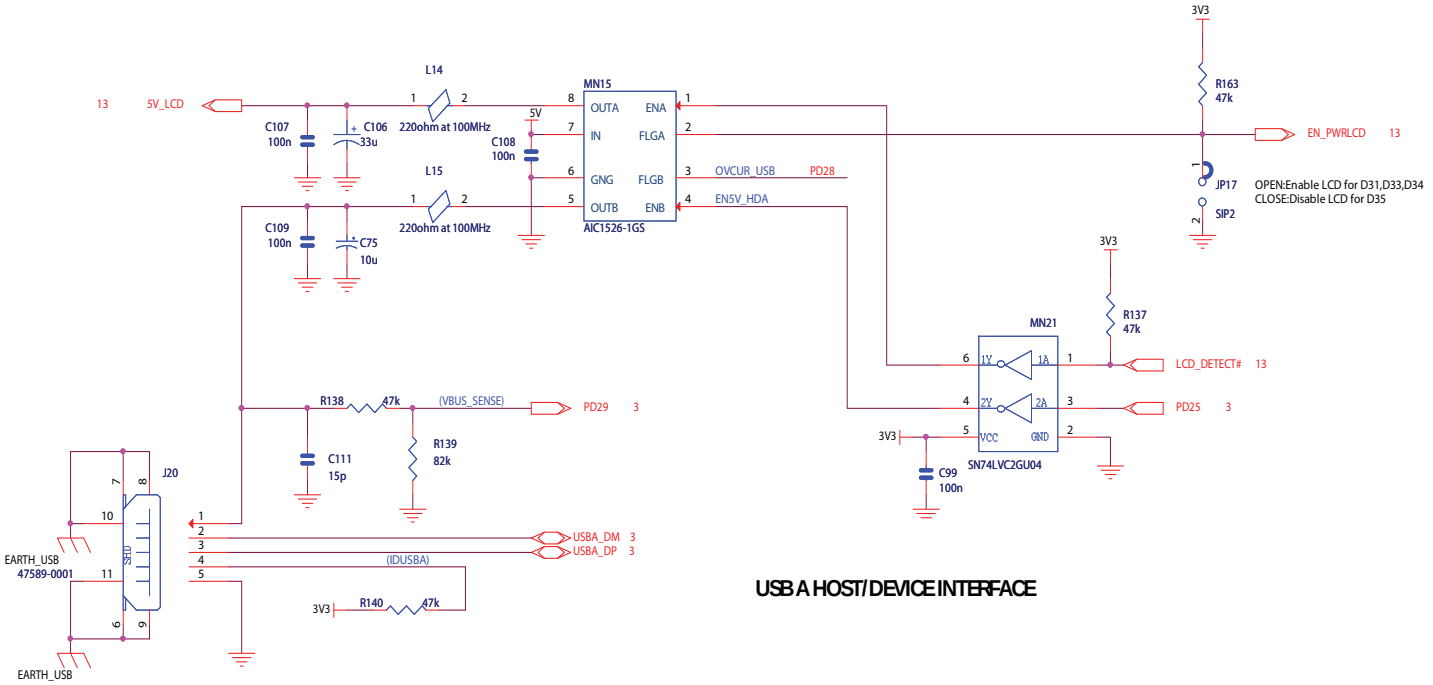
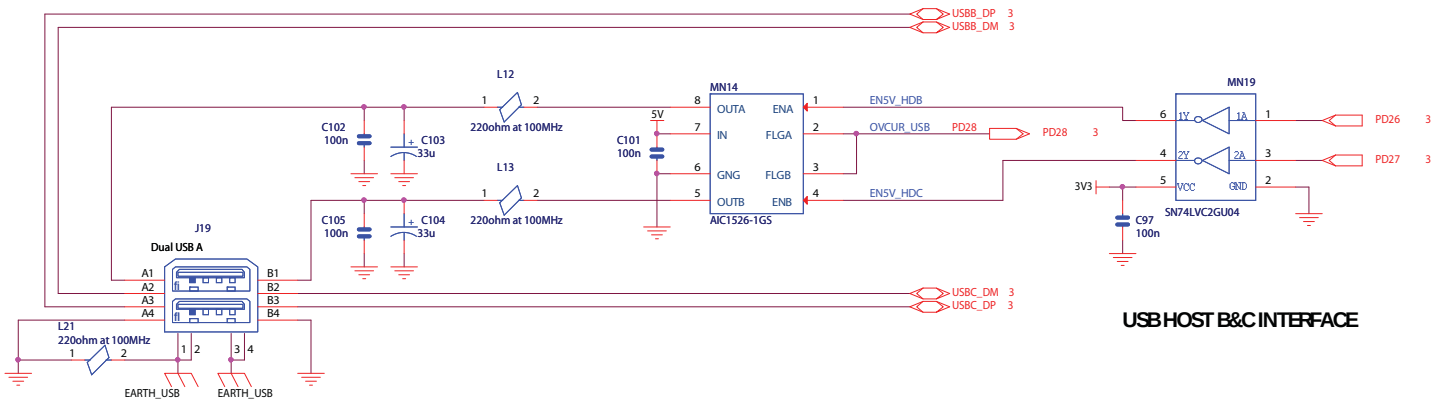


Figure 6-9. USB Ports B and C



6.2.6 Ethernet 10/100 (EMAC) Port

The main board contains a MICREL PHY device (KSZ8051) operating at 10/100 Mbps. The board supports MII and RMII interface modes.

The two independent PHY devices embedded on CM and MB boards are connected to independent RJ-45 connectors with built-in magnetic and status LEDs.

Additionally, for monitoring and control purposes, LED functionality is carried on the RJ45 connectors to indicate activity, link, and speed status information for the respective ports.

Figure 6-10. ETH0 Port

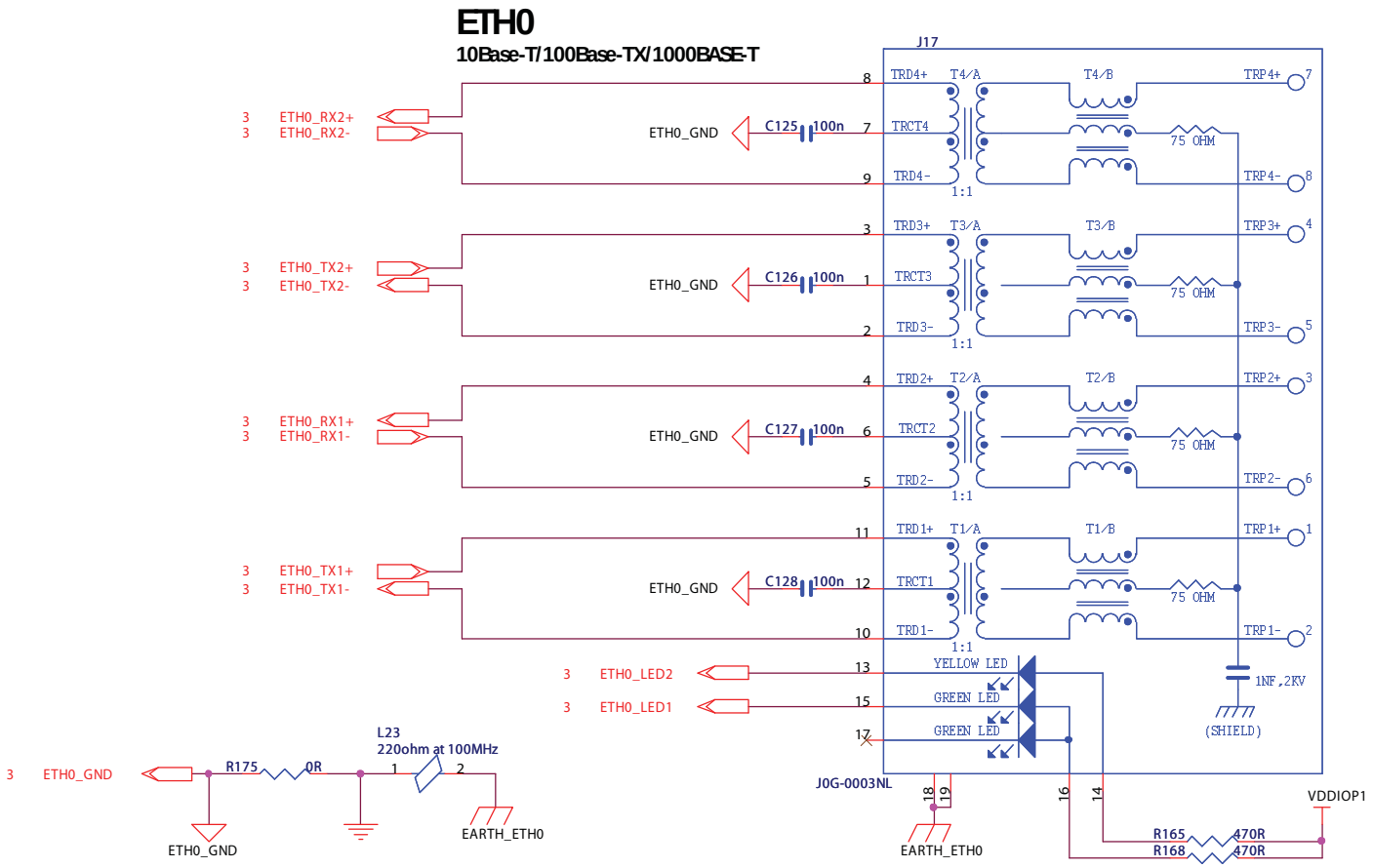
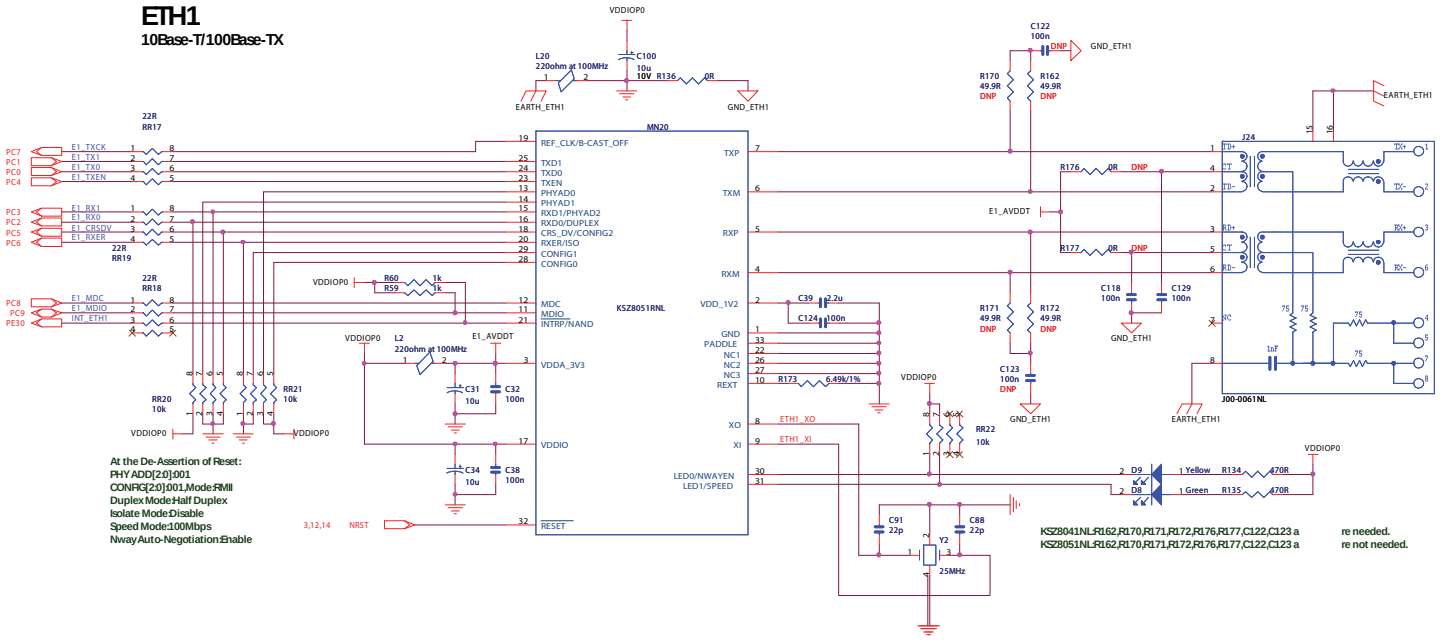


Figure 6-11. ETH1 Port



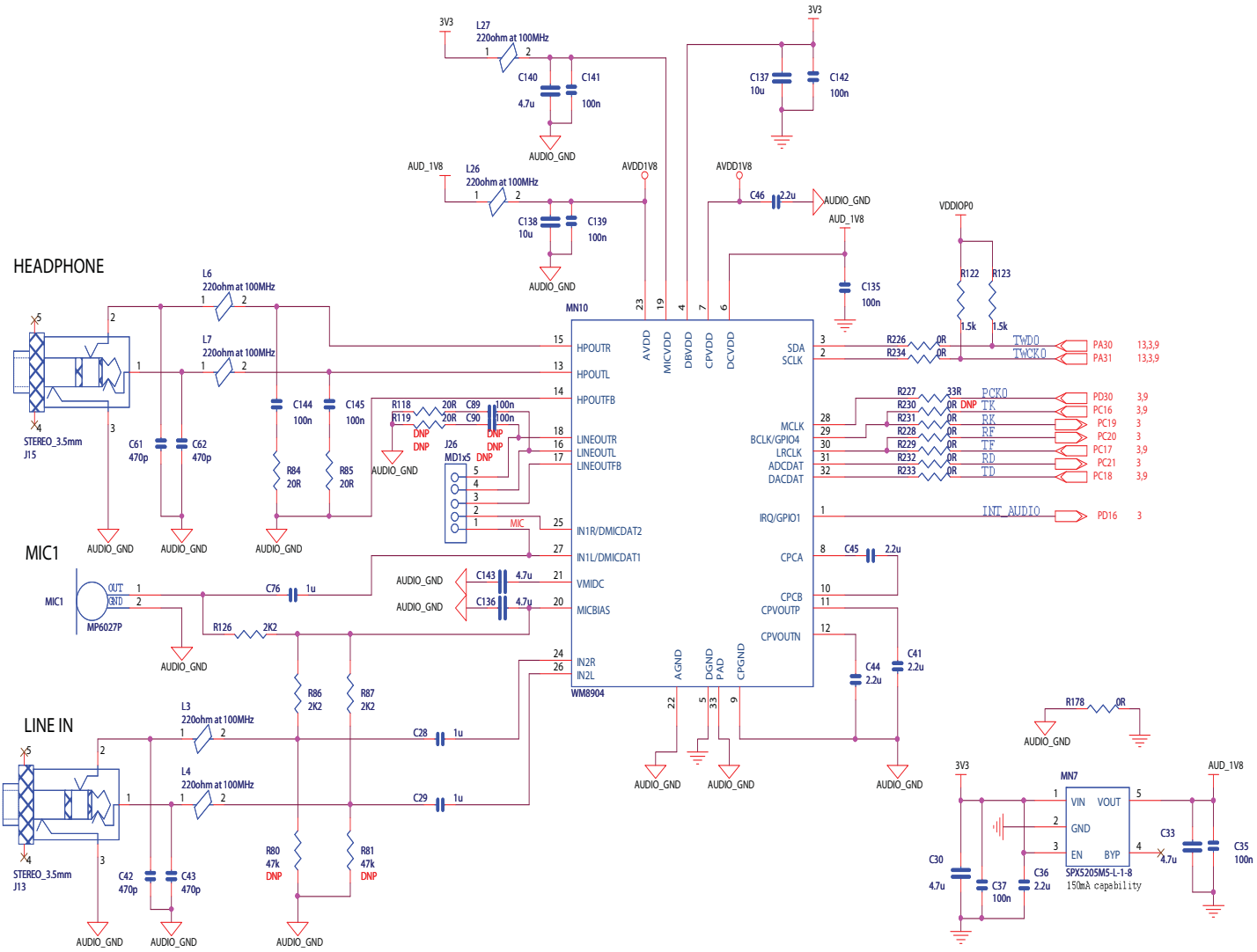
6.2.7 Audio

The Main Board includes a WM8904 CODEC for digital sound input and output. This interface includes audio jacks for micro input (J13) and headphone line output (J15).

This interface can be used to play and record audio. The WM8904 has left and right channel line inputs, a microphone input and an on-board microphone, a left and right headphone output. The microphone input and right/left headphone outputs are easily accessible via two 2.5 mm audio jacks on the J13 and J15 connectors. The Line In and Line Out connections are accessible via a 5-pin header (J26).

The SAMA5D3 series processor is configured as IIS slave mode to interface with the WM8904 CODEC.

Figure 6-12. Audio Interface



6.2.8 HDMI Transmitter Interface

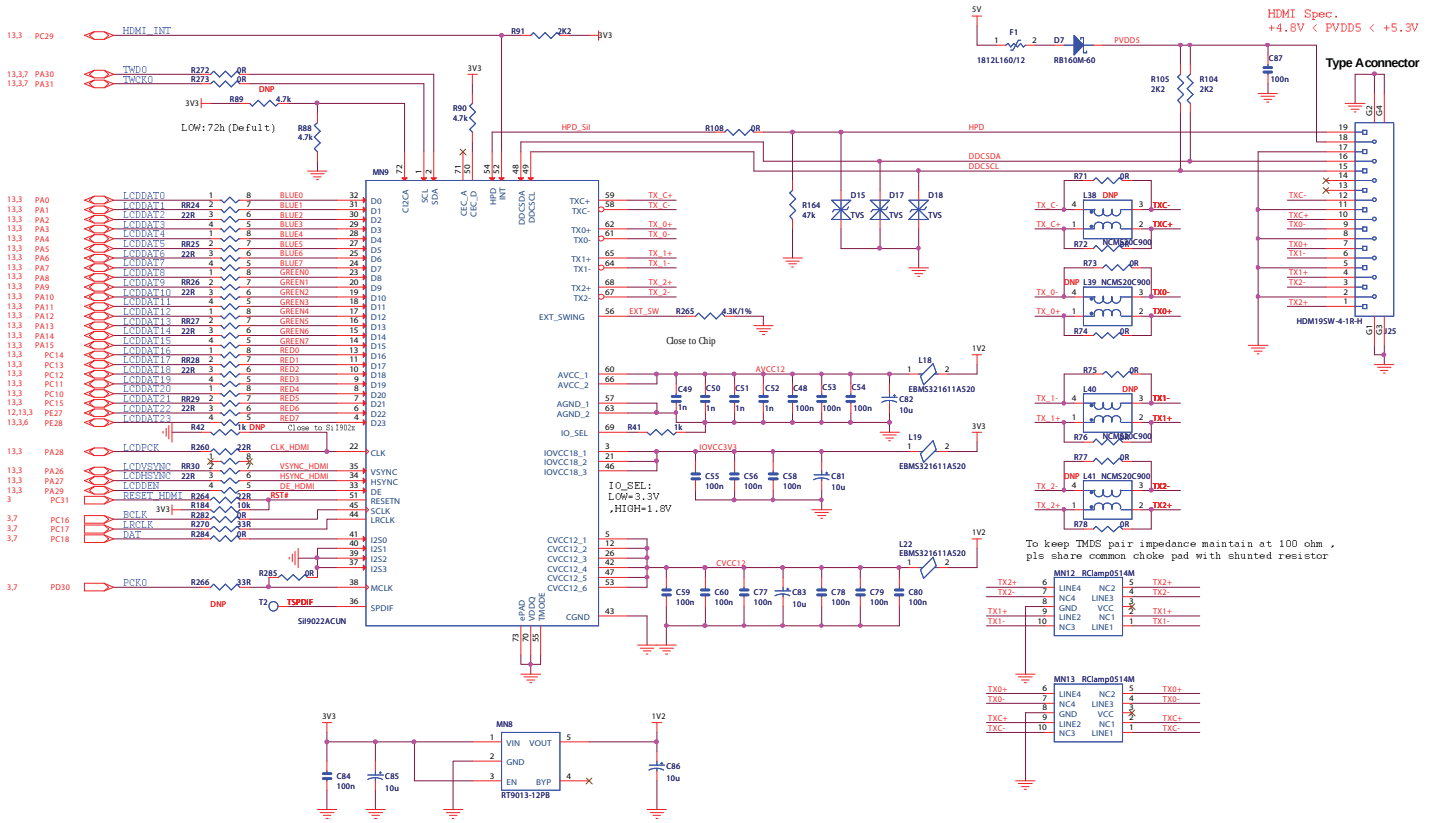
The Main Board (MB) is equipped with an HDMI transmitter interface.

The SiI9022/9024 HDMI Tx provides a complete solution for transmitting HDMI compliant digital audio/video. Specialized audio/video processing is available within the transmitter to easily and cost-effectively add HDMI capability to consumer electronics devices.

The user must use an HDMI cable to connect to a monitor. This cable is not provided with the SAMA5D3 series-EK. A standard HDMI cable can be used .

Note: Do not plug in the HDMI connector to a display with the Evaluation Kit powered on. Be certain that the EK Board is not powered, plug in the cable to the display and then power on the SAMA5D3 series-EK.

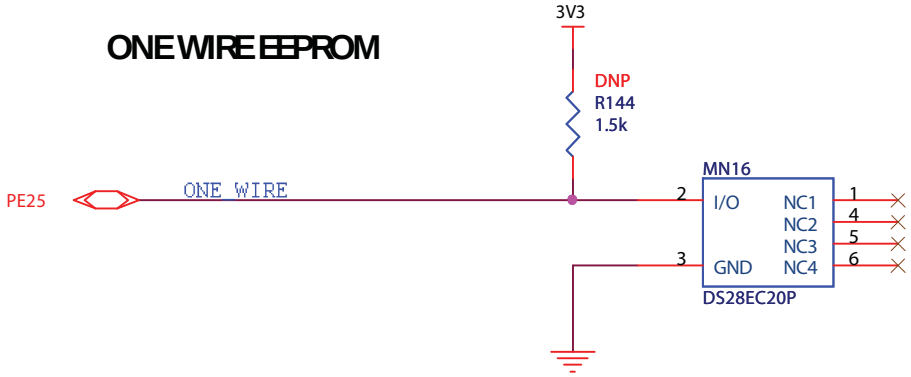
Figure 6-13. HDMI Interface



6.2.9 1-Wire EEPROM

The Main Board (MB) also features a 1-Wire device as "software identification label" to store information such as chip type, manufacture name, production date, etc.

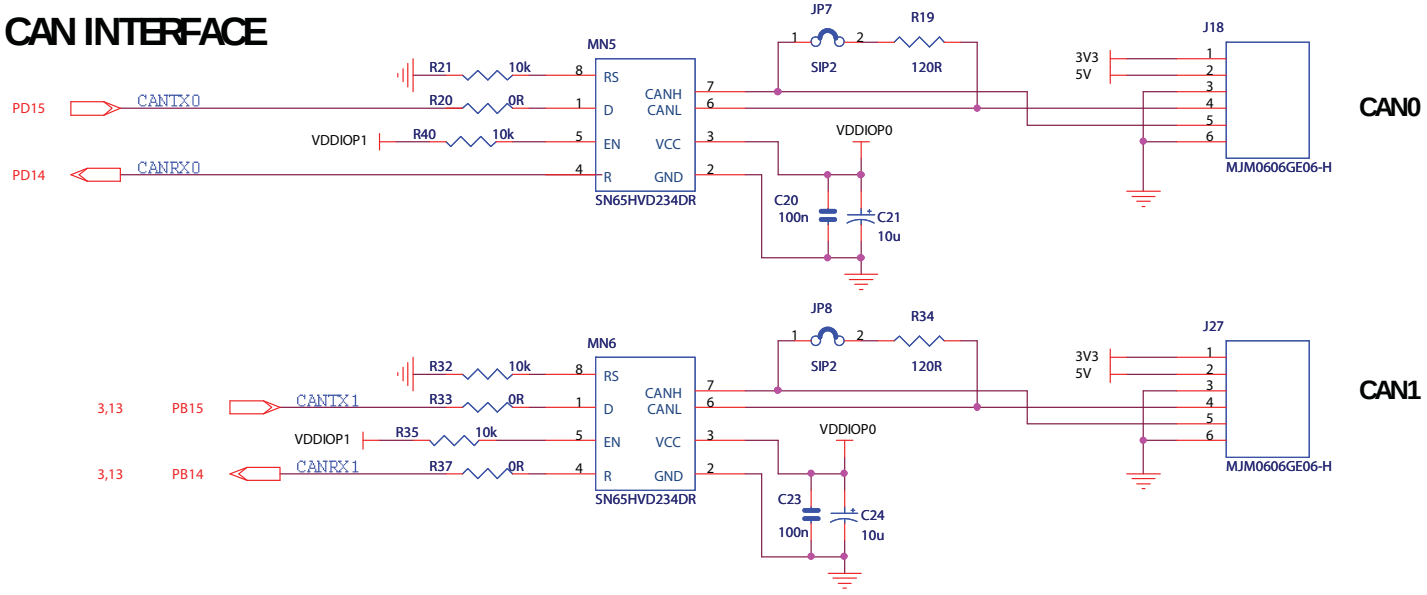
Figure 6-14. 1-Wire on MB



6.2.10 CAN Bus

The Main Board (MB) offers two CPU-controlled CAN (Controller Area Network) interfaces with transceivers available through connector J18, and two ports on connector J27.

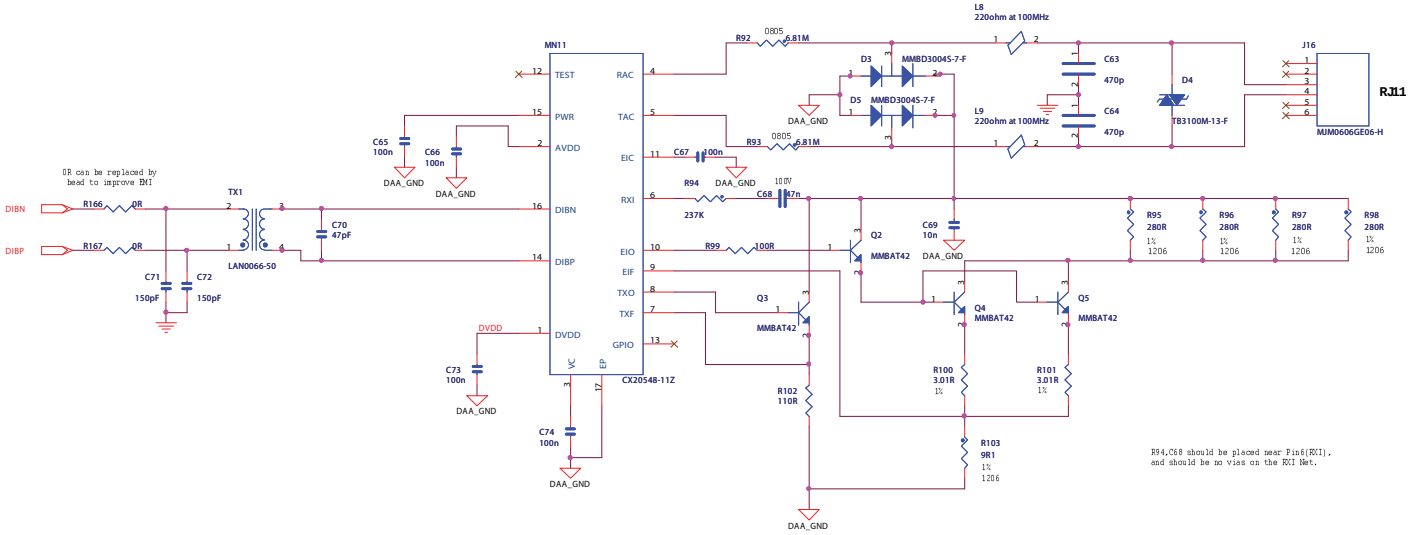
Figure 6-15. CAN on MB



6.2.11 Smart DAA

The SAMA5D3 series-MB features a smart DAA chip to drive an analog telephone line on RJ11 6P4C port (J16).

Figure 6-16. Smart DAA



6.2.12 SD/MMC Interface

SD/MMC is a standard Secure Digital / MultiMedia Card interface.

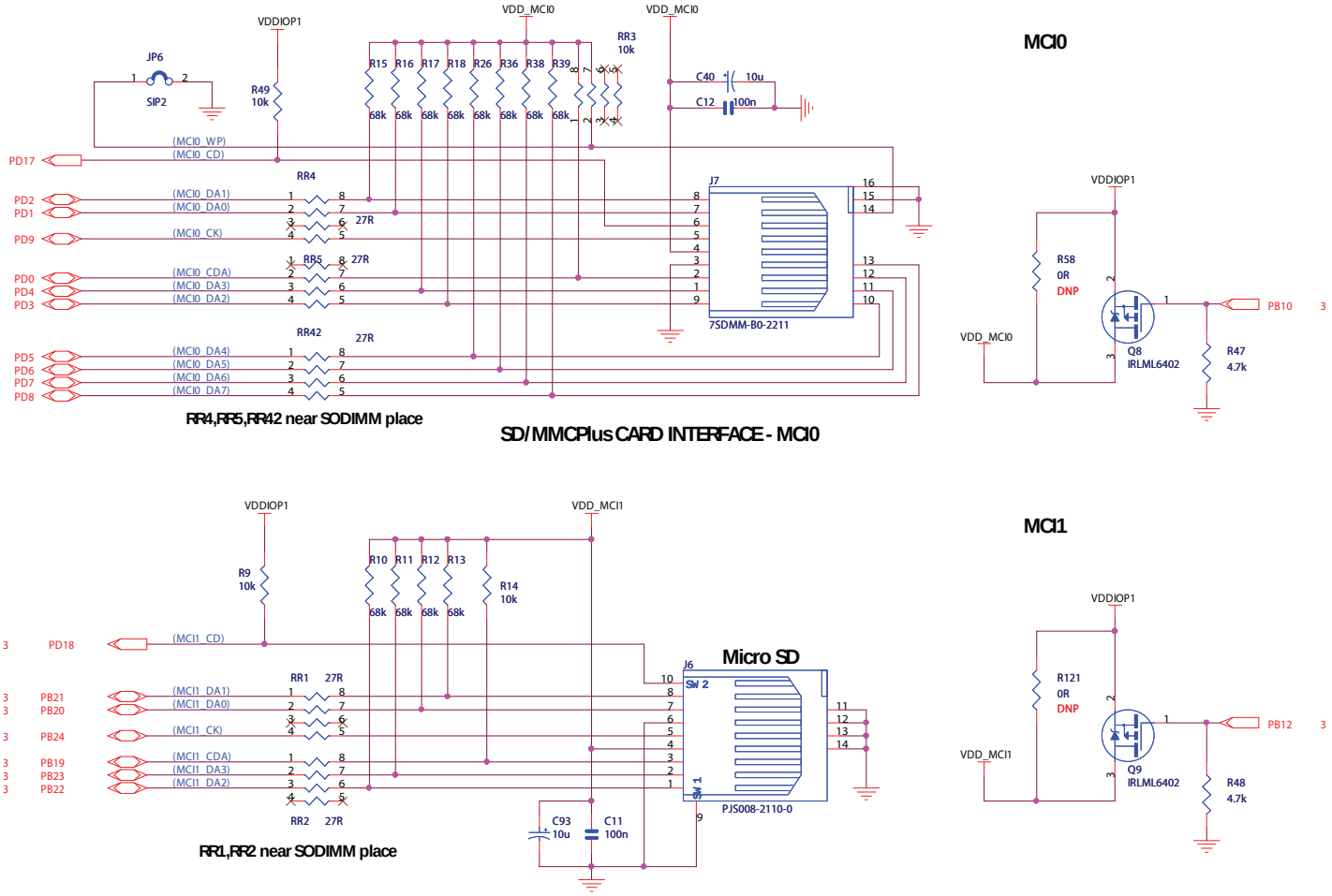
The Main Board (MB) has two high-speed Multimedia Card Interfaces (MCI).

- The first interface is used as a 8-bit interface (MCI0), connected to a SD/MMC card slot.
- The second interface is used as a 4-bit interface (MCI1), connected to a MicroSD card slot.

Each power line is on by default and is connected to a MOSFET controlled by a PIO to switch On or Off the SD card power.

Note: Please note that the power is connected to VCC, which is 3.3V.

Figure 6-17. SD/MMC Interface

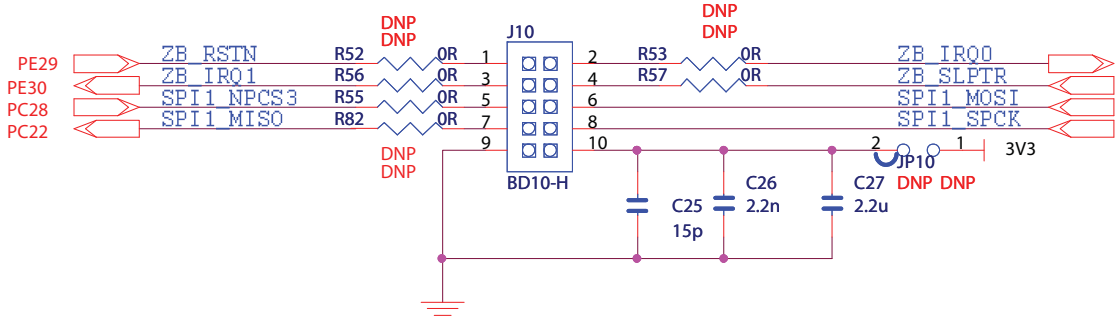


6.2.13 ZigBee

The Main Board (MB) has a 10-pin male connector for the Atmel RZ600 ZigBee module.

DNP 0 Ohm resistors have been implemented in series with the PIO lines that are used elsewhere in the design, thereby enabling their individual disconnection, should a conflict occur in user application.

Figure 6-18. ZigBee Interface



6.2.14 LED Indicators

MB board has one LED indicator as power LED.

6.2.15 Push Button Switches

- One Reset, board reset (BP1)
- One Wake up, push button to bring the processor out of low power mode (BP2)
- One User momentary Push Button
- One Disable CS Push Button

6.2.15.1 Reset

When pressed and released, causes a power-on reset of the SAMA5D3 series-EK (boards MB, CM and DM).

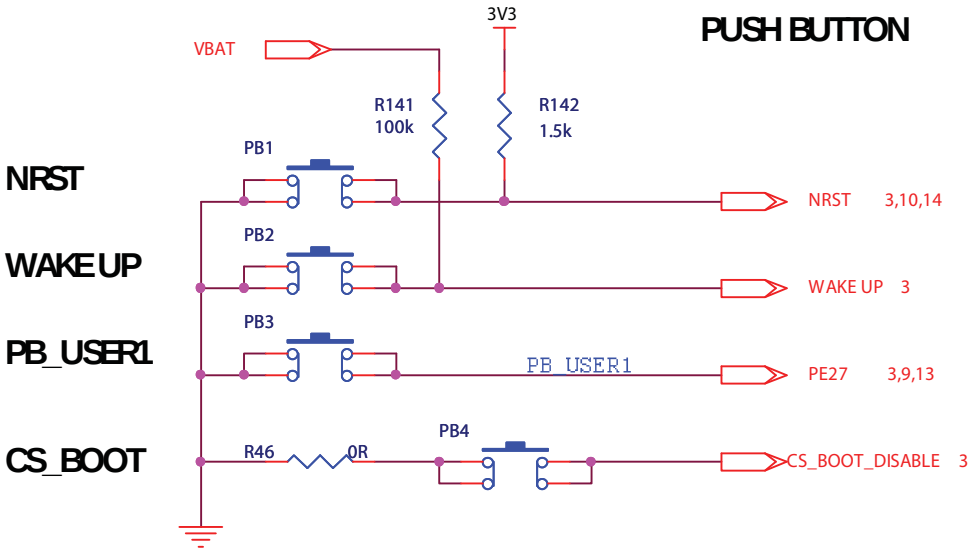
6.2.15.2 CS_BOOT Button

The CS_BOOT can be used to prevent the system to boot out of external memories (NandFlash, SPI flash). The purpose is mainly to execute the SAM-BA part of the ROM code.

2 methods can be used:

1. Press the CS_BOOT and power-cycle the board.
2. Press the CS_BOOT and then press the NRST button.

Figure 6-19. PushButton

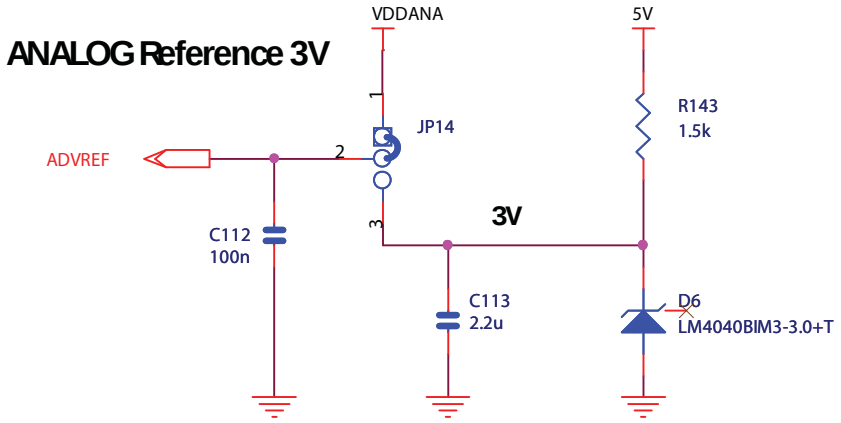


6.2.16 Analog Reference

The 3V voltage reference is based on a LM4040 (Precision Micropower Shunt Voltage Reference).

This ADVREF level can be set as 3V or 3.3V via the jumper JP14.

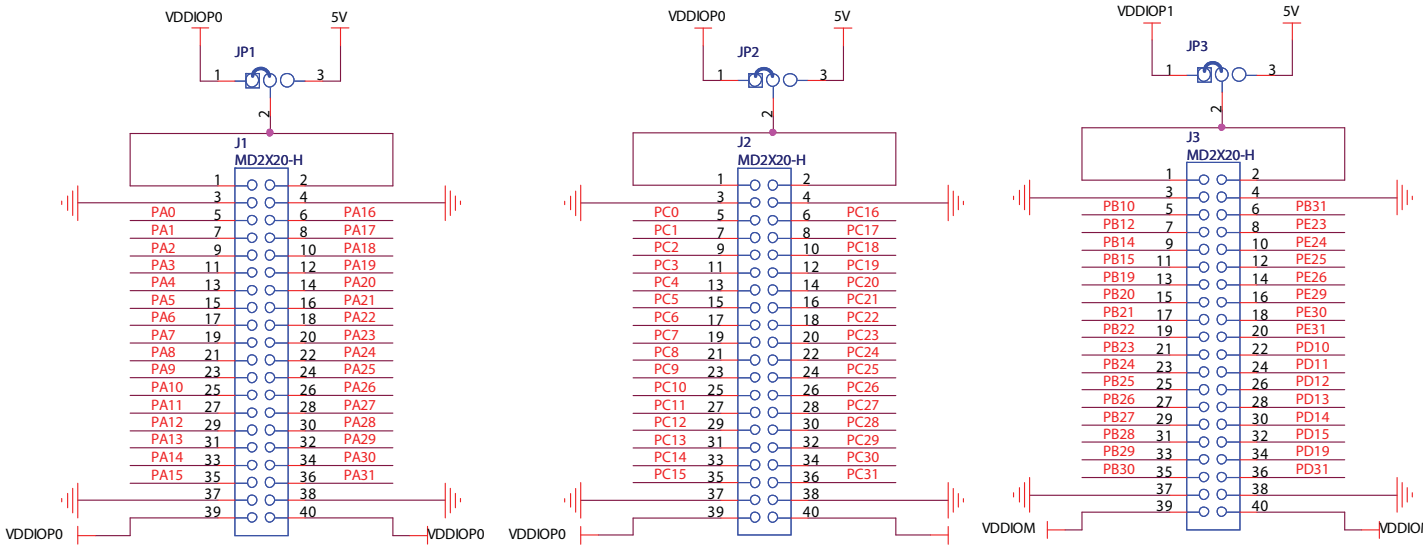
Figure 6-20. Analog Reference



6.2.17 Expansion Ports

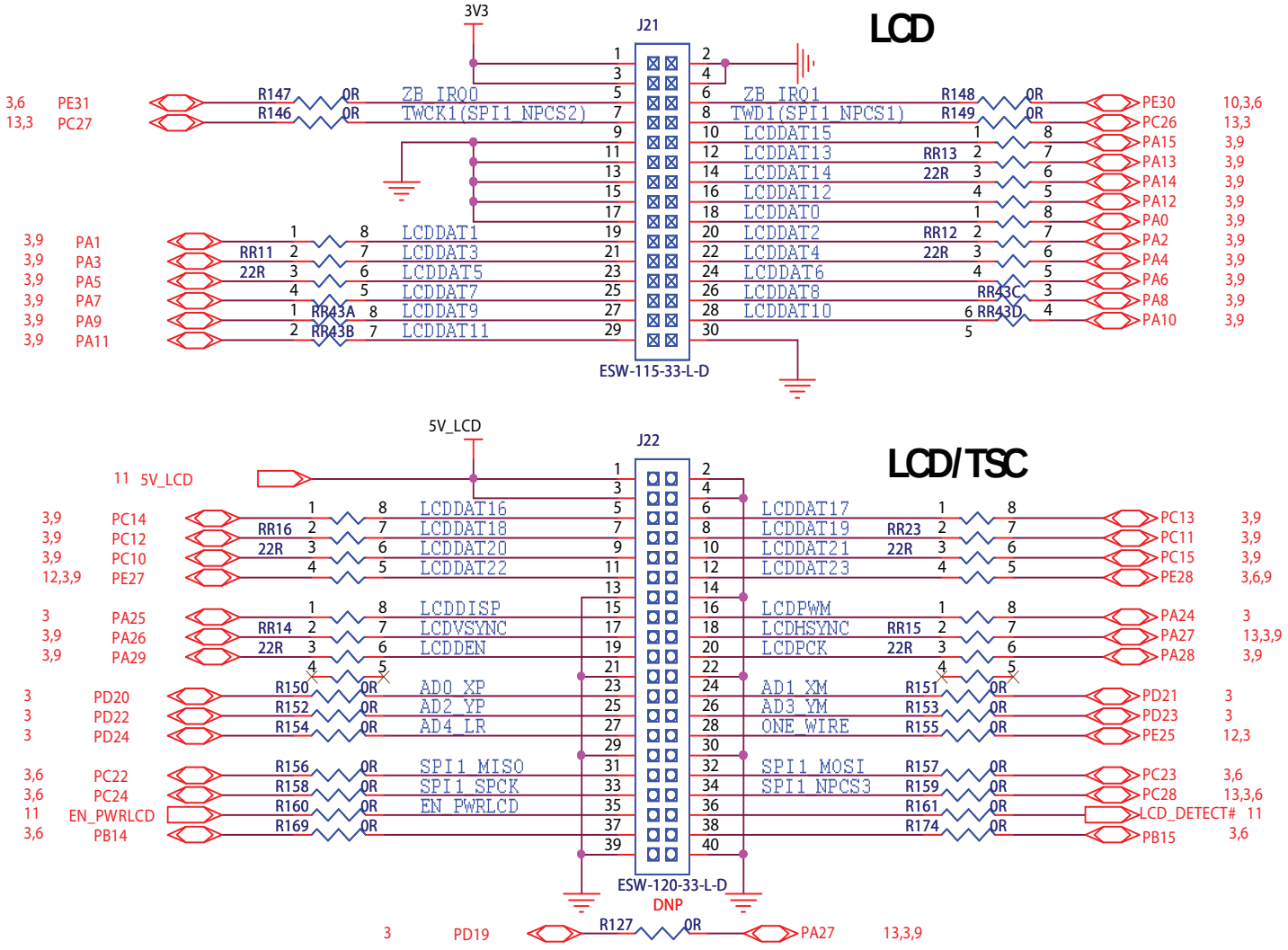
Three 40-pin headers (J1, J2, J3) are provided on the board to allow for the PIO connection of various expansion cards that could be developed by the users or other sources. Due to multiplexing, different signals can be provided on each pin.

Figure 6-21. I/O Expansion



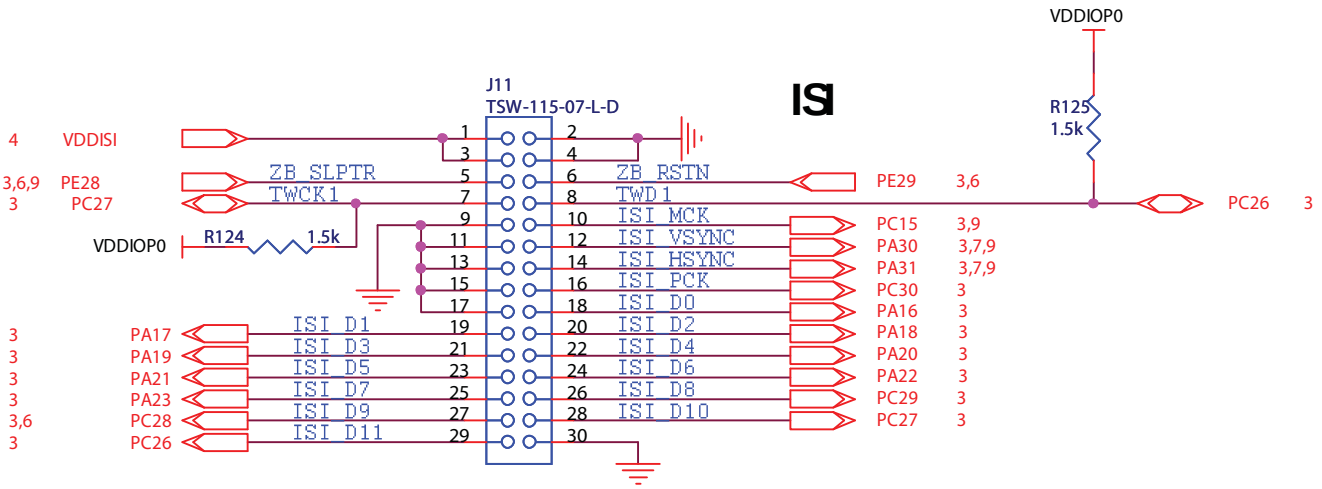
Two connectors (J21, J22) are provided on board to interface the optional LCD and touch screen DM board.

Figure 6-22. LCD Expansion



All I/Os of the SAMA5D3 series Image Sensor Interface (ISI) are routed to connectors J11.

Figure 6-23. ISI Expansion



6.3 Configuration

This section describes the PIO usage, the jumpers, the test points and the solder drops of a SAMA5D3 series-EK board.

Table 6-2. Jumpers and Solderdrops

Reference	Default	Function
JP1	1-2	VDDIOP0 or 5V selection for J1
JP2	1-2	VDDIOP0 or 5V selection for J2
JP3	1-2	VDDIOP0 or 5V selection for J3
JP4	CLOSE	Backup supply on/off
JP5	CLOSE	Force power on function
JP6	CLOSE	MCI0 write protect select
JP7	CLOSE	CAN0 diff termination select
JP8	CLOSE	CAN1 diff termination select
JP9	OPEN	Default boot on embedded ROM, close boot on external memory
JP10	OPEN	ZigBee power on/off select
JP11		
JP12		
JP13		
JP14	1-2	ADVREF input selection
JP15	OPEN	JTAG enable
JP16	OPEN	CDC enable
JP17	OPEN CLOSE	Enable LCD for D31, D33, D34 Disable LCD for D35
JP18	1-2	SAM3U powered by main 3V3

Table 6-3. Default Not Populated Parts

Page	Reference	Function
3	R6,R51,R50,R120	Optional PD10, PD11, PD12, PD13 from MB
5	R58	Optional for MCI0 power supply mode
	R121	Optional for MCI1 power supply mode
6	R52,R53,R55,R56,R57,R82,JP10	Optional ZigBee
	R132,R133	Debug or USART1 option
7	C89,C90,R118,R119,J26	Optional Audio Line out, MIC in
	R80,R81	Optional MIC level setting
	R230	Optional audio TK

Table 6-3. Default Not Populated Parts

Page	Reference	Function
9	L38,L39,L40,L41	Optional HDMI EMI filter
	R89	HDMI chip I2C address setting
	R266	Optional for I2S PCLK
	R42	Optional for LCD PCLK
10	R162,R170,R171,R172,R176,R177,C122,C123	Optional for KSZ8041NL
12	R144	Optional pull up for DS28EC20P
13	R127	Optional for ADC trigger
14	R79,R106,R107,R109,R113,R110,R112,R111,J9	Optional JTAG
	R54	SAM3U JTAG selection
	R63	5V Option
	D11,D12	USB ESD protect option
	R186	Main 3V3 optional for VCC_3V3_DEBUG

6.4 PIO Usage and Interface Connectors Details

6.4.1 Power supply

Figure 6-24. Power Supply Connector J4

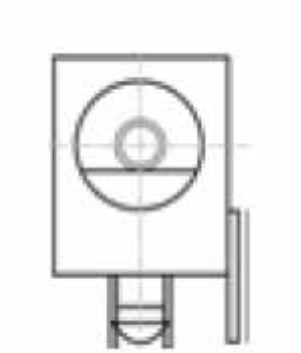


Table 6-4. Power Supply Connector J4 Signal Description

Pin	Mnemonic	Signal Description
1	Center	+5V
2		GND
3		Floating

6.4.2 JTAG/ICE Connector

Figure 6-25. JTAG J9

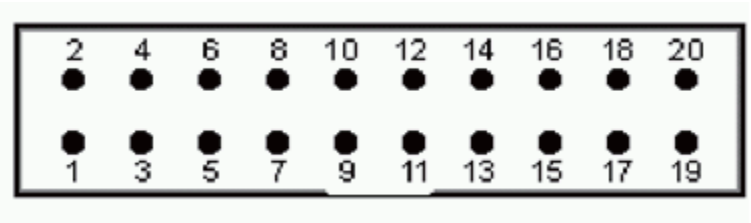


Table 6-5. JTAG/ICE Connector J9 Signal Descriptions

Pin	Mnemonic	Signal Description
1	VTref 3.3V power	This is the target reference voltage. It is used to check if the target has power, to create the logic-level reference for the input comparators, and to control the output logic levels to the target. It is normally fed from VDD on the target board and must not have a series resistor.
2	Vsupply 3.3V power	This pin is not connected in SAM-ICE. It is reserved for compatibility with other equipment. Connect to VDD or leave open in target system.
3	nTRST Target Reset - Active-low output signal that resets the target.	JTAG Reset. Output from SAM-ICE to the Reset signal on the target JTAG port. Typically connected to nTRST on the target CPU. This pin is normally pulled High on the target to avoid unintentional resets when there is no connection.
4	GND	Common ground
5	TDI Test Data Input - Serial data output line, sampled on the rising edge of the TCK signal.	JTAG data input of target CPU. It is recommended that this pin is pulled to a defined state on the target board. Typically connected to TDI on target CPU.
6	GND	Common ground
7	TMS Test Mode Select.	JTAG mode set input of target CPU. This pin should be pulled up on the target. Typically connected to TMS on target CPU. Output signal that sequences the target's JTAG state machine, sampled on the rising edge of the TCK signal.
8	GND	Common ground
9	TCK Test Clock - Output timing signal, for synchronizing test logic and control register access.	JTAG clock signal to target CPU. It is recommended that this pin is pulled to a defined state on the target board. Typically connected to TCK on target CPU.
10	GND	Common ground
11	RTCK - Input Return Test Clock signal from the target.	Some targets must synchronize the JTAG inputs to internal clocks. To assist in meeting this requirement, a returned and retimed TCK can be used to dynamically control the TCK rate. SAM-ICE supports adaptive clocking which waits for TCK changes to be echoed correctly before making further changes. Connect to RTCK if available, otherwise to GND.
12	GND	Common ground

Table 6-5. JTAG/ICE Connector J9 Signal Descriptions

Pin	Mnemonic	Signal Description
13	TDO JTAG Test Data Output - Serial data input from the target.	JTAG data output from target CPU. Typically connected to TDO on target CPU.
14	GND	Common ground
15	nSRST RESET	Active-low reset signal. Target CPU reset signal.
16	GND	Common ground
17	RFU	This pin is not connected in SAM-ICE.
18	GND	Common ground
19	RFU	This pin is not connected in SAM-ICE.
20	GND	Common ground

6.4.3 USB Type A Dual Port

Figure 6-26. USB Type A Dual Port J19

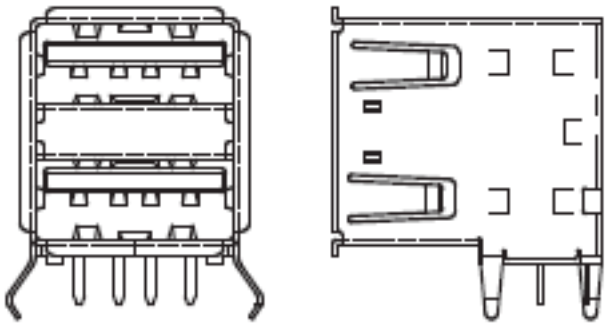


Table 6-6. USB Type A Dual Port J19 Signal Descriptions

Pin	Mnemonic	PIO	Signal Description
A1	Vbus - USB_A		5V power
A2	DM - USB_A		Data minus
A3	DP - USB_A		Data plus
A4	GND		Common ground
B1	Vbus - USB_A		5V power
B2	DM - USB_A		Data minus
B3	DP - USB_A		Data plus
B4	GND		Common ground
Mechanical pins			Shield

6.4.4 USB MicroAB

Figure 6-27. USB Host/Device MicroAB Connector J20

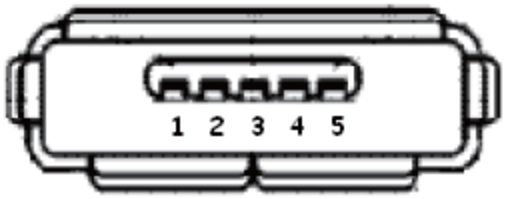


Table 6-7. USB Host/Device Micro AB Connector J20 Signal Descriptions

Pin	Mnemonic	PIO	Signal Description
1	Vbus		5V power
2	DM		Data minus
3	DP		Data plus
4	ID		On the Go identification
5	GND		Common ground

6.4.5 JTAG OB USB MicroAB

Figure 6-28. USB JTAG OB MicroAB connector J14

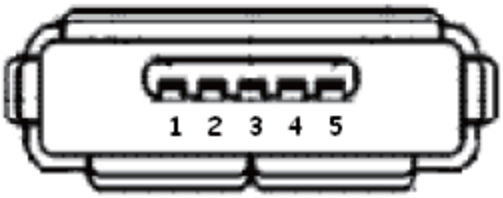


Table 6-8. USB JTAG OB MicroAB connector J14 Signal Descriptions

Pin	Mnemonic	PIO	Signal description
1	Vbus		5V power
2	DM		Data minus
3	DP		Data plus
4	ID		On the Go Identification
5	GND		Common ground

6.4.6 HDMI Connector

Figure 6-29. HDMI Female Type A Connector J25

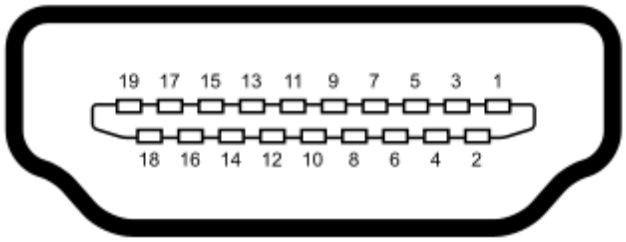


Table 6-9. HDMI Type A Female Connector J25

LCD	Pin Num		LCD
TMDS Data 2+	1	2	TMDS Data 2 Shield
TMDS Data 2-	3	4	TMDS Data 1+
TMDS Data 1 Shield	5	6	TMDS Data 1-
TMDS Data 0+	7	8	TMDS Data 0 Shield
TMDS Data 0-	9	10	TMDS Clock +
TMDS Clock Shield	11	12	TMDS Clock -
NC	13	14	NC
SCL	15	16	SDA
GND	17	18	+5V
Hot Plus Detect	19	20	

6.4.7 RS232 Connector with RTS/CTS Handshake Support

Figure 6-30. USART1 Connector J8

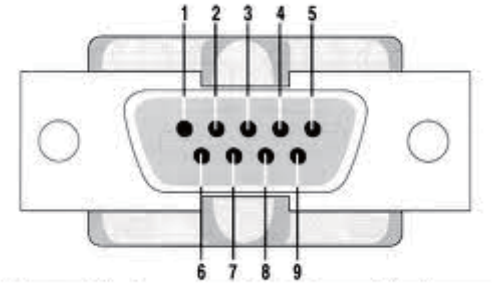


Table 6-10. USART Connector J8 Signal Descriptions

Pin	Mnemonic	PIO	Signal Description
1, 4, 6, 9			No connection
2	RXD (Received Data)	PB28	RS232 serial data output signal
3	TXD (Transmitted Data)	PB29	RS232 serial data input signal
5	GND		Common ground
7	RTS (Request To Send)	PB27	Active-positive RS232 input signal
8	CTS (Clear To Send)	PB26	Active-positive RS232 output signal
Mechanical pins			Shield

6.4.8 DAA RJ11 Socket (6P4C)

Figure 6-31. DAA RJ11 Socket J16

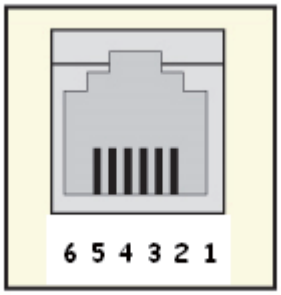


Table 6-11. DAA RJ11 Socket J16 Signal Descriptions

Pin	Mnemonic	Signal Description
1, 2, 5, 6		No connection
3	RAC	RING side of ordinary telephone line
4	TAC	TIP side of ordinary telephone line

6.4.9 CAN RJ12 Socket (6P6C)

Figure 6-32. CAN RJ12 Socket J18, J27

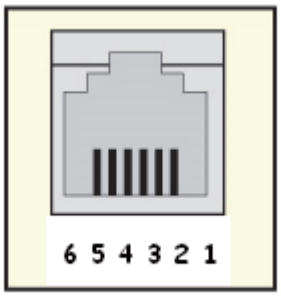


Table 6-12. CAN RJ12 Socket Signal Descriptions

Pin	Mnemonic	Signal Description
1	3V3	Power pin
2	5V	Power pin
4	CANL	CAN bus differential pair
5	CANH	CAN bus differential pair
3, 6	GND	Common ground

6.4.10 SD/MMC Plus MCI0

Figure 6-33. SD Socket J7

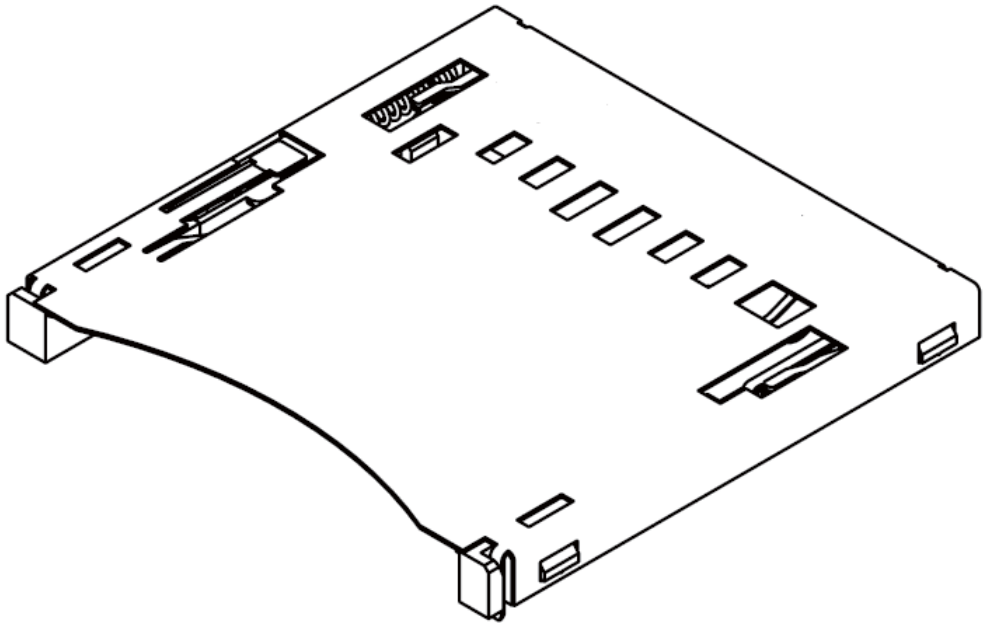


Table 6-13. MicroSD Socket J7 Signal Descriptions

Pin	Mnemonic	PIO	Signal Description
1	DAT3	PD4	Data bit
2	CMD	PD0	Command line
3	VSS		Command line
4	VCC		Supply voltage 3.3V
5	CLK	PD9	Clock / command line
6	CD	PD17	Card detect
7	DAT0	PD1	Data bit
8	DAT1	PD2	Data bit
9	DAT2	PD3	Data bit
10	DAT4	PD5	Data bit
11	DAT5	PD6	Data bit
12	DAT6	PD7	Data bit
13	DAT7	PD8	Data bit
14	WP	JP6	Protect
15		VSS	Common ground
16		VSS	Common ground

6.4.11 MicroSD MCI1

Figure 6-34. MicroSD Socket J6

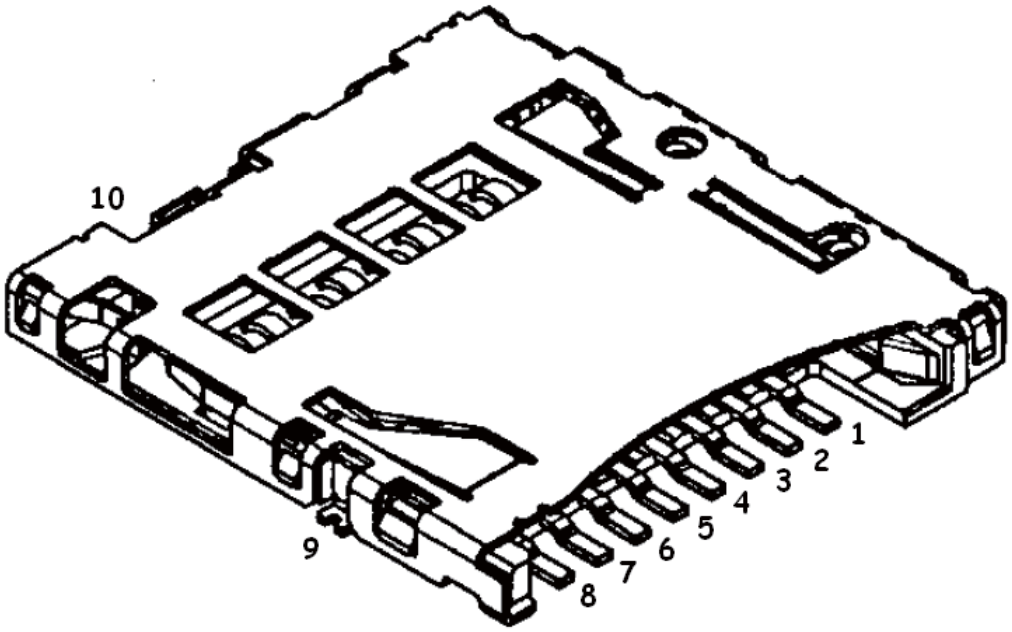
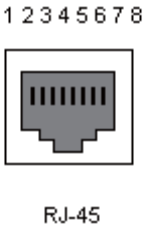


Table 6-14. MicroSD Socket J6 Signal Descriptions

Pin	Mnemonic	PIO	Signal Description
1	DAT2	PB22	Data bit 2
2	CD/DAT3	PB23	Card detect / data bit 3
3	CMD	PB19	Command line
4	VCC		Supply voltage 3.3V
5	CLK	PB24	Clock / command line
6	VSS		Common ground
7	DAT0	PB20	Data bit 0
8	DAT1	PB21	Data bit 1
9	SW1		Not used, grounded
10	CARD DETECT	PD18	Card detect

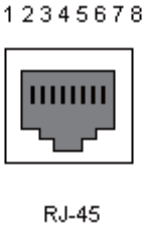
6.4.12 Gigabit Ethernet ETH0 RJ45 Socket J17

Figure 6-35. Gigabit Ethernet RJ45 Socket J17



6.4.13 Ethernet ETH1 RJ45 Socket J24

Figure 6-36. Ethernet RJ45 Socket J24



6.4.14 ZigBee Socket J10

Figure 6-37. ZigBee Socket J10

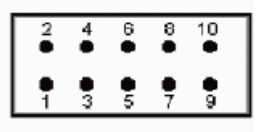


Table 6-15. ZigBee Socket J10 Signal Descriptions

Function	Signal Name	Port	Pin	Pin	Port	Signal Name	Function	Option on Misc. Port Set by OR or Solder Shunts
Reset	/RST		1	2		Misc.	EEPROM for MAC address, cap array settings and serial number TST: test mode activation CLKM: RF chip clock output	
Interrupt Request	IRQ		3	4		SLP_TR	SLP_TR	
SPI chip select	/SEL		5	6		MOSI	SPI MOSI	
SPI MISO	MISO		7	8		SCLK	SPI CLK	
Power Supply	GND	GND	9	10	VCC	VCC	VCC	Voltage range: 1.8V to 5.5V, regulated to 3.3V

6.4.15 LCD Socket J21

Figure 6-38. LCD Socket J21

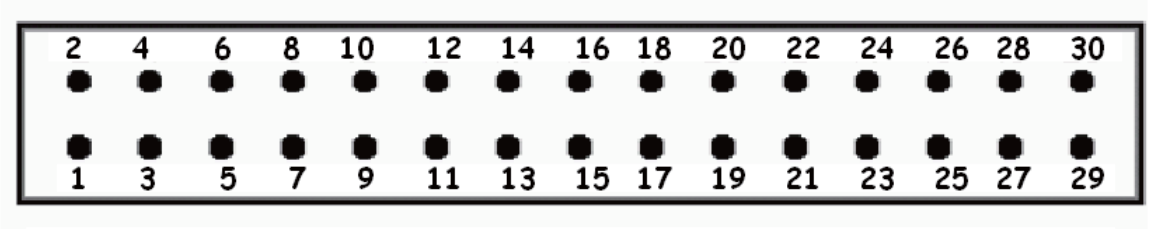


Table 6-16. LCD Socket J21 HE10 Female LCD 2*15p

LCD	Pin Num		LCD
VDD3V3	1	2	GND
VDD3V3	3	4	GND
ZB_IRQ0	5	6	ZB_IRQ1
TWCK1	7	8	TWD1
GND	9	10	LCDDAT15
GND	11	12	LCDDAT13
GND	13	14	LCDDAT14
GND	15	16	LCDDAT12
GND	17	18	LCDDAT0
LCDDAT1	19	20	LCDDAT2
LCDDAT3	21	22	LCDDAT4
LCDDAT5	23	24	LCDDAT6
LCDDAT7	25	26	LCDDAT8
LCDDAT9	27	28	LCDDAT10
LCDDAT11	29	30	GND

6.4.16 LCD/TSC Socket J22

Figure 6-39. LCD/TSC Socket J22

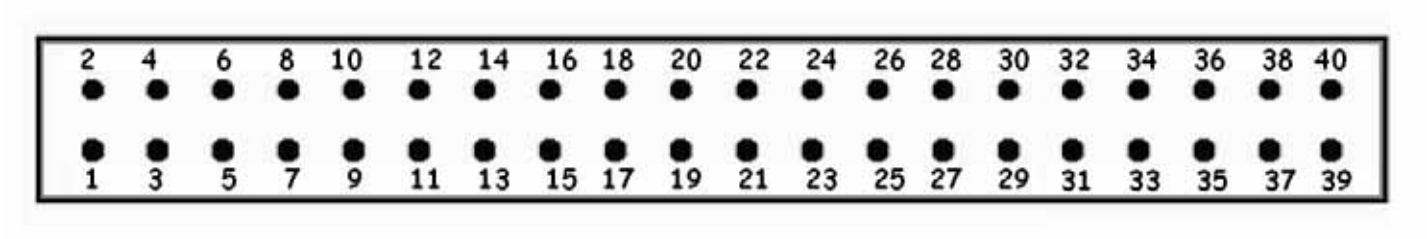


Table 6-17. LCD/TSC Socket J22 HE10 Female LCD/TSC/QT 2*20p

LCD		Pin Num			LCD
5V	5V_LCD	1	2	GND	GND
5V	5V_LCD	3	4	GND	GND
LCDDAT16		5	6		LCDDAT17
LCDDAT18		7	8		LCDDAT19
LCDDAT20		9	10		LCDDAT21
LCDDAT22		11	12		LCDDAT23
GND	GND	13	14	GND	GND
LCDDISP		15	16		LCDPWM
LCDCSYNC		17	18		LCDHSYNC
LCDDEN		19	20		LCDPCK
GND	GND	21	22	GND	GND
AD0_XP	TSC	23	24	TSC	AD1_XM
AD2_YP	TSC	25	26	TSC	AD3_YM
AD4_LR	TSC	27	28		ONE_WIRE
GND1	GND	29	30	GND	GND
SPI1_MISO		31	32		SPI1_MOSI
SPI1_SPCK		33	34		SPI1_NPCS3
EN_PWRLCD		35	36	LCD_DETECT	LCD_DETECT#
	PB14	37	38	PB15	
GND	GND	39	40	GND	GND

6.4.17 ISI Socket J11

Figure 6-40. ISI Socket J11

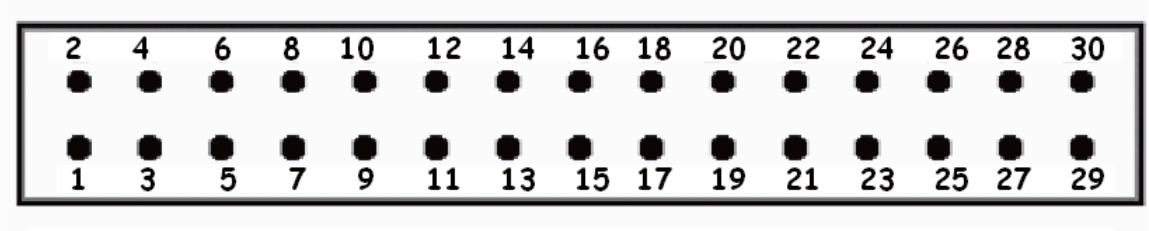


Table 6-18. ISI Socket J11 HE10 Female ISI 2*15p

ISI	Pin Num		ISI
VDDISI	1	2	GND
VDDISI	3	4	GND
ZB_SLPTR	5	6	ZB_RST
TWCK1	7	8	TWD1
GND	9	10	ISI_MCK
GND	11	12	ISI_VSYNC
GND	13	14	ISDI_HSYNC
GND	15	16	ISI_PCK
GND	17	18	ISI_D0
ISI_D1	19	20	ISI_D2
ISI_D3	21	22	ISI_D4
ISI_D5	23	24	ISI_D6
ISI_D7	25	26	ISI_D8
ISI_D9	27	28	ISI_D10
ISI_D11	29	30	GND

6.4.18 PIO Usage

Table 6-19. PIO A Pin Assignment and Signal Description

Power Rail	Signal	Signal	Signal	Signal	SAMA5-CM	SAMA5-MB
VDDIOP0	PA0	LCDDAT0	PIO	PU		LCDDAT0
VDDIOP0	PA1	LCDDAT1	PIO	PU		LCDDAT1
VDDIOP0	PA2	LCDDAT2	PIO	PU		LCDDAT2
VDDIOP0	PA3	LCDDAT3	PIO	PU		LCDDAT3
VDDIOP0	PA4	LCDDAT4	PIO	PU		LCDDAT4
VDDIOP0	PA5	LCDDAT5	PIO	PU		LCDDAT5
VDDIOP0	PA6	LCDDAT6	PIO	PU		LCDDAT6
VDDIOP0	PA7	LCDDAT7	PIO	PU		LCDDAT7
VDDIOP0	PA8	LCDDAT8	PIO	PU		LCDDAT8
VDDIOP0	PA9	LCDDAT9	PIO	PU		LCDDAT9
VDDIOP0	PA10	LCDDAT10	PIO	PU		LCDDAT10
VDDIOP0	PA11	LCDDAT11	PIO	PU		LCDDAT11
VDDIOP0	PA12	LCDDAT12	PIO	PU		LCDDAT12
VDDIOP0	PA13	LCDDAT13	PIO	PU		LCDDAT13
VDDIOP0	PA14	LCDDAT14	PIO	PU		LCDDAT14
VDDIOP0	PA15	LCDDAT15	PIO	PU		LCDDAT15
VDDIOP0	PA16	LCDDAT16	ISI_D0	PIO		ISI_D0
VDDIOP0	PA17	LCDDAT17	ISI_D1	PIO		ISI_D1
VDDIOP0	PA18	LCDDAT18	TWD2	ISI_D2		ISI_D2
VDDIOP0	PA19	LCDDAT19	TWCK2	ISI_D3		ISI_D3
VDDIOP0	PA20	LCDDAT20	PWMH0	ISI_D4		ISI_D4
VDDIOP0	PA21	LCDDAT21	PWML0	ISI_D5		ISI_D5
VDDIOP0	PA22	LCDDAT22	PWMH1	ISI_D6		ISI_D6
VDDIOP0	PA23	LCDDAT23	PWML1	ISI_D7		ISI_D7
VDDIOP0	PA24	LCDPWM	PIO	PU		LCDPWM
VDDIOP0	PA25	LCDDISP	PIO	PU		LCDDISP
VDDIOP0	PA26	LCDVSYNC	PIO	PU		LCDVSYNC
VDDIOP0	PA27	LCDHSYNC	PIO	PU		LCDHSYNC
VDDIOP0	PA28	LCDPCK	PIO	PU		LCDPCK
VDDIOP0	PA29	LCDDEN	PIO	PU		LCDDEN
VDDIOP0	PA30	TWD0	URXD1	ISI_VSYNC		ISI_VSYNC
VDDIOP0	PA31	TWCK0	UTXD1	ISI_HSYNC		ISI_HSYNC

Table 6-20. PIO B Pin Assignment and Signal Description

Power Rail	Signal	Signal	Signal	Signal	SAMA5-CM	SAMA5-MB
VDDIOP1	PB0	GTX0	PWMH0	PIO	GETH CM	
VDDIOP1	PB1	GTX1	PWML0	PIO	GETH CM	
VDDIOP1	PB2	GTX2	TK1	PIO	GETH CM	
VDDIOP1	PB3	GTX3	TF1	PIO	GETH CM	
VDDIOP1	PB4	GRX0	PWMH1	PIO	GETH CM	
VDDIOP1	PB5	GRX1	PWML1	PIO	GETH CM	
VDDIOP1	PB6	GRX2	TD1	PIO	GETH CM	
VDDIOP1	PB7	GRX3	RK1	PIO	GETH CM	
VDDIOP1	PB8	GTXCK	PWMH2	PIO	GETH CM	
VDDIOP1	PB9	GTXEN	PWML2	PIO	GETH CM	
VDDIOP1	PB10	GTXER	RF1	PIO		PWR_MCI0
VDDIOP1	PB11	GRXCK	RD1	PIO	GETH CM	
VDDIOP1	PB12	GRXDV	PWMH3	PIO		PWR_MCI1
VDDIOP1	PB13	GRXER	PWML3	PIO	GETH CM	RX_DV (KSZ9021)
VDDIOP1	PB14	GCRS	CANRX1	PIO		CANRX1
VDDIOP1	PB15	GCOL	CANTX1	PIO		CANTX1
VDDIOP1	PB16	GMDC	PIO	PU	GETH CM	
VDDIOP1	PB17	GMDIO	PIO	PU	GETH CM	
VDDIOP1	PB18	G125CK	PIO	PU	GETH CM	
VDDIOP1	PB19	MCI1_CDA	GTX4	PIO		MCI1_CDA
VDDIOP1	PB20	MCI1_DA0	GTX5	PIO		MCI1_DA0
VDDIOP1	PB21	MCI1_DA1	GTX6	PIO		MCI1_DA1
VDDIOP1	PB22	MCI1_DA2	GTX7	PIO		MCI1_DA2
VDDIOP1	PB23	MCI1_DA3	GRX4	PIO		MCI1_DA3
VDDIOP1	PB24	MCI1_CK	GRX5	PIO		MCI1_CK
VDDIOP1	PB25	SCK1	GRX6	PIO	INT_GETH0	
VDDIOP1	PB26	CTS1	GRX7	PIO		CTS1
VDDIOP1	PB27	RTS1	PWMH1	PIO		RTS1
VDDIOP1	PB28	RXD1	PIO	PU		RXD1
VDDIOP1	PB29	TXD1	PIO	PU		TXD1
VDDIOP0	PB30	DRXD	PIO	PU		DRXD (DBGU)
VDDIOP0	PB31	DTXD	PIO	PU		DTXD (DBGU)

Table 6-21. PIO C Pin Assignment and Signal Description

Power Rail	Signal	Signal	Signal	Signal	SAMA5-MB	
VDDIOP0	PC0	ETX0	TIOA3	PIO	ETX0	
VDDIOP0	PC1	ETX1	TIOB3	PIO	ETX1	
VDDIOP0	PC2	ERX0	TCLK3	PIO	ERX0	
VDDIOP0	PC3	ERX1	TIOA4	PIO	ERX1	
VDDIOP0	PC4	ETXEN	TIOB4	PIO	ETXEN	
VDDIOP0	PC5	ECRSDV	TCLK4	PIO	ECRSDV	
VDDIOP0	PC6	ERXER	TIOA5	PIO	ERXER	
VDDIOP0	PC7	EREFCK	TIOB5	PIO	EREFCK	
VDDIOP0	PC8	EMDC	TCLK5	PIO	EMDC	
VDDIOP0	PC9	EMDIO	PIO	PU	EMDIO	
VDDIOP0	PC10	MCI2_CDA	LCDDAT20	PIO	LCDDAT20	
VDDIOP0	PC11	MCI2_DA0	LCDDAT19	PIO	LCDDAT19	
VDDIOP0	PC12	MCI2_DA1	TIOA1	LCDDAT18	LCDDAT18	
VDDIOP0	PC13	MCI2_DA2	TIOB1	LCDDAT17	LCDDAT17	
VDDIOP0	PC14	MCI2_DA3	TCLK1	LCDDAT16	LCDDAT16	
VDDIOP0	PC15	MCI2_CK	PCK2	LCDDAT21	LCDDAT21	ISI_MCK
VDDIOP0	PC16	TK0	PIO	PU	TK0 Audio	
VDDIOP0	PC17	TF0	PIO	PU	TF0 Audio	
VDDIOP0	PC18	TD0	PIO	PU	TD0 Audio	
VDDIOP0	PC19	RK0	PIO	PU	RK0 Audio	
VDDIOP0	PC20	RF0	PIO	PU	RF0 Audio	
VDDIOP0	PC21	RD0	PIO	PU	RD0 Audio	
VDDIOP0	PC22	SPI1_MISO	PIO	PU	SPI1_MISO	SPI LCD
VDDIOP0	PC23	SPI1_MOSI	PIO	PU	SPI1_MOSI	SPI LCD
VDDIOP0	PC24	SPI1_SPCK	PIO	PU	SPI1_SPCK	SPI LCD
VDDIOP0	PC25	SPI1_NPCS0	PIO	PU	SPI1_NPCS0	
VDDIOP0	PC26	SPI1_NPCS1	TWD1	ISI_D11	ISI_D11	TWI LCD
VDDIOP0	PC27	SPI1_NPCS2	TWCK1	ISI_D10	ISI_D10	TWI LCD
VDDIOP0	PC28	SPI1_NPCS3	PWMFI0	ISI_D9	ISI_D9	SPI LCD
VDDIOP0	PC29	URXD0	PWMFI2	ISI_D8	ISI_D8	HDMI_INT
VDDIOP0	PC30	UTXD0	ISI_PCK	PIO	ISI_PCK	
VDDIOP0	PC31	FIQ	PWMFI1	PIO		Reset_HDMI

Table 6-22. PIO D Pin Assignment and Signal Description

Power Rail	Signal	Signal	Signal	Signal	SAMA5-MB	
VDDIOP1	PD0	MCI0_CDA	PIO	PU		MCI0_CDA
VDDIOP1	PD1	MCI0_DA0	PIO	PU		MCI0_DA0
VDDIOP1	PD2	MCI0_DA1	PIO	PU		MCI0_DA1
VDDIOP1	PD3	MCI0_DA2	PIO	PU		MCI0_DA2
VDDIOP1	PD4	MCI0_DA3	PIO	PU		MCI0_DA3
VDDIOP1	PD5	MCI0_DA4	TIOA0	PWMH2		MCI0_DA4
VDDIOP1	PD6	MCI0_DA5	TIOB0	PWML2		MCI0_DA5
VDDIOP1	PD7	MCI0_DA6	TCLK0	PWMH3		MCI0_DA6
VDDIOP1	PD8	MCI0_DA7	PWML3	PIO		MCI0_DA7
VDDIOP1	PD9	MCI0_CK	PIO	PU		MCI0_CK
VDDIOP1	PD10	SPI0_MISO	PIO	PU	CM_SerFlash	
VDDIOP1	PD11	SPI0_MOSI	PIO	PU	CM_SerFlash	
VDDIOP1	PD12	SPI0_SPCK	PIO	PU	CM_SerFlash	
VDDIOP1	PD13	SPI0_NPCS0	PIO	PU	CM_SerFlash	
VDDIOP1	PD14	SCK0	SPI0_NPCS1	CANRX0		CANRX0
VDDIOP1	PD15	CTS0	SPI0_NPCS2	CANTX0		CANTX0
VDDIOP1	PD16	RTS0	SPI0_NPCS3	PWMFI3	INT_AUDIO	
VDDIOP1	PD17	RXD0	PIO	PU		MCI0_CD
VDDIOP1	PD18	TXD0	PIO	PU		MCI1_CD
VDDIOP1	PD19	ADTRG	PIO	PU		ADTRG (HSYNC)
VDDANA	PD20	AD0	PIO	PU		LCD TSC
VDDANA	PD21	AD1	PIO	PU		LCD TSC
VDDANA	PD22	AD2	PIO	PU		LCD TSC
VDDANA	PD23	AD3	PIO	PU		LCD TSC
VDDANA	PD24	AD4	PIO	PU		LCD TSC
VDDANA	PD25	AD5	PIO	PU		EN5V_USBA
VDDANA	PD26	AD6	PIO	PU		EN5V_USBB
VDDANA	PD27	AD7	PIO	PU		EN5V_USBC
VDDANA	PD28	AD8	PIO	PU		OVCUR_USB
VDDANA	PD29	AD9	PIO	PU		VBUS_SENSE
VDDANA	PD30	AD10	PCK0	PIO	MCLK_AUDIO	MCLK_HDMI
VDDANA	PD31	AD11	PCK1	PIO		ISI_MCK

Table 6-23. PIO E Pin Assignment and Signal Description

Power Rail	Signal	Signal	Signal	SAMA5-CM	SAMA5-MB	
VDDIOM	PE0	A0/NBS0	I			
VDDIOM	PE1	A1	I	NOR		
VDDIOM	PE2	A2	I	NOR		
VDDIOM	PE3	A3	I	NOR		
VDDIOM	PE4	A4	I	NOR		
VDDIOM	PE5	A5	I	NOR		
VDDIOM	PE6	A6	I	NOR		
VDDIOM	PE7	A7	I	NOR		
VDDIOM	PE8	A8	I	NOR		
VDDIOM	PE9	A9	I	NOR		
VDDIOM	PE10	A10	I	NOR		
VDDIOM	PE11	A11	I	NOR		
VDDIOM	PE12	A12	I	NOR		
VDDIOM	PE13	A13	I	NOR		
VDDIOM	PE14	A14	I	NOR		
VDDIOM	PE15	A15	SCK3	NOR		
VDDIOM	PE16	A16	CTS3	NOR		
VDDIOM	PE17	A17	RTS3	NOR		
VDDIOM	PE18	A18	RXD3	NOR		
VDDIOM	PE19	A19	TXD3	NOR		
VDDIOM	PE20	A20	SCK2	NOR		
VDDIOM	PE21	A21/NANDALE	I	NOR / NAND		
VDDIOM	PE22	A22/NANDCLE	I	NOR / NAND		
VDDIOM	PE23	A23	CTS2	NOR		
VDDIOM	PE24	A24	RTS2	Power LED	ISI_RST	
VDDIOM	PE25	A25	RXD2	1-Wire / User LED	1-Wire	
VDDIOM	PE26	NCS0	TXD2	CS NOR		
VDDIOM	PE27	NCS1	TIOA2		PB_USER1	LCDDAT22
VDDIOM	PE28	NCS2	TIOB2		ZB_SLPTR	LCDDAT23
VDDIOM	PE29	NWR1/NBS1	TCLK2		ZB_RST	
VDDIOM	PE30	NWAIT	I		ZB_IRQ1	INT_ETH1
VDDIOM	PE31	IRQ	PWML1		ZB_IRQ0	HDMI_INT

6.4.19 IO Expansion Port J1

Figure 6-41. IO Expansion Socket J1

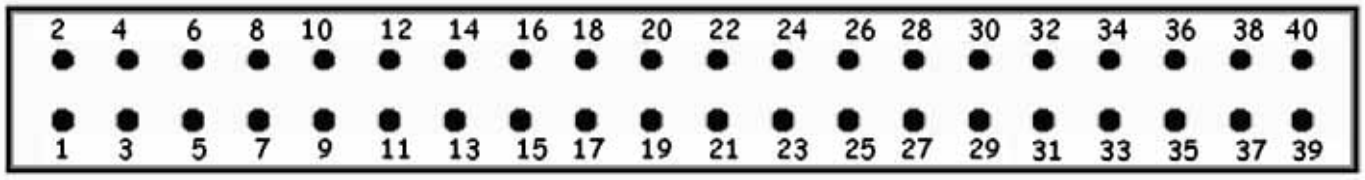


Table 6-24. IO Expansion Socket J1 HE10 Male 2*20 Signal Descriptions

Signal	Pin Num		Signal
VDDIOP0 / 5V	1	2	VDDIOP0 / 5V
GND	3	4	GND
PA0	5	6	PA16
PA1	7	8	PA17
PA2	9	10	PA18
PA3	11	12	PA19
PA4	13	14	PA20
PA5	15	16	PA21
PA6	17	18	PA22
PA7	19	20	PA23
PA8	21	22	PA24
PA9	23	24	PA25
PA10	25	26	PA26
PA11	27	28	PA27
PA12	29	30	PA28
PA13	31	32	PA29
PA14	33	34	PA30
PA15	35	36	PA31
GND	37	38	GND
VDDIOP0	39	40	VDDIOP0

6.4.20 IO Expansion Port J2

Figure 6-42. IO Expansion Socket J2

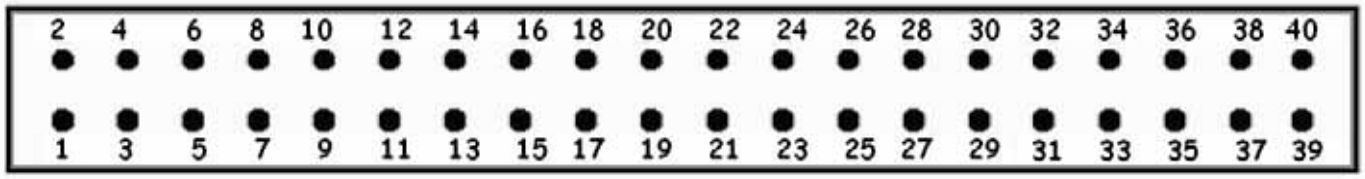


Table 6-25. Expansion Socket J2 HE10 Male 2*20 Signal Descriptions

Signal	Pin Num		Signal
VDDIOP0 / 5V	1	2	VDDIOP0 / 5V
GND	3	4	GND
PC0	5	6	PC16
PC1	7	8	PC17
PC2	9	10	PC18
PC3	11	12	PC19
PC4	13	14	PC20
PC5	15	16	PC21
PC6	17	18	PC22
PC7	19	20	PC23
PC8	21	22	PC24
PC9	23	24	PC25
PC10	25	26	PC26
PC11	27	28	PC27
PC12	29	30	PC28
PC13	31	32	PC29
PC14	33	34	PC30
PC15	35	36	PC31
GND	37	38	GND
VDDIOP0	39	40	VDDIOP0

6.4.21 IO Expansion Port J3

Figure 6-43. IO Expansion Socket J3

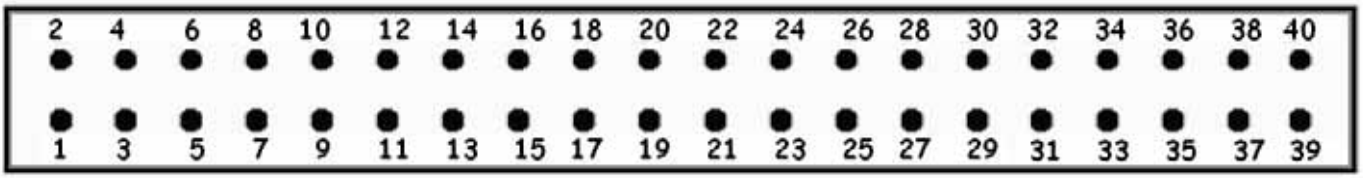


Table 6-26. Expansion Socket J3 HE10 Male 2*20 Signal Descriptions

Signal	Pin Num		Signal
VDDIOP0 / 5V	1	2	VDDIOP0 / 5V
GND	3	4	GND
PB10	5	6	PB31
PB12	7	8	PE23
PB14	9	10	PE24
PB15	11	12	PE25
PB19	13	14	PE26
PB20	15	16	PE29
PB21	17	18	PE30
PB22	19	20	PE31
PB23	21	22	PD10
PB24	23	24	PD11
PB25	25	26	PD12
PB26	27	28	PD13
PB27	29	30	PD14
PB28	31	32	PD15
PB29	33	34	PD19
PB30	35	36	PD31
GND	37	38	GND
VDDIOP0	39	40	VDDIOP0

6.4.22 SODIMM Card Edge Socket

The SAMA5D3 series-EK implements a SODIMM200 standard connector for CM board interfacing.

Please note this is not an industry standard pin-out and that it is unlikely to be compatible with off the self SODIMM.

Figure 6-44. SODIMM200 Socket CON1

Table 6-27. SODIMM200 CON1 Signal Descriptions

PIOC	PIOB	PIOA		SODIMM 200			PIOA	PIOB	PIOC
			Front Side	A	B	Back Side			
		VCC 5V		1	2	VCC 5V			
		VCC 5V		3	4	VCC 5V			
		GND		5	6	VBAT			
		CTS2	PE23	7	8	PE29	NWR1/NBS1	TCLK2	
		RTS2	PE24	9	10	PE30	NWAIT		
		RXD2	PE25	11	12	PE31	IRQ	PWML1	
		TXD2	PE26	13	14			GND	
		VDDIOM		15	16	VDDIOM			
		SPI1_NPCS0	PC25	17	18	PC24	SPI1_SPCK		
		SPI1_MOSI	PC23	19	20	PC22	SPI1_MISO		
		RD0	PC21	21	22	PC20	RF0		
		GND		23	24	PC19	RK0		
		TD0	PC18	25	26	PC17	TF0		
		TK0	PC16	27	28	PC9	EMDIO	PIO	
	TCLK5	EMDC	PC8	29	30	PC7	EREFCK	TIOB5	
	TIOA5	ERXER	PC6	31	32			GND	
	TIOB4	ETXEN	PC4	33	34	PC5	ECRSDV	TCLK4	
	TCLK3	ERX0	PC2	35	36	PC3	ERX1	TIOA4	
	TIOA3	ETX0	PC0	37	38	PC1	ETX1	TIOB3	
	Power Enable		Enable_0	39	40	Enable_1	CS Boot Disable		
				KEY					
		VCC 3V3		41	42	VCC 3V3			
		VCC 3V3		43	44	VCC 3V3			
		NC	Enable_2	45	46	Enable_3	NC		
		NC		47	48		ADVREF		
LCDDAT22	TIOA2	NCS1	PE27	49	50	PE28	NCS2	TIOB2	LCDDAT23
	LCDDAT20	MCI2_CDA	PC10	51	52	PC11	MCI2_DA0	LCDDAT19	PIO
		GND		53	54	PC13	MCI2_DA2	TIOB1	LCDDAT17
LCDDAT18	TIOA1	MCI2_DA1	PC12	55	56	PC15	MCI2_CK	PCK2	LCDDAT21
LCDDAT16	TCLK1	MCI2_DA3	PC14	57	58	PC26	SPI1_NPCS1		ISI_D11
ISI_D10		SPI1_NPCS2	PC27	59	60	PC28	SPI1_NPCS3	PWMFI0	ISI_D9
ISI_D8	PWMFI2	URXD0	PC29	61	62		GND		
	PWMFI1	FIQ	PC31	63	64	PC30	UTXD0	ISI_PCK	
VDDIOP0				65	66	VDDIOP0			
		LCDDAT0	PA0	67	68	PA1	LCDDAT1		
		LCDDAT2	PA2	69	70	PA3	LCDDAT3		

Table 6-27. SODIMM200 CON1 Signal Descriptions

PIOC	PIOB	PIOA		SODIMM 200			PIOA	PIOB	PIOC
		GND		71	72	PA4	LCDDAT4		
		LCDDAT5	PA5	73	74	PA6	LCDDAT6		
		LCDDAT7	PA7	75	76	PA8	LCDDAT8		
		LCDDAT9	PA9	77	78	PA10	LCDDAT10		
		LCDDAT11	PA11	79	80		GND		
		LCDDAT12	PA12	81	82	PA13	LCDDAT13		
		LCDDAT14	PA14	83	84	PA15	LCDDAT15		
	ISI_D0	LCDDAT16	PA16	85	86	PA17	LCDDAT17	ISI_D1	
ISI_D2	TWD2	LCDDAT18	PA18	87	88	PA19	LCDDAT19	TWCK2	ISI_D3
		GND		89	90	PA20	LCDDAT20	PWMH0	ISI_D4
ISI_D5	PWML0	LCDDAT21	PA21	91	92	PA22	LCDDAT22	PWMH1	ISI_D6
ISI_D7	PWML1	LCDDAT23	PA23	93	94	PA24	LCDPWM		
		LCDDISP	PA25	95	96	PA26	LCDVSYNC		
		LCDHSYNC	PA27	97	98		GND		
		LCDPCK	PA28	99	100	PA29	LCDDEN		
ISI_VSYNC	URXD1	TWD0	PA30	101	102	PA31	TWCK0	UTXD1	ISI_HSYNC
VDDANA				103	104	VDDANA			
	PCK0	AD10	PD30	105	106	PD31	AD11	PCK1	
		GND		107	108	PD29	AD9		
		AD8	PD28	109	110	PD27	AD7		
		AD6	PD26	111	112	PD25	AD5		
		AD4	PD24	113	114	PD23	AD3		
		AD2	PD22	115	116		GND		
		AD0	PD20	117	118	PD21	AD1		
		TXD0	PD18	119	120	PD19	ADTRG		
PWMFI3	SPI0_NPCS3	RTS0	PD16	121	122	PD17	RXD0	PIO	
CANRX0	SPI0_NPCS1	SCK0	PD14	123	124	PD15	CTS0	SPI0_NPCS2	CANTX0
		GND		125	126	PD13	SPI0_NPCS0		
		SPI0_SPCK	PD12	127	128	PD11	SPI0_MOSI		
		SPI0_MISO	PD10	129	130	PD9	MCI0_CK		
PIO	PWML3	MCI0_DA7	PD8	131	132	PD7	MCI0_DA6	TCLK0	PWMH3
PWML2	TIOB0	MCI0_DA5	PD6	133	134		GND		
PWMH2	TIOA0	MCI0_DA4	PD5	135	136	PD4	MCI0_DA3		
		MCI0_DA2	PD3	137	138	PD2	MCI0_DA1		
		MCI0_DA0	PD1	139	140	PD0	MCI0_CDA		
VDDIOP1				141	142	VDDIOP1			
		GND		143	144	PB13	GRXER	PWML3	
	RF1	GTXER	PB10	145	146	PB12	GRXDV	PWMH3	
	CANRX1	GCRS	PB14	147	148	PB15	GCOL	CANTX1	

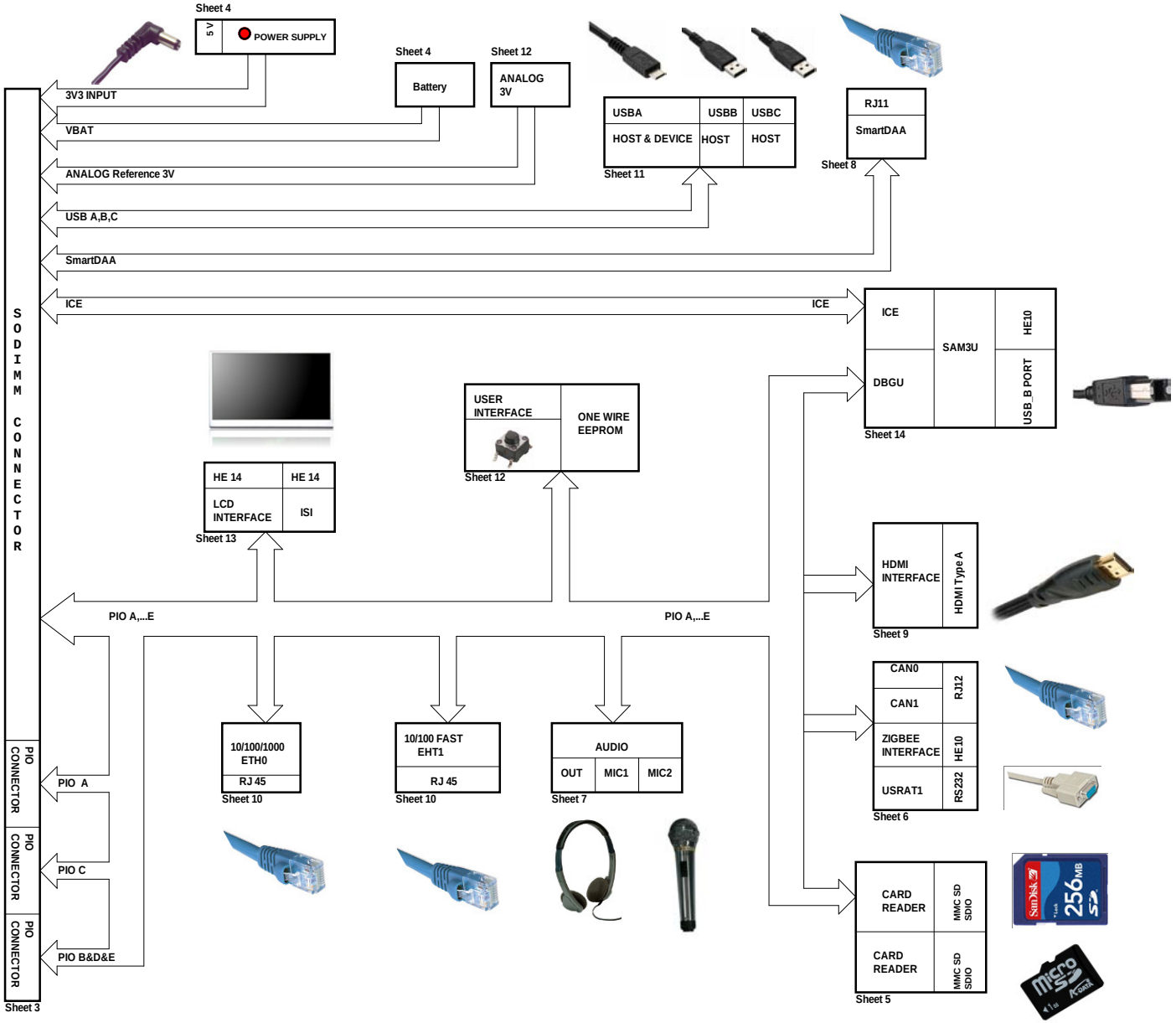
Table 6-27. SODIMM200 CON1 Signal Descriptions

PIOC	PIOB	PIOA		SODIMM 200			PIOA	PIOB	PIOC
	GTX4	MCI1_CDA	PB19	149	150	PB20	MCI1_DA0	GTX5	
	GTX6	MCI1_DA1	PB21	151	152	PB22	MCI1_DA2	GTX7	
	GRX4	MCI1_DA3	PB23	153	154		GND		
	GRX5	MCI1_CK	PB24	155	156	PB25	SCK1	GRX6	
		GND		157	158	PB27	RTS1	PWMH1	
	USB A	USBA_DP		159	160	PB29	TXD1	PIO	
	USB A	USBA_DM		161	162	PB31	DTXD		
		GND		163	164	PB30	DRXD		
	USB B	USBB_DP		165	166	PB26	CTS1	GRX7	
	USB B	USBB_DM		167	168	PB28	RXD1	PIO	
		GND		169	170		GND		
	USB C	USBC_DP		171	172	DIB	DIBP		
	USB C	USBC_DM		173	174	DIB	DIBN		
		GND_ETH		175	176		GND		
	GIGA_ETH	ETH0_TX1+		177	178		JTAGSEL	SYSC	
	GIGA_ETH	ETH0_TX1-		179	180		WKUP	SYSC	
	GIGA_ETH	ETH0_RX1+		181	182		SHDN	SYSC	
	GIGA_ETH	ETH0_RX1-		183	184		BMS	RSTJTAG	
		GND_ETH		185	186		nRST	SYSC	
	GIGA_ETH	ETH0_TX2+		187	188		nTRST	RSTJTAG	
	GIGA_ETH	ETH0_TX2-		189	190		TDI	RSTJTAG	
	GIGA_ETH	ETH0_RX2+		191	192		TCK	RSTJTAG	
	GIGA_ETH	ETH0_RX2-		193	194		TMS	RSTJTAG	
		GND		195	196		TDO	RSTJTAG	
		LED2		197	198		RTCK	RSTJTAG	
		LED1		199	200		GND		

6.5 Schematics

This section contains the following schematics:

- Block Diagram
- Describe
- SODIMM
- Power Supply
- HSMCI
- CAN & ZigBee & USART1
- Audio
- Smart DAA
- HDMI
- ETH
- USB Interface
- Miscellaneous
- LCD & ISI
- Segger - SAM3U



C		Derek	30-Sep-12	XX	XX-XXX-XX
B		Derek	30-Mar-12	XX	XX-XXX-XX
A		Derek	11-Nov-11	XX	XX-XXX-XX
REV.	MODIF.	DES.	DATE	VER.	DATE

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SAMA5D3x-MB

BLOCK Diagram

SCALE 1/1

REV. C

SHEET 1/14

REVISION HISTORY

REV	DATA	NOTE
A	2011.11	ORIGINAL RELEASED
B	2012.03	SECOND RELEASED
C	2012.10	THIRD RELEASED

JUMPER and SOLDERDROP

PAGE	REFERENCE	DEFAULT	FUNCTION
3	JP1	1-2	VDDIOP0 or 5V selection for J1
	JP2	1-2	VDDIOP0 or 5V selection for J2
	JP3	1-2	VDDIOP1 or 5V selection for J3
	JP9	OPEN	Default boot on embedded ROM,Close boot on external memory
4	JP4	CLOSE	Backup supply on/off
	JP5	CLOSE	Force power on function
5	JP6	CLOSE	MCI0 write protect select
6	JP7	CLOSE	CAN0 diff termination select
	JP8	CLOSE	CAN1 diff termination select
	JP10	OPEN	Zigbee Power on/off select
12	JP14	1-2	ADVREF input selection
14	JP15	OPEN	JTAG Enabled,close to disable
14	JP16	OPEN	CDC Enabled,close to disable
11	JP17	OPEN	Enable LCD for D31,D33,D34
		CLOSE	Disable LCD for D35

TABLE OF CONTENTS

PAGE	DESCRIPTION
1	Block Diagram
2	Describe
3	SODIMM
4	POWER SUPPLY
5	HSMCI
6	CAN & ZIGBEE &USART1
7	AUDIO
8	SmartDAA
9	HDMI
10	ETH
11	USB Interface
12	Miscellaneous
13	LCD&ISI
14	Segger-SAM3U

SAMA5D3x config

	SAMA5D31	SAMA5D33	SAMA5D34	SAMA5D35
CAN0			✓	✓
CAN1			✓	✓
GMAC		✓	✓	✓
EMAC	✓			✓
HSMCI2	✓		✓	✓
LCDC	✓	✓	✓	
USART0	✓			✓
USART1	✓			✓
ISI	✓	✓	✓	✓
TC1				✓

SCHEMATICS CONVENTIONS

(1) Resistance Unit: "K" is "Kohm", "R" is "Ohm"

(2) "DNP" means the component is not populated by default

TEST POINT

PAGE	REFERENCE	FUNCTION
4	TP1, TP2	GND
4	TP3	5V
4	TP4	3V3
4	TP5	VDDIOP0
4	TP6	VDDIOP1
4	TP7	VDDIOM
4	TP8	VDDANA

DEFAULT NO POPULATE PARTS

PAGE	REFERENCE	FUNCTION
3	R6,R51,R50,R120	Optional PD10,PD11,PD12,PD13 from MB
5	R58	Optional for MCI0 Power supply mode
	R121	Optional for MCI1 Power supply mode
6	R52, R53,R55,R56,R57,R82,JP10	Optional Zigbee
	R132,R133	Debug or USART1 option
7	C89,C90,R118,R119,J26	Optional Audio Line out,mic in
	R80,R81	Optional MIC level setting
	R230	Optional audio TK
9	L38,L39,L40,L41	Optional HDMI EMI filter
	R89	HDMI chip I2C address setting
	R266	Optional for I2S PCLK
	R42	Optional for LCD PCLK
10	R162,R170,R171,R172,R176,R177,C122,C123,	Optional for KSZ8041NL
12	R144	Optional pull up for DS28EC20P
13	R127	Optional for ADC triger
14	R79, R106,R107,R109,R113,R110,R112,R111,J9	Optional JTAG
	R54	SAM3U JTAG selection
	R63	5V Option
	D11,D12	USB ESD protect option
	R186	Main 3V3 Optional for VCC_3V3_DEBUG

PIO MUXING

PIOA	USAGE	PIOA	USAGE	PIOB	USAGE	PIOB	USAGE	PIOC	USAGE	PIOC	USAGE	PIOD	USAGE	PIOD	USAGE	PIOE	USAGE	PIOE	USAGE
PA0	LCDD0	PA16	ISI_D0	PB0		PB16		PC0	E1_TX0	PC16	TK0	PD0	MCI0_CDA	PD16	INT_AUDIO	PE0		PE16	
PA1	LCDD1	PA17	ISI_D1	PB1		PB17		PC1	E1_TX1	PC17	TF0	PD1	MCI0_DA0	PD17	MCI0_CD	PE1		PE17	
PA2	LCDD2	PA18	ISI_D2	PB2		PB18		PC2	E1_RX0	PC18	TD0	PD2	MCI0_DA1	PD18	MCI1_CD	PE2		PE18	
PA3	LCDD3	PA19	ISI_D3	PB3		PB19	MCI1_CDA	PC3	E1_RX1	PC19	RK0	PD3	MCI0_DA2	PD19	ADTRG	PE3		PE19	
PA4	LCDD4	PA20	ISI_D4	PB4		PB20	MCI1_DA0	PC4	E1_TXEN	PC20	RF0	PD4	MCI0_DA3	PD20	AD0_XP	PE4		PE20	
PA5	LCDD5	PA21	ISI_D5	PB5		PB21	MCI1_DA1	PC5	E1_CRSDV	PC21	RD0	PD5	MCI0_DA4	PD21	AD1_XM	PE5		PE21	
PA6	LCDD6	PA22	ISI_D6	PB6		PB22	MCI1_DA2	PC6	E1_RXER	PC22	SPI1_MISO	PD6	MCI0_DA5	PD22	AD2_YP	PE6		PE22	
PA7	LCDD7	PA23	ISI_D7	PB7		PB23	MCI1_DA3	PC7	E1_TXCK	PC23	SPI1_MOSI	PD7	MCI0_DA6	PD23	AD3_YM	PE7		PE23	
PA8	LCDD8	PA24	LCDPWM	PB8		PB24	MCI1_CK	PC8	E1_MDC	PC24	SPI1_SPCK	PD8	MCI0_DA7	PD24	AD4_LR	PE8		PE24	ISI_RST
PA9	LCDD9	PA25	LCDDISP	PB9		PB25		PC9	E1_MDIO	PC25	SPI1_NPCS0	PD9	MCI0_CK	PD25	EN5V_HDA	PE9		PE25	ONE_WIRE
PA10	LCDD10	PA26	LCDVSYNC	PB10	PWR_MCI0	PB26	CTS1	PC10	LCDD20	PC26	TWD1 ISI_D11	PD10		PD26	EN5V_HDB	PE10		PE26	
PA11	LCDD11	PA27	LCDHSYNC	PB11		PB27	RTS1	PC11	LCDD19	PC27	TWCK1 ISI_D10	PD11		PD27	EN5V_HDC	PE11		PE27	PB_USER1 LCDD22
PA12	LCDD12	PA28	LCDPCK	PB12	PWR_MCI1	PB28	RXD1	PC12	LCDD18	PC28	SPI1_NPCS3 ISI_D9	PD12		PD28	OVCUR_USB	PE12		PE28	ZB_SLPTR LCDD23
PA13	LCDD13	PA29	LCDDEN	PB13		PB29	TXD1	PC13	LCDD17	PC29	HDMI_INT ISI_D8	PD13		PD29	VBUS_SENSE	PE13		PE29	ZB_RST
PA14	LCDD14	PA30	TWD0 ISI_VSYNC	PB14	CANRX1	PB30	DRXD	PC14	LCDD16	PC30	ISI_PCK	PD14	CANRX0	PD30	PCK0(Audio,HDMI)	PE14		PE30	ZB_IRQ1 INT_ETH1
PA15	LCDD15	PA31	TWCK0 ISI_HSYNC	PB15	CANTX1	PB31	DTXD	PC15	LCDD21	PC31	RESET_HDMI	PD15	CANTX0	PD31	PCK1(ISI_MCK)	PE15		PE31	ZB_IRQ0

REV.	MODIF.	DES.	DATE	VER.	DATE
C		Derek	30-Sep-12	X.X	XX-XXX-XX
B		Derek	30-Mar-12	X.X	XX-XXX-XX
A		Derek	11-Nov-11	X.X	XX-XXX-XX

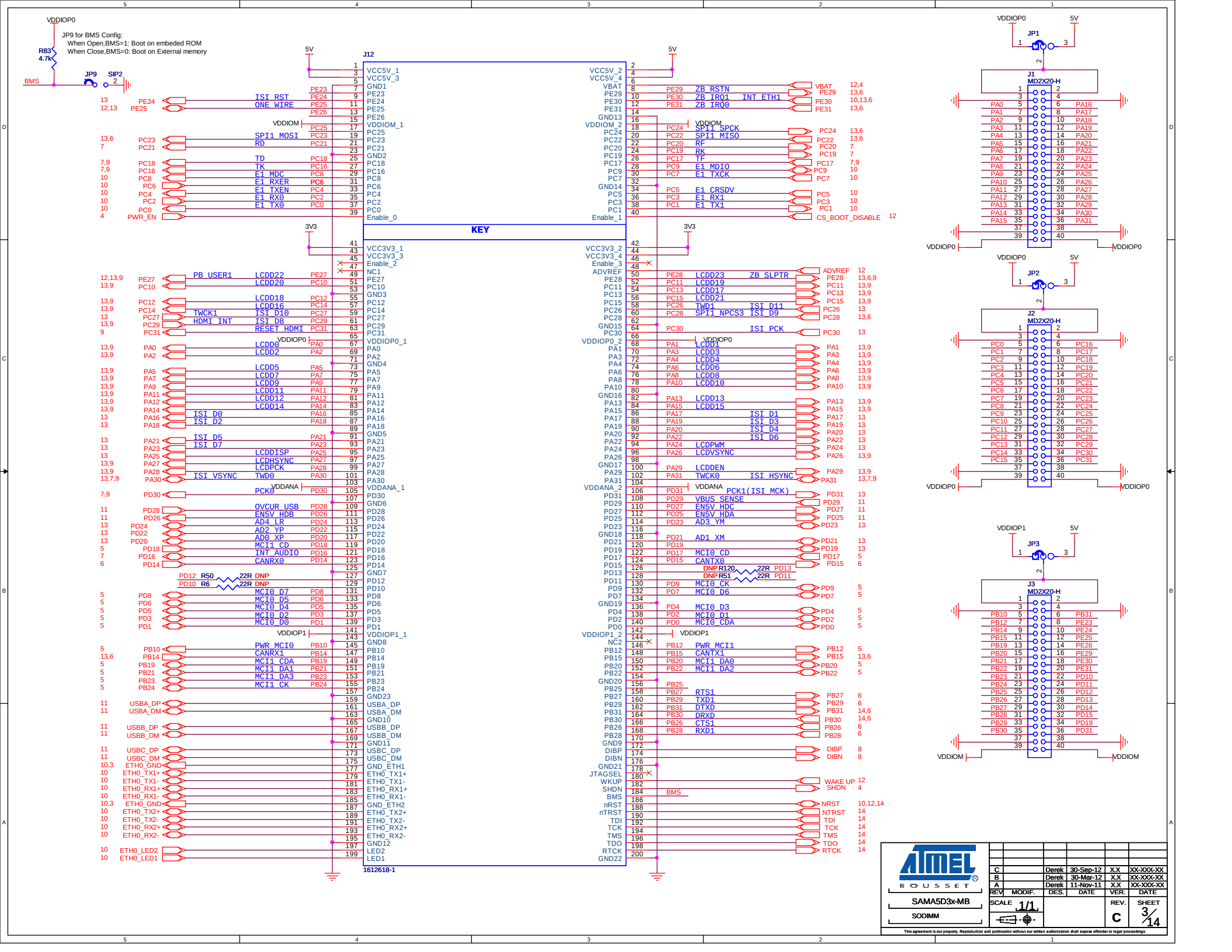
SAMA5D3x-MB

Describe

SCALE 1/1

REV. C

SHEET 2/14


JP9 for BMS Config:
When Open,BMS=1: Boot on embeded ROM
When Close,BMS=0: Boot on External memory
R83 4.7k
VDDIOP0
BMS
JP9
SIP2
J12
KEY
1612618-1
VDDIOM
VDDIOP0
VDDIOP1
VDDANA
3V3
5V
ISI_RST
ONE_WIRE
SPI1_MOSI
RD
TD
TK
E1_MDC
E1_RXER
E1_TXEN
E1_RX0
E1_TX0
PWR_EN
PB_USER1
LCDD22
LCDD20
LCDD18
LCDD16
TWCK1
ISI_D10
HDMI_INT
ISI_D8
RESET_HDMI
LCDD0
LCDD2
LCDD5
LCDD7
LCDD9
LCDD11
LCDD12
LCDD14
ISI_D0
ISI_D2
ISI_D5
ISI_D7
LCDDISP
LCDHSYNC
LCDPCK
ISI_VSYNC
TWD0
PCK0
OVCUR_USB
EN5V_HDB
AD4_LR
AD2_YP
AD0_XP
MCI1_CD
INT_AUDIO
CANRX0
R50 22R DNP
R6 22R DNP
MCI0_D7
MCI0_D5
MCI0_D4
MCI0_D2
MCI0_D0
PWR_MCI0
CANRX1
MCI1_CDA
MCI1_DA1
MCI1_DA3
MCI1_CK
USBA_DP
USBA_DM
USBB_DP
USBB_DM
USBC_DP
USBC_DM
ETH0_GND
ETH0_TX1+
ETH0_TX1-
ETH0_RX1+
ETH0_RX1-
ETH0_GND
ETH0_TX2+
ETH0_TX2-
ETH0_RX2+
ETH0_RX2-
ETH0_LED2
ETH0_LED1
ZB_RSTN
ZB_IRQ1
INT_ETH1
ZB_IRQ0
SPI1_SPCK
SPI1_MISO
RF
RK
TF
E1_MDIO
E1_TXCK
E1_CRSDV
E1_RX1
E1_TX1
CS_BOOT_DISABLE
LCDD23
ZB_SLPTR
LCDD19
LCDD17
LCDD21
TWD1
ISI_D11
SPI1_NPCS3
ISI_D9
ISI_PCK
LCDD1
LCDD3
LCDD4
LCDD6
LCDD8
LCDD10
LCDD13
LCDD15
ISI_D1
ISI_D3
ISI_D4
ISI_D6
LCDPWM
LCDVSYNC
LCDDEN
TWCK0
ISI_HSYNC
PCK1(ISI_MCK)
VBUS_SENSE
EN5V_HDC
EN5V_HDA
AD3_YM
AD1_XM
MCI0_CD
CANTX0
DNP R120 22R
DNP R51 22R
MCI0_CK
MCI0_D6
MCI0_D3
MCI0_D1
MCI0_CDA
PWR_MCI1
CANTX1
MCI1_DA0
MCI1_DA2
RTS1
TXD1
DTXD
DRXD
CTS1
RXD1
DIBP
DIBN
WAKE UP
SHDN
BMS
NRST
NTRST
TDI
TCK
TMS
TDO
RTCK
JP1
JP2
JP3
J1
J2
J3
MD2X20-H
SAMA5D3x-MB
SODIMM
REV. C
SHEET 3/14
Derek 30-Sep-12 X.X XX-XXX-XX
Derek 30-Mar-12 X.X XX-XXX-XX
Derek 11-Nov-11 X.X XX-XXX-XX
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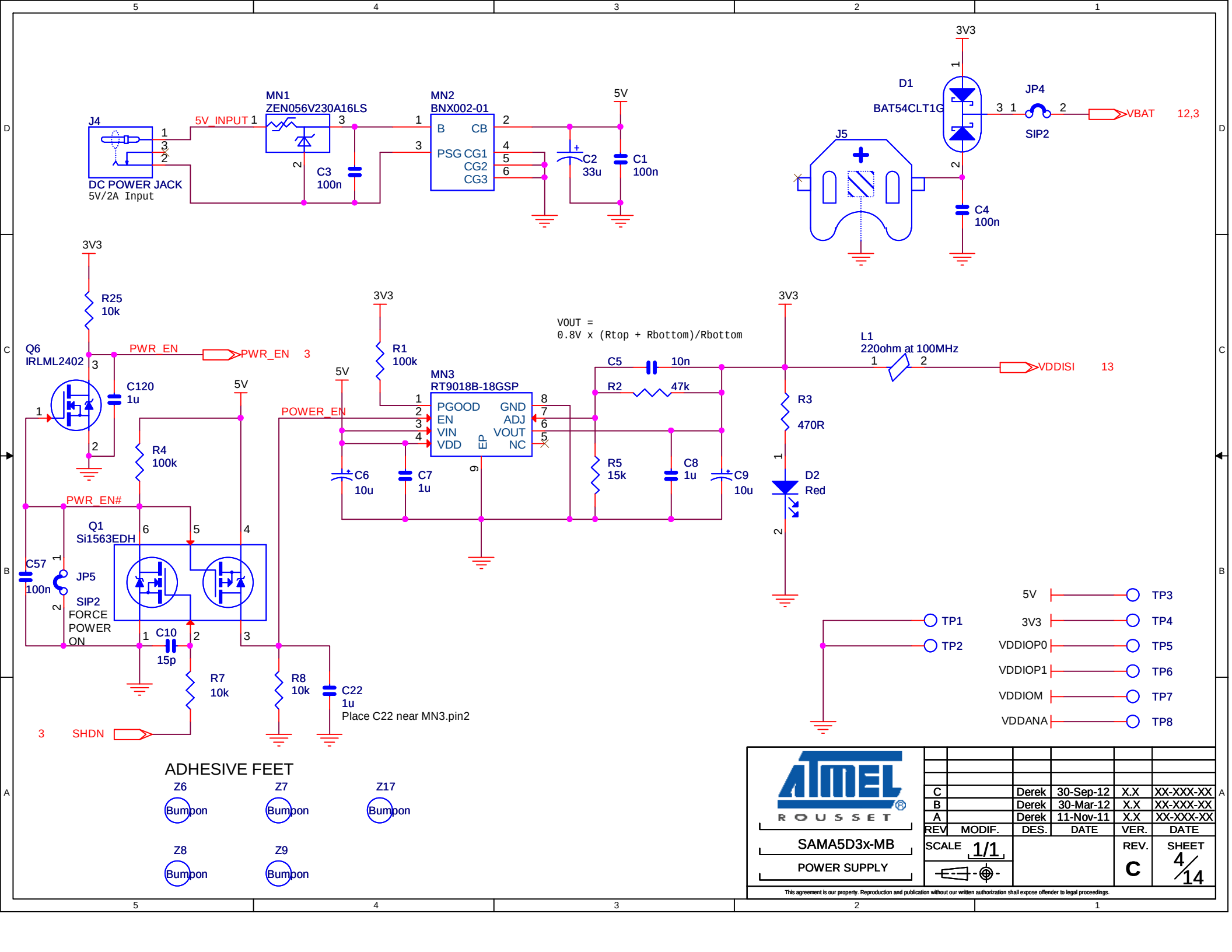

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B		Derek	30-Mar-12	X.X	XX-XXX-XX
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ATMEL ROUSSET

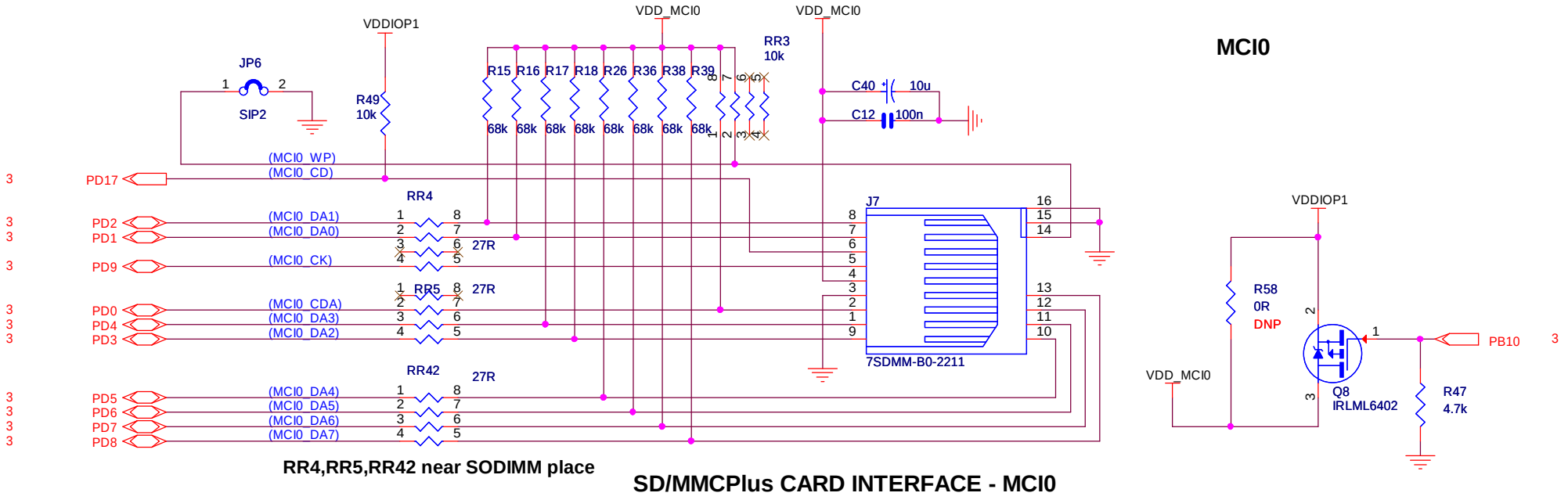
SAMA5D3x-MB

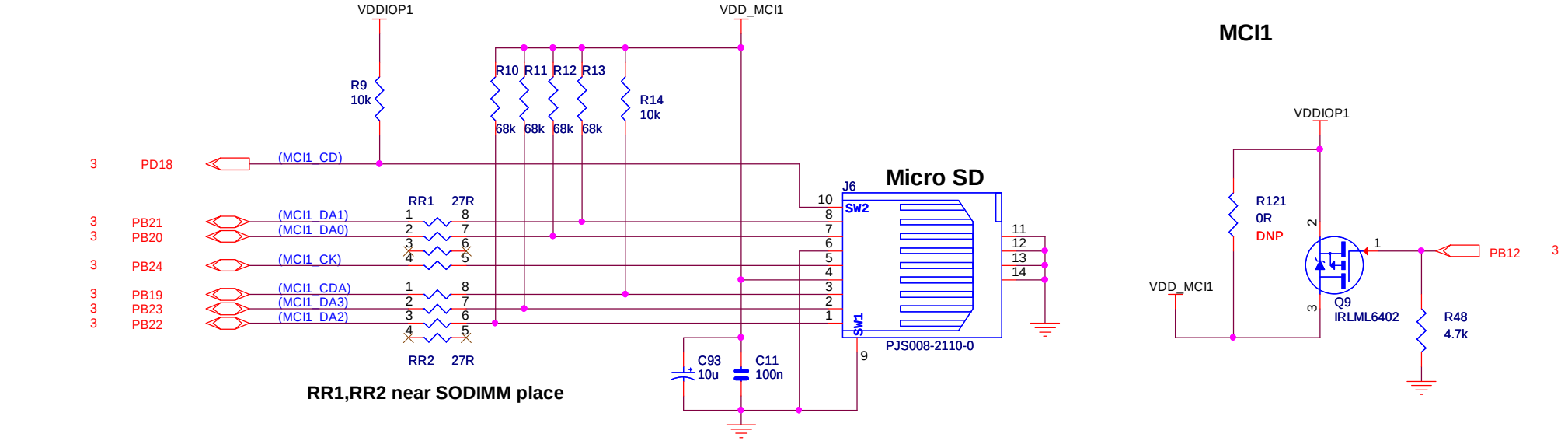
POWER SUPPLY

SCALE 1/1

REV. C

SHEET 4/14





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REV	MODIF.	DES.	DATE	VER.	DATE

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HSMCI

SCALE 1/1

REV. C

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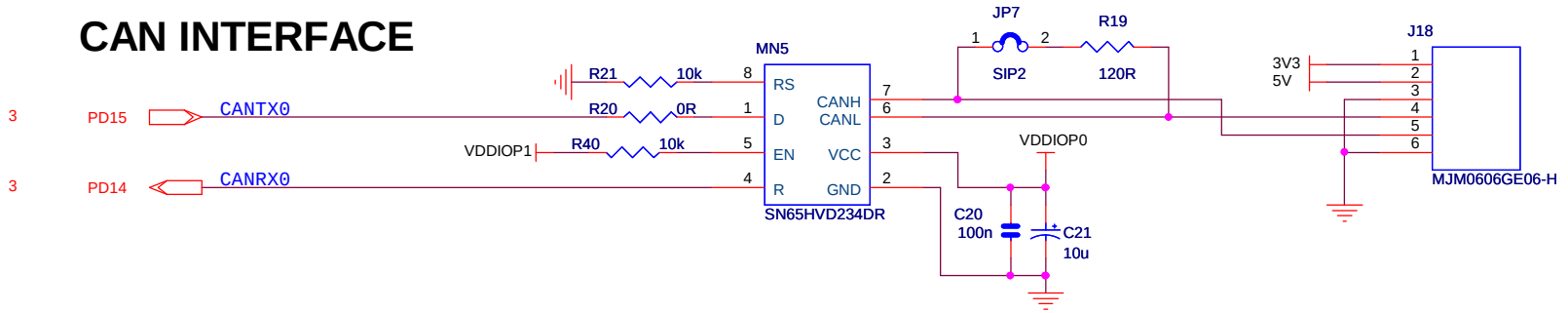
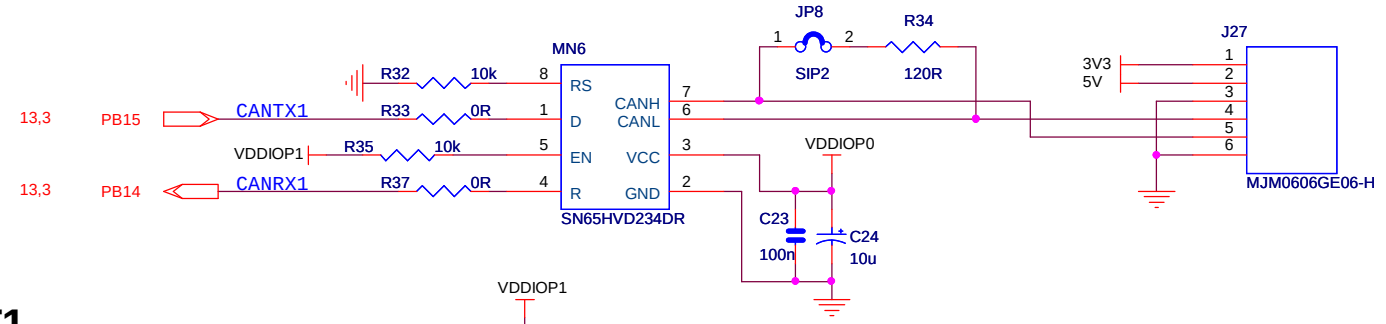
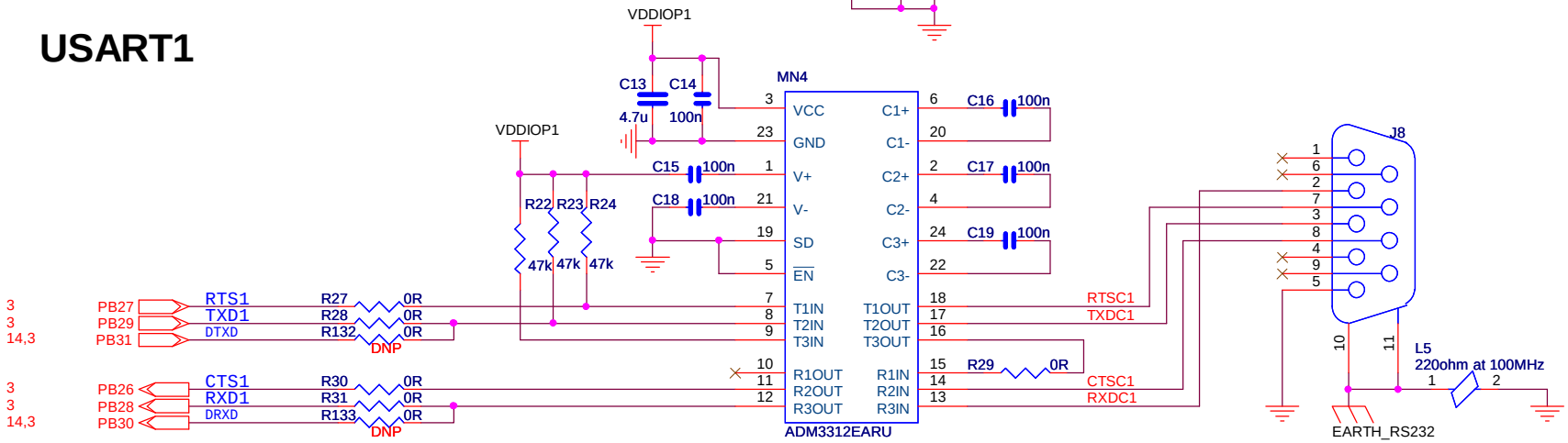
CAN INTERFACE

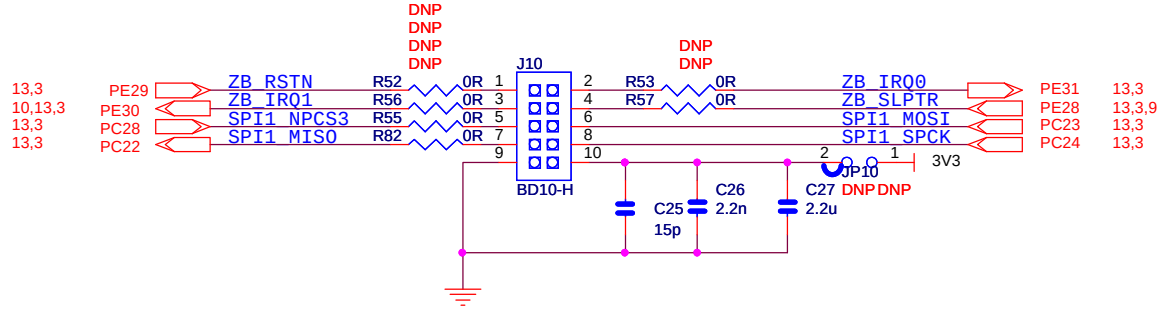




USART1



ZIGBEE INTERFACE



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B		Derek	30-Mar-12	X.X	XX-XXX-XX
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CAN & ZIGBEE & USART1

SCALE 1/1

REV. C

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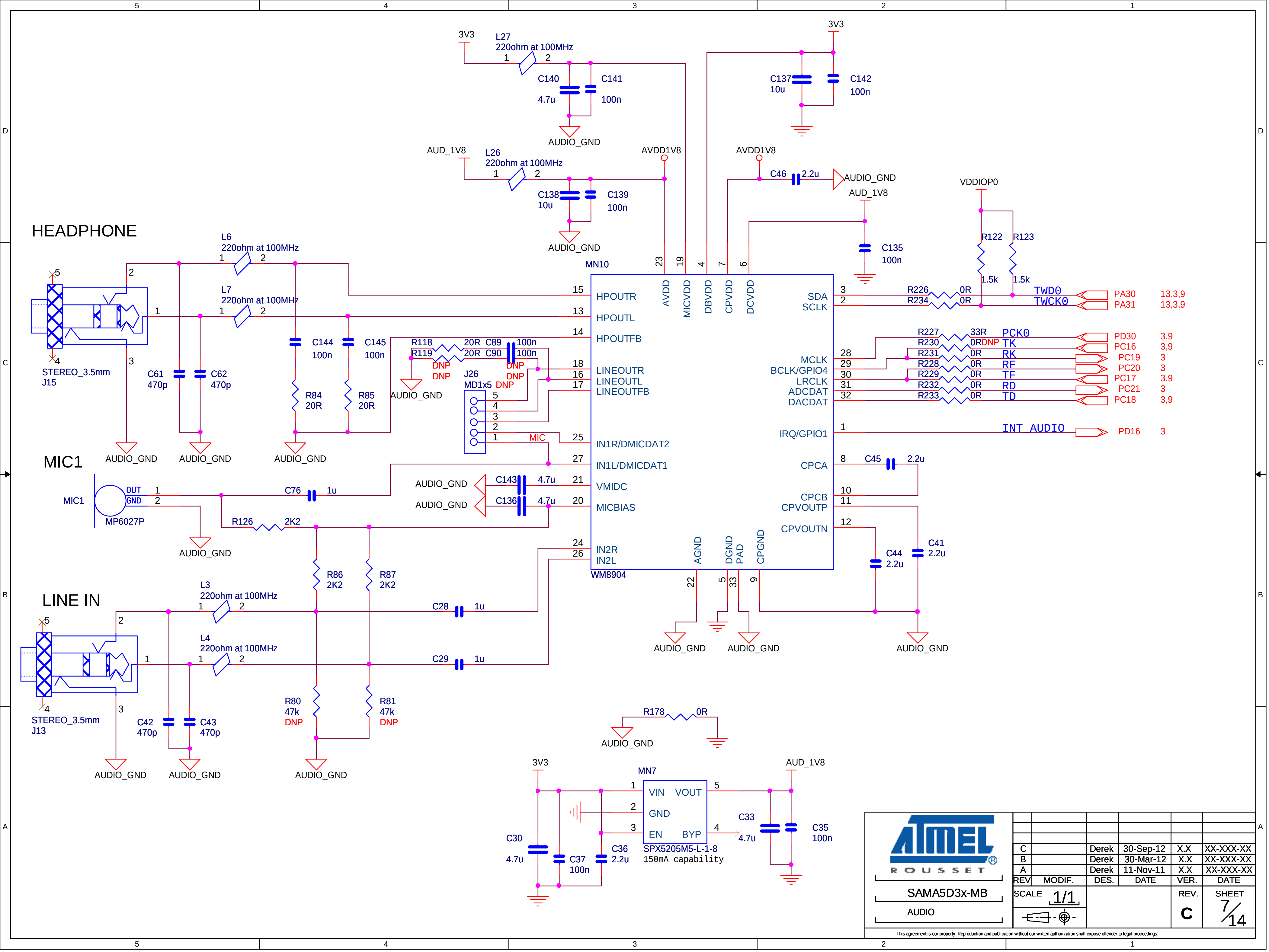
HEADPHONE
MIC1
LINE IN
STEREO_3.5mm
J15
J13
L6 220ohm at 100MHz
L7 220ohm at 100MHz
L27 220ohm at 100MHz
L26 220ohm at 100MHz
L3 220ohm at 100MHz
L4 220ohm at 100MHz
3V3
AUD_1V8
AVDD1V8
VDDIOP0
AUDIO_GND
C140 4.7u
C141 100n
C137 10u
C142 100n
C138 10u
C139 100n
C46 2.2u
C135 100n
C144 100n
C145 100n
C61 470p
C62 470p
R84 20R
R85 20R
R118 20R
R119 20R
C89 100n
C90 100n
DNP
J26 MD1x5
MIC
MN10
WM8904
HPOUTR
HPOUTL
HPOUTFB
LINEOUTR
LINEOUTL
LINEOUTFB
IN1R/DMICDAT2
IN1L/DMICDAT1
VMIDC
MICBIAS
IN2R
IN2L
AVDD
MICVDD
DBVDD
CPVDD
DCVDD
AGND
DGND
PAD
CPGND
SDA
SCLK
MCLK
BCLK/GPIO4
LRCLK
ADCDAT
DACDAT
IRQ/GPIO1
CPCA
CPCB
CPVOUTP
CPVOUTN
R122 1.5k
R123 1.5k
R226 0R
R234 0R
TWD0
TWCK0
PA30 13,3,9
PA31 13,3,9
R227 33R
R230 0R DNP
R231 0R
R228 0R
R229 0R
R232 0R
R233 0R
PCK0
TK
RK
RF
TF
RD
TD
PD30 3,9
PC16 3,9
PC19 3
PC20 3
PC17 3,9
PC21 3
PC18 3,9
INT AUDIO
PD16 3
C45 2.2u
C44 2.2u
C41 2.2u
C143 4.7u
C136 4.7u
C76 1u
MIC1 OUT GND
MP6027P
R126 2K2
R86 2K2
R87 2K2
C28 1u
C29 1u
R80 47k DNP
R81 47k DNP
C42 470p
C43 470p
R178 0R
MN7
VIN VOUT
GND
EN BYP
SPX5205M5-L-1-8
150mA capability
C30 4.7u
C37 100n
C36 2.2u
C33 4.7u
C35 100n
ATMEL
ROUSSET
SAMA5D3x-MB
AUDIO
C Derek 30-Sep-12 X.X XX-XXX-XX
B Derek 30-Mar-12 X.X XX-XXX-XX
A Derek 11-Nov-11 X.X XX-XXX-XX
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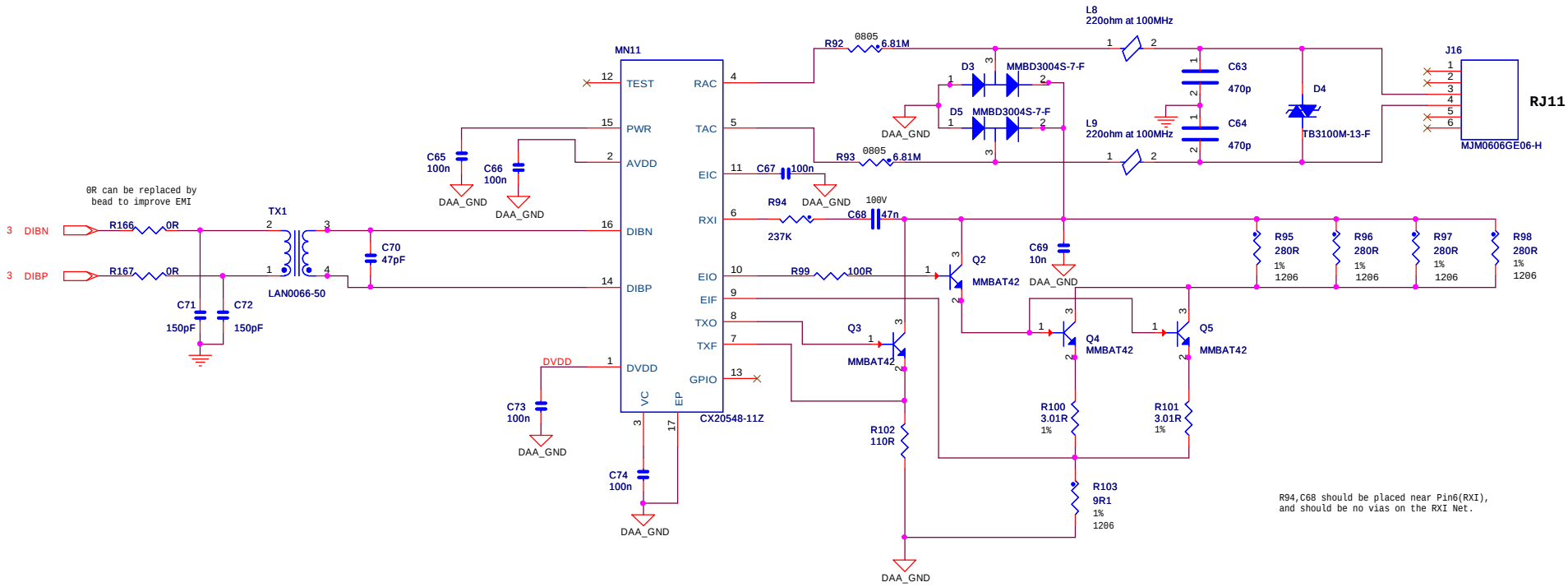

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B		Derek	30-Mar-12	X.X	XX-XXX-XX
A		Derek	11-Nov-11	X.X	XX-XXX-XX

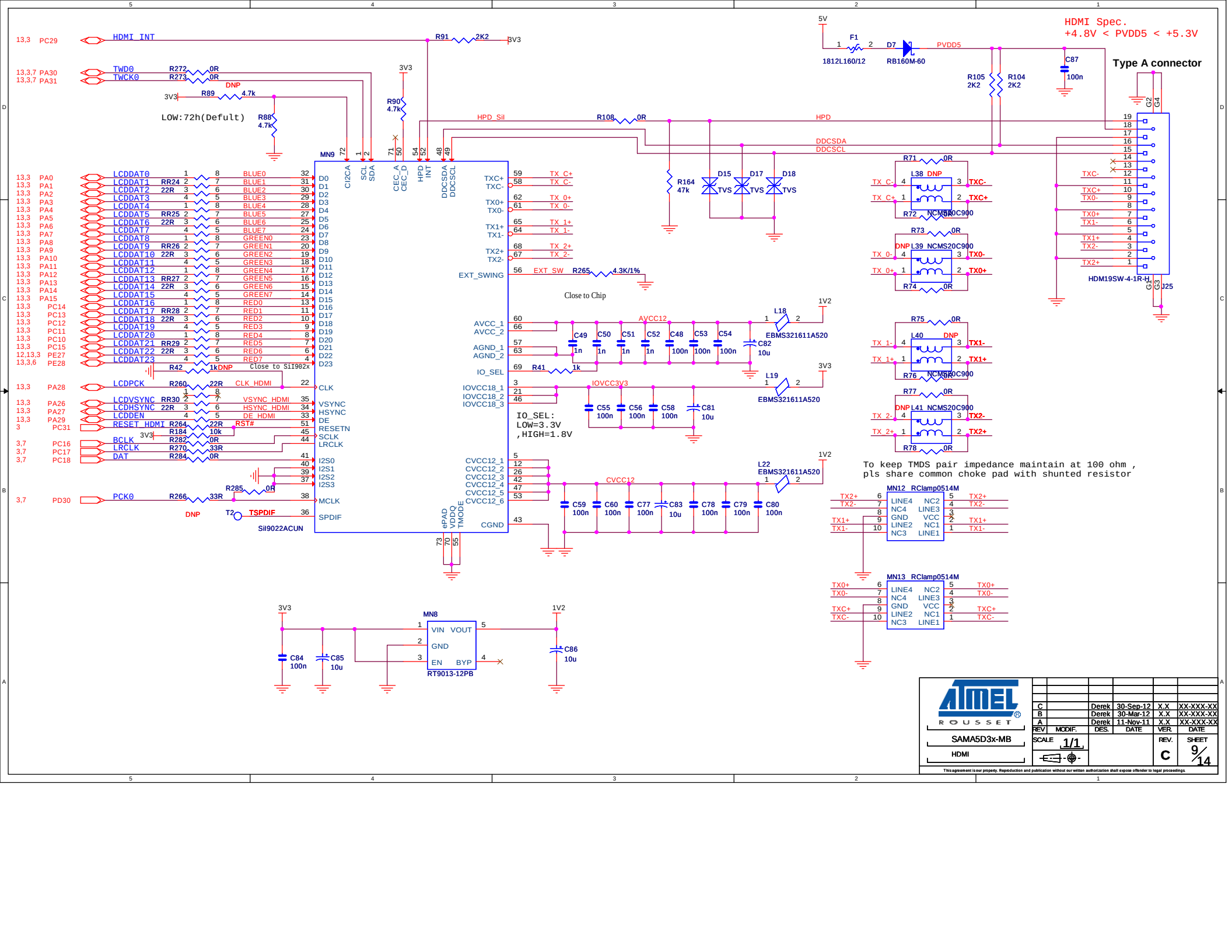
SAMA5D3x-MB

SmartDAA

SCALE 1/1

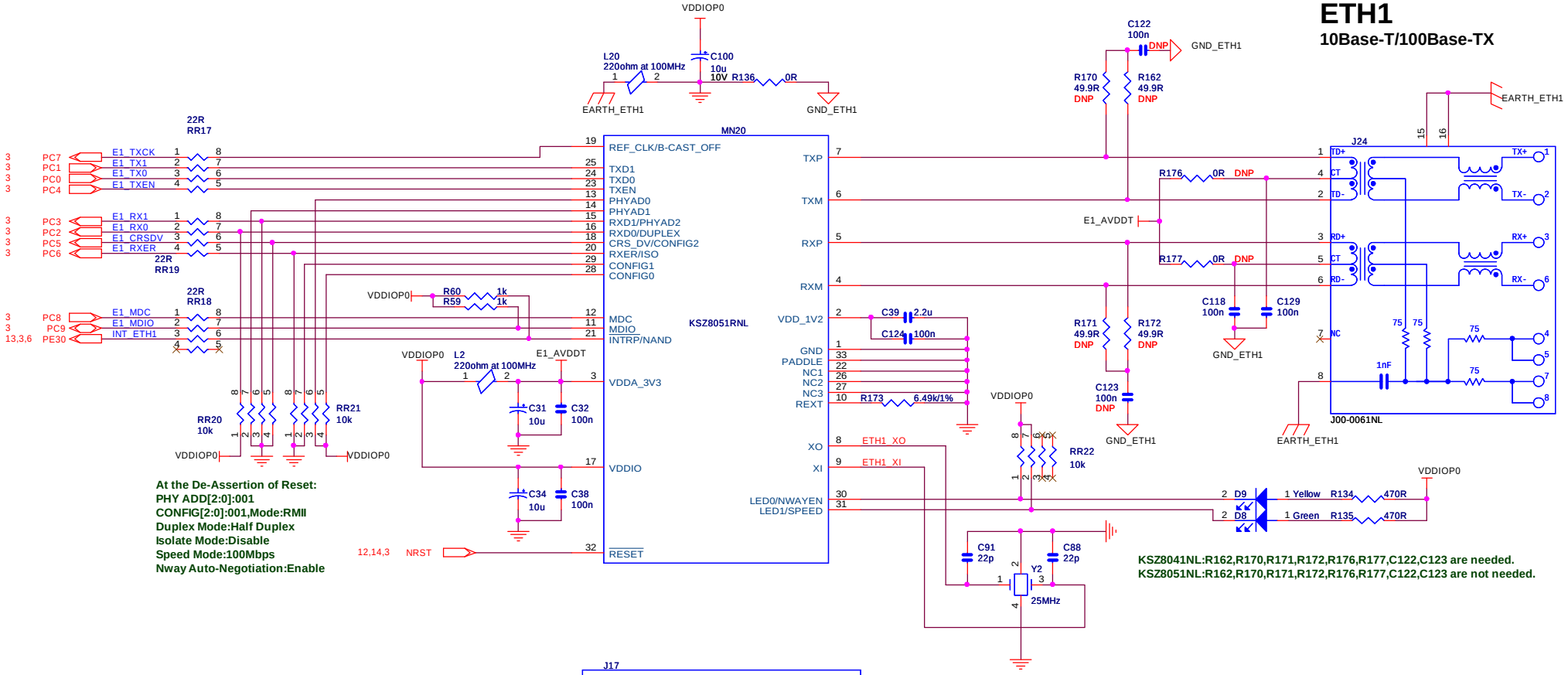
REV. C

SHEET 8/14


HDMI Spec.
+4.8V < PVDD5 < +5.3V
Type A connector
HDMI_INT
TWD0
TWCK0
LOW:72h(Defult)
HPD_Sil
HPD
DDCSDA
DDCSCL
PVDD5
RB160M-60
1812L160/12
HDM19SW-4-1R-H
Close to Chip
Close to Sil902x
EXT_SWING
IO_SEL:
LOW=3.3V
,HIGH=1.8V
To keep TMDS pair impedance maintain at 100 ohm ,
pls share common choke pad with shunted resistor
Sil9022ACUN
RT9013-12PB
EBMS321611A520
NCMS20C900
RClamp0514M
SAMA5D3x-MB
HDMI
ROUSSET
Derek 30-Sep-12 X.X XX-XXX-XX
Derek 30-Mar-12 X.X XX-XXX-XX
Derek 11-Nov-11 X.X XX-XXX-XX
SCALE 1/1
REV. C
SHEET 9/14

ETH1

10Base-T/100Base-TX

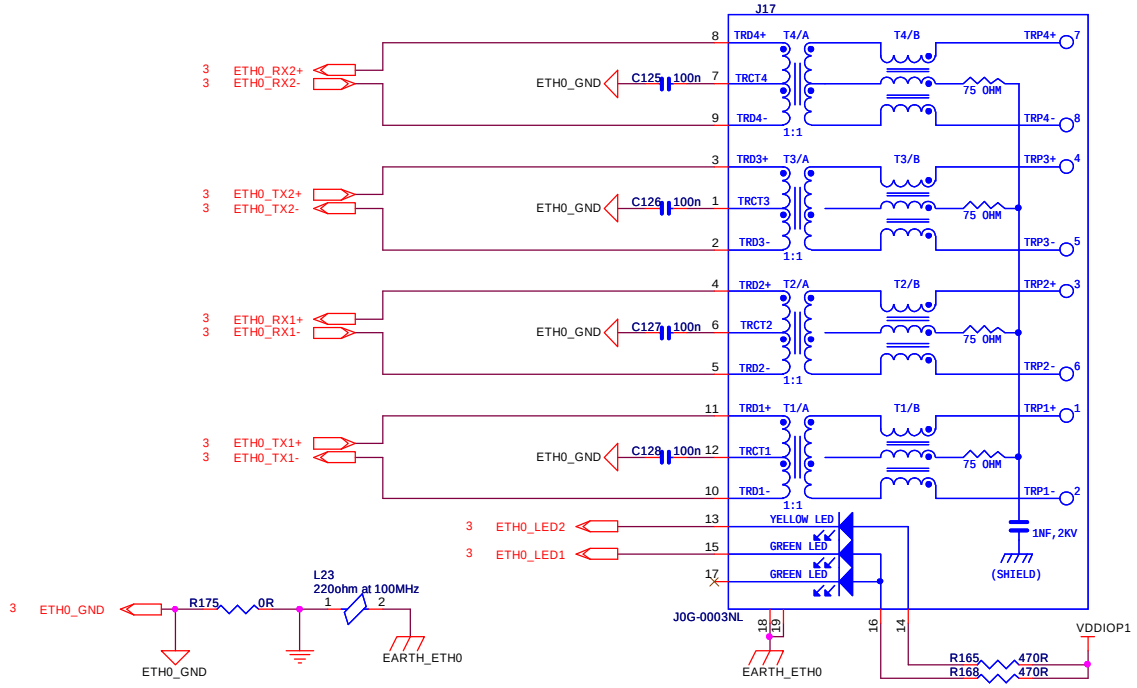


At the De-Assertion of Reset:
PHY ADD[2:0]:001
CONFIG[2:0]:001,Mode:RMII
Duplex Mode:Half Duplex
Isolate Mode:Disable
Speed Mode:100Mbps
Nway Auto-Negotiation:Enable

KSZ8041NL:R162,R170,R171,R172,R176,R177,C122,C123 are needed.
KSZ8051NL:R162,R170,R171,R172,R176,R177,C122,C123 are not needed.

ETH0

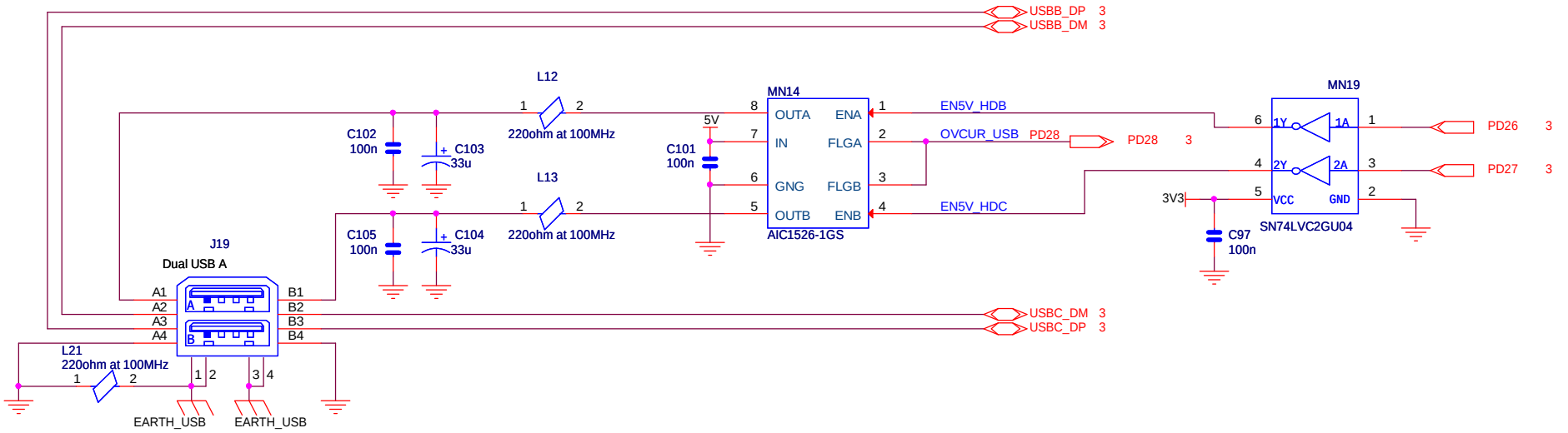
10Base-T/100Base-TX/1000BASE-T



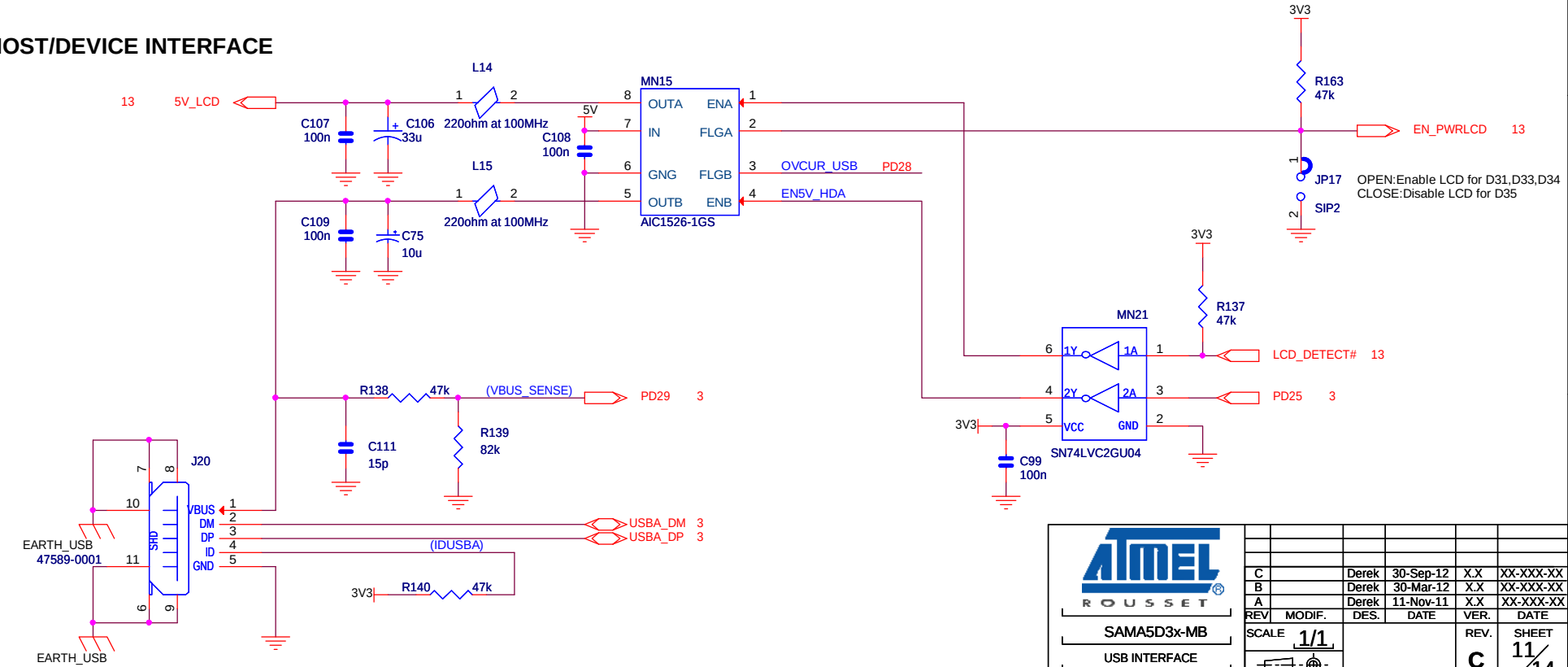
REV	MODIF.	DES.	DATE	VER.	DATE
C		Derek	30-Sep-12	X.X	XX-XXX-XX
B		Derek	30-Mar-12	X.X	XX-XXX-XX
A		Derek	11-Nov-11	X.X	XX-XXX-XX

SAMA5D3x-MB
ETH
SCALE 1/1
REV. C
SHEET 10/14

USB HOST B&C INTERFACE



USB A HOST/DEVICE INTERFACE



REV	MODIF.	DES.	DATE	VER.	DATE
C		Derek	30-Sep-12	X.X	XX-XXX-XX
B		Derek	30-Mar-12	X.X	XX-XXX-XX
A		Derek	11-Nov-11	X.X	XX-XXX-XX

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SAMA5D3x-MB

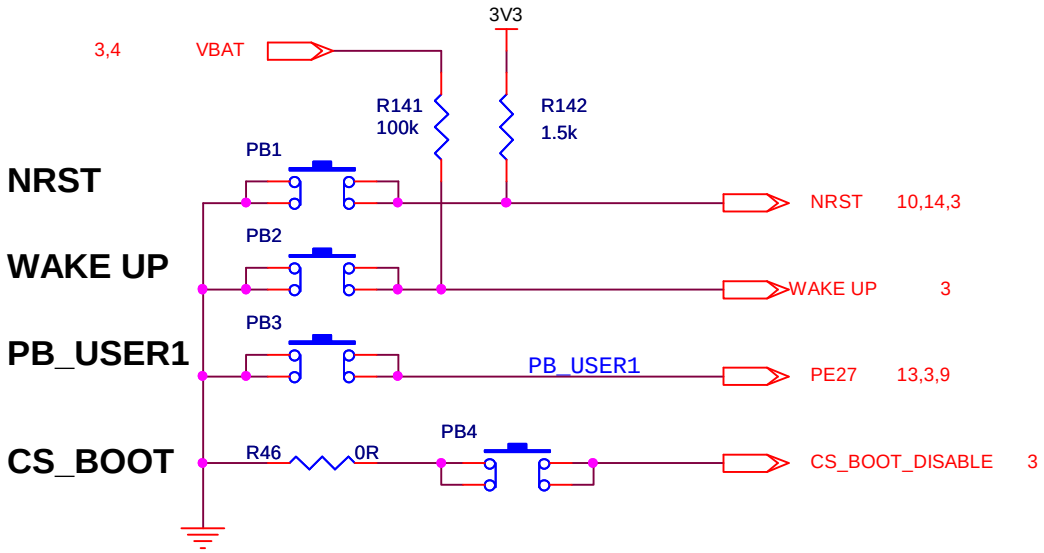
USB INTERFACE

SCALE 1/1

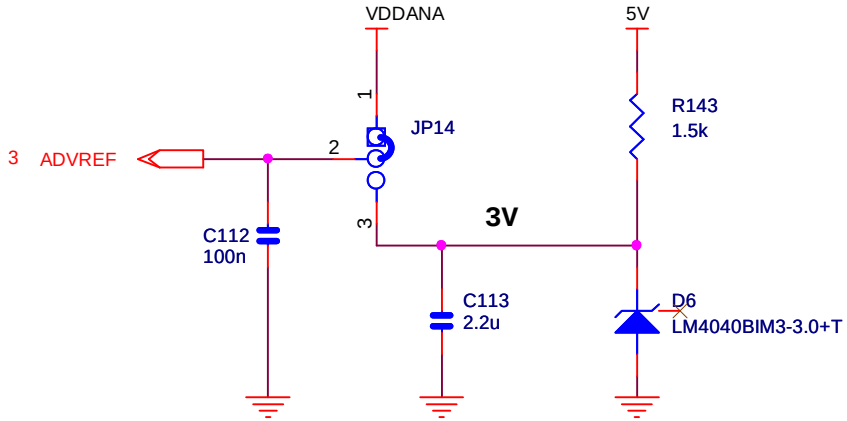
REV. C

SHEET 11/14

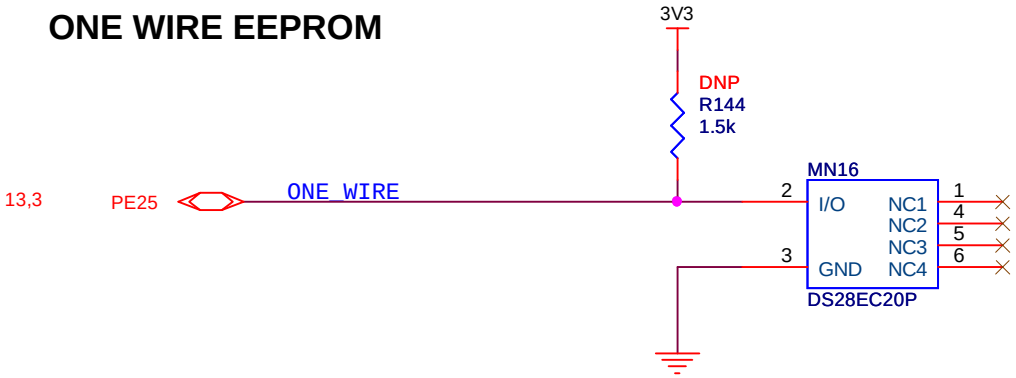
PUSH BUTTON



ANALOG Reference 3V



ONE WIRE EEPROM



REV	MODIF.	DES.	DATE	VER.	DATE
C		Derek	30-Sep-12	X.X	XX-XXX-XX
B		Derek	30-Mar-12	X.X	XX-XXX-XX
A		Derek	11-Nov-11	X.X	XX-XXX-XX

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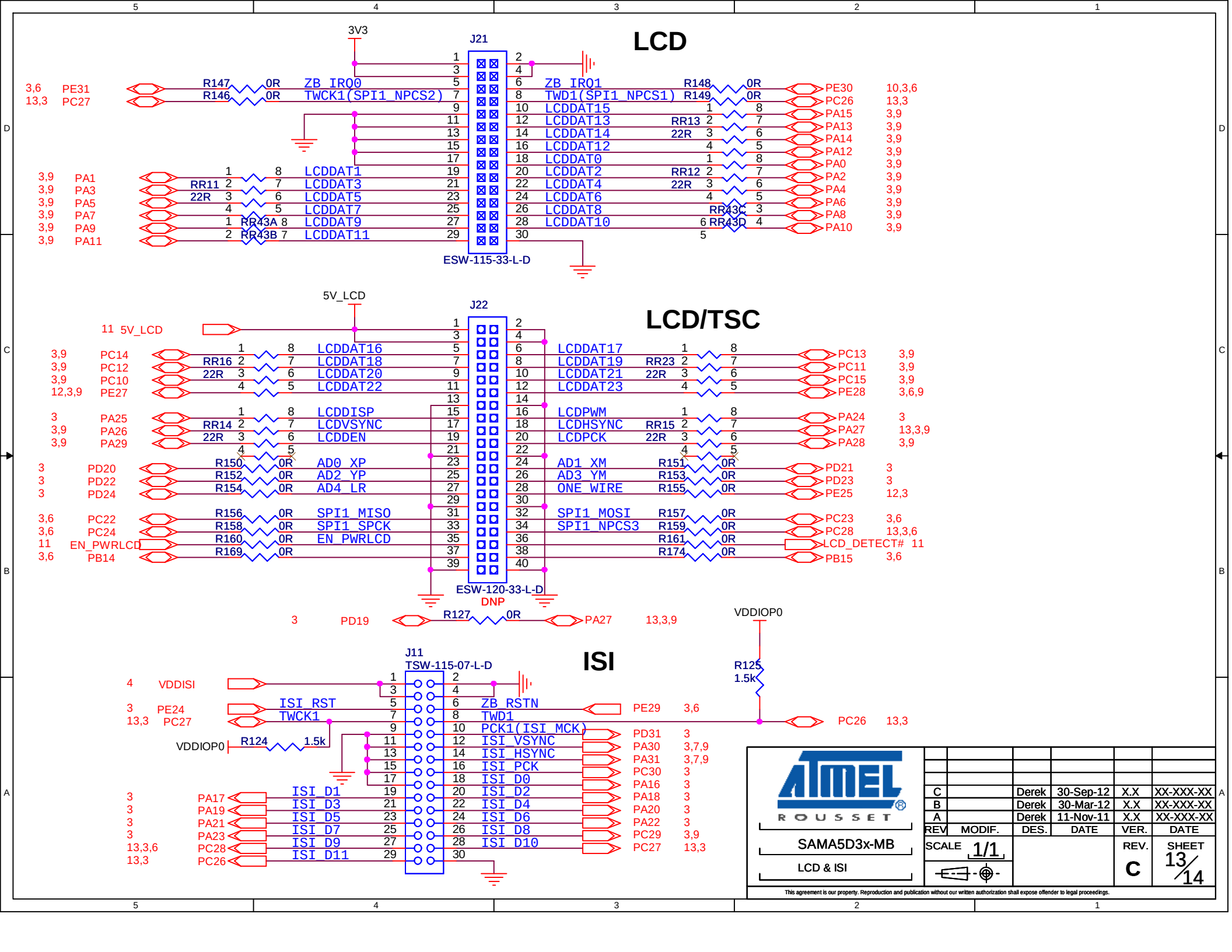
SAMA5D3x-MB

Miscellaneous

SCALE 1/1

REV. C

SHEET 12/14


LCD
J21
3V3
ESW-115-33-L-D
ZB_IRQ0
ZB_IRQ1
TWCK1(SPI1_NPCS2)
TWD1(SPI1_NPCS1)
LCDDAT15
LCDDAT13
LCDDAT14
LCDDAT12
LCDDAT0
LCDDAT2
LCDDAT4
LCDDAT6
LCDDAT8
LCDDAT10
LCDDAT1
LCDDAT3
LCDDAT5
LCDDAT7
LCDDAT9
LCDDAT11
LCD/TSC
J22
5V_LCD
ESW-120-33-L-D
DNP
LCDDAT16
LCDDAT18
LCDDAT20
LCDDAT22
LCDDAT17
LCDDAT19
LCDDAT21
LCDDAT23
LCDDISP
LCDVSYNC
LCDDEN
LCDPWM
LCDHSYNC
LCDPCK
AD0_XP
AD2_YP
AD4_LR
AD1_XM
AD3_YM
ONE_WIRE
SPI1_MISO
SPI1_SPCK
EN_PWRLCD
SPI1_MOSI
SPI1_NPCS3
LCD_DETECT#
ISI
J11
TSW-115-07-L-D
VDDIOP0
VDDISI
ISI_RST
TWCK1
ZB_RSTN
TWD1
PCK1(ISI_MCK)
ISI_VSYNC
ISI_HSYNC
ISI_PCK
ISI_D0
ISI_D1
ISI_D2
ISI_D3
ISI_D4
ISI_D5
ISI_D6
ISI_D7
ISI_D8
ISI_D9
ISI_D10
ISI_D11
ROUSSET
SAMA5D3x-MB
LCD & ISI
SCALE 1/1
REV C
SHEET 13/14
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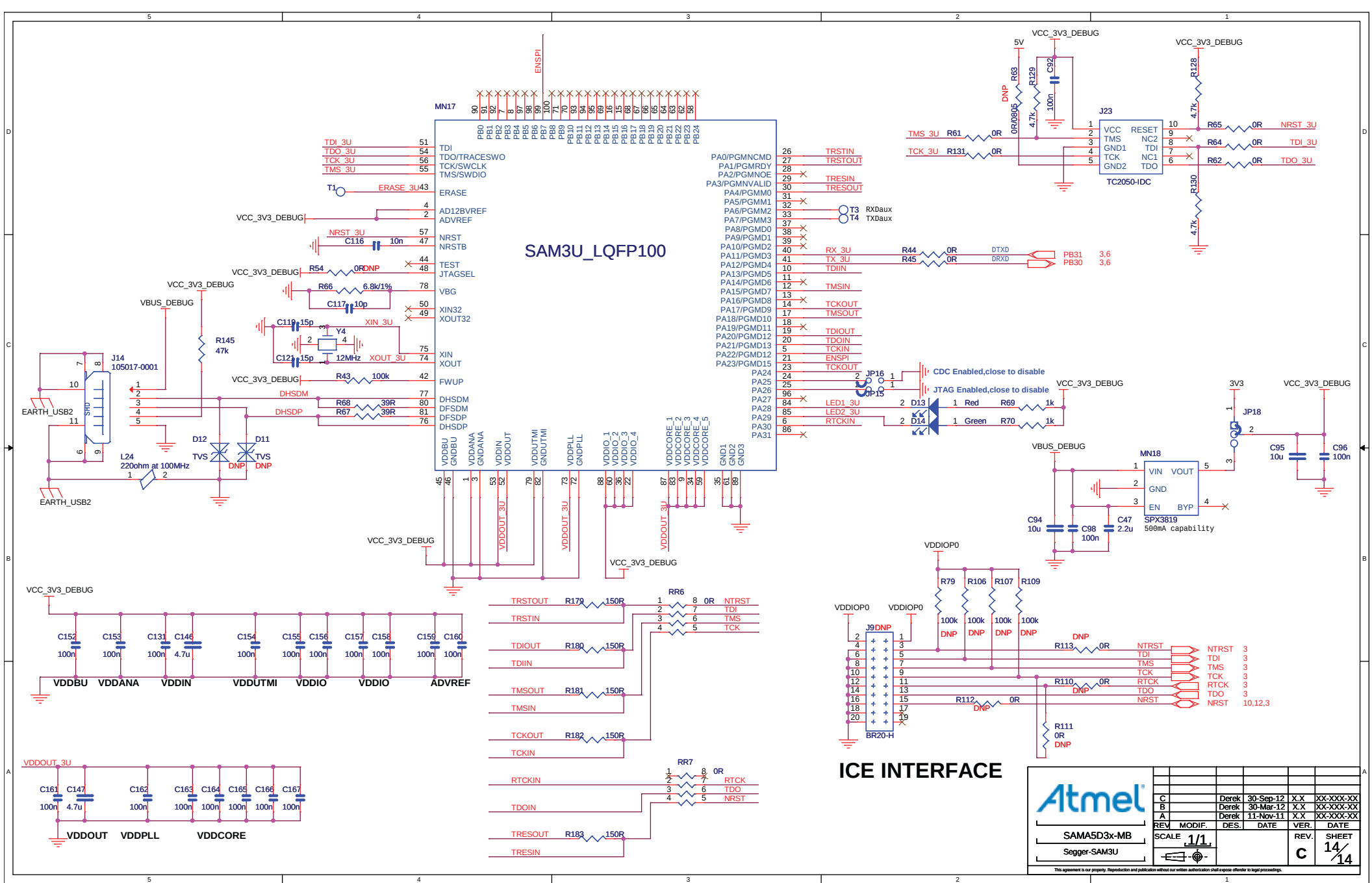
SAM3U_LQFP100
MN17
ENSPI
TDI_3U
TDO_3U
TCK_3U
TMS_3U
ERASE_3U
VCC_3V3_DEBUG
NRST_3U
C116 10n
R54 0R DNP
R66 6.8k/1%
C117 10p
C119 15p
C121 15p
Y4 12MHz
XIN_3U
XOUT_3U
R43 100k
DHSDM
DHSDP
R68 39R
R67 39R
R145 47k
VBUS_DEBUG
J14 105017-0001
EARTH_USB2
D12 TVS DNP
D11 TVS DNP
L24 220ohm at 100MHz
TRSTIN
TRSTOUT
TDIIN
TDIOUT
TMSIN
TMSOUT
TCKIN
TCKOUT
RTCKIN
TDOIN
TRESIN
TRESOUT
RXDaux
TXDaux
RX_3U
TX_3U
TMSIN
TMSOUT
TCKOUT
TDIIN
TDIOUT
TDOIN
TCKIN
ENSPI
LED1_3U
LED2_3U
RTCKIN
JP16
JP15
CDC Enabled,close to disable
JTAG Enabled,close to disable
D13 Red R69 1k
D14 Green R70 1k
R44 0R DTXD
R45 0R DRXD
PB31 3,6
PB30 3,6
VDDBU
VDDANA
VDDIN
VDDUTMI
VDDIO
VDDIO
ADVREF
VDDOUT
VDDPLL
VDDCORE
RR6
RR7
J23 TC2050-IDC
R63 DNP 0R/0805
R129 4.7k
C92 100n
R128 4.7k
R130 4.7k
R65 0R NRST_3U
R64 0R TDI_3U
R62 0R TDO_3U
MN18 SPX3819 500mA capability
C94 10u
C98 100n
C47 2.2u
C95 10u
C96 100n
JP18
3V3
VDDIOP0
R79 R106 R107 R109 100k DNP
R113 0R DNP
R110 0R DNP
R112 0R DNP
R111 0R DNP
J9 DNP BR20-H
NTRST
TDI
TMS
TCK
RTCK
TDO
NRST
ICE INTERFACE
SAMA5D3x-MB
Segger-SAM3U
SCALE 1/1
REV. C
SHEET 14/14
Derek 30-Sep-12 X.X XX-XXX-XX
Derek 30-Mar-12 X.X XX-XXX-XX
Derek 11-Nov-11 X.X XX-XXX-XX
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Section 7

Optional Display Module (DM)

7.1 DM Board Overview

DM board carries a 5.0” TFT LCD module with touch screen. DM board also carries four QTouch pads.

Figure 7-1. DM board

7.1.1 Equipment List

Here is the list of the DM board components:

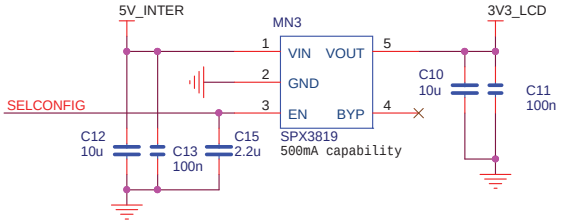
- One 5.0” TFT LCD module
- LCD back light driver
- 3.3V regulator
- QTouch device
- One-Wire device

7.1.2 Function Blocks

3.3V Regulator:

The 5-0_WVGA_R_AEA-DM Board features its own LDO for local power regulation. It accepts DC 5V power from 500 mA high-side power switch on EK and outputs a regulated +3.3V to most other circuits on the board.

Figure 7-2. DM Power Supply



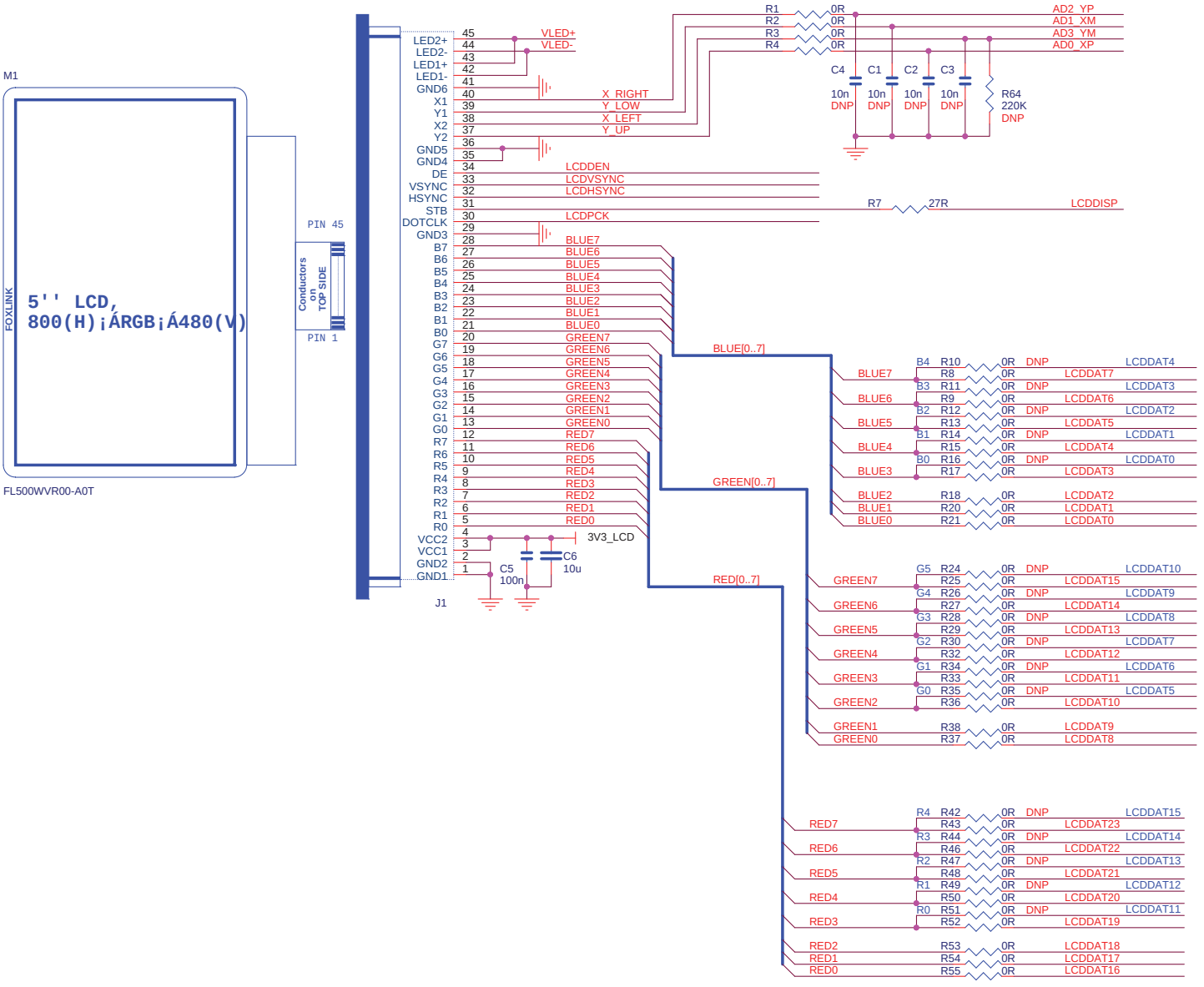
7.1.3 TFT LCD with Touch Panel

The 5-0_WVGA_R_AEA-DM features a LCD controller. The 5” 800x480 LCD provides the DM with a low power LCD display feature, back light unit and a touch panel, similar to that used on commercial PDAs.

Graphics and text can be displayed on the dot matrix panel with up to 16 million colors by supplying 24-bit data signals (8bit x RGB by default) or 16-bit data signals (5+6+5bit x RGB in option). This allows the user to develop graphical user interfaces for a wide variety of end applications.

Warning: never connect/disconnect the LCD display from the board while the power supply is on. This can damage the elements.

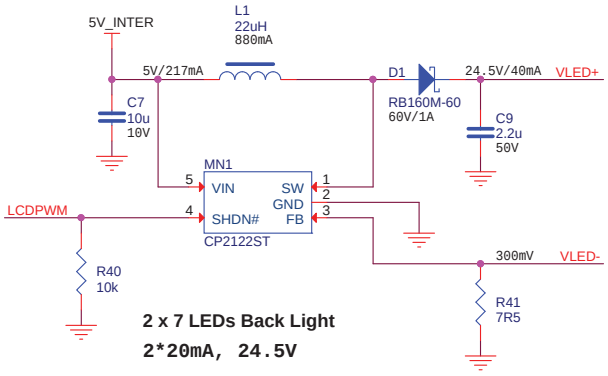
Figure 7-3. LCD with Touch Panel



7.1.4 Back Light

The back light voltage is generated from a CP2122ST/CP2123ST boost converter. It is powered directly by the DC 5V from the EK board. The back light level is controlled by a PWM signal generated from the SAMA5D3 series processor.

Figure 7-4. DM Back Light Control

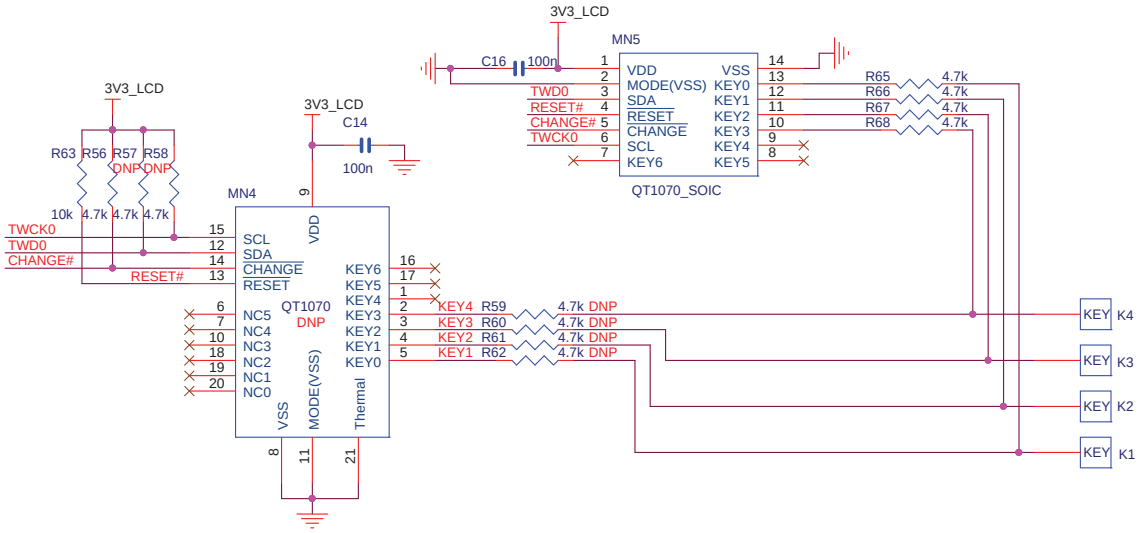


7.1.5 QTouch

The 5-0_WVGA_R_AEA-DM board carries a QTouch device piloted through a TWI interface. It manages four capacitive touch buttons directly printed on the PCB.

There is dual footprint for QTouch device, SOIC is the default mounted one.

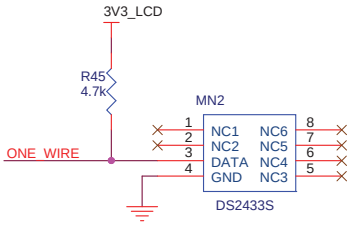
Figure 7-5. DM QTouch



7.1.6 One-Wire

The 5-0_WVGA_R_AEA-DM board also uses 1-Wire device as "soft label" to store the information such as chip type, manufacture name, production date, etc.

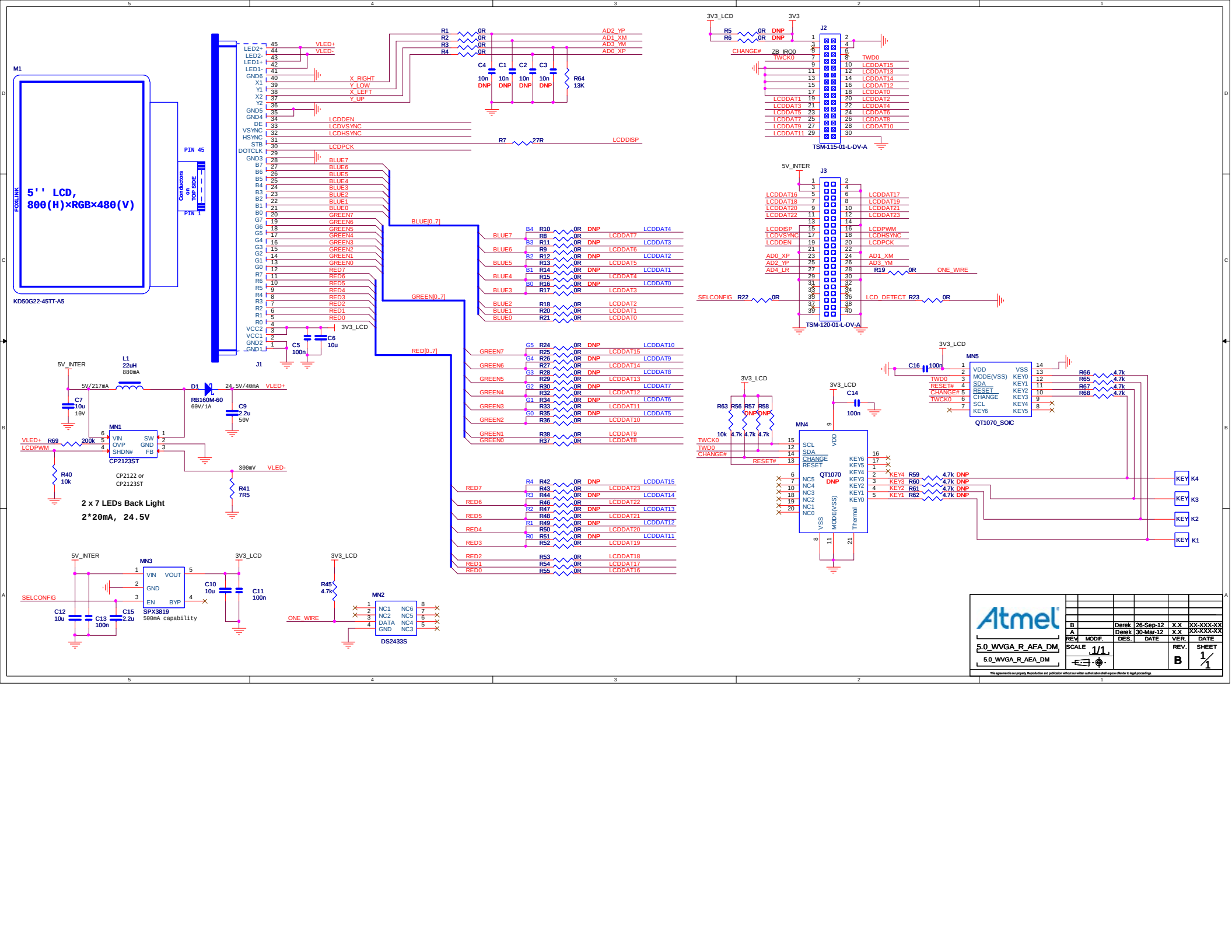
Figure 7-6. DM 1-Wire



7.2 Schematics

This section contains the following schematic:

- LCD Board


M1
5'' LCD,
800(H)×RGB×480(V)
KD50G22-45TT-A5
FOXLINK
PIN 45
PIN 1
Conductors
TOP SIDE
J1
LED2+
LED2-
LED1+
LED1-
GND6
X1
Y1
X2
Y2
GND5
GND4
DE
VSYNC
HSYNC
STB
DOTCLK
GND3
B7
B6
B5
B4
B3
B2
B1
B0
G7
G6
G5
G4
G3
G2
G1
G0
R7
R6
R5
R4
R3
R2
R1
R0
VCC2
VCC1
GND2
GND1
VLED+
VLED-
X_RIGHT
Y_LOW
X_LEFT
Y_UP
LCDDEN
LCDVSYNC
LCDHSYNC
LCDPCK
BLUE7
BLUE6
BLUE5
BLUE4
BLUE3
BLUE2
BLUE1
BLUE0
GREEN7
GREEN6
GREEN5
GREEN4
GREEN3
GREEN2
GREEN1
GREEN0
RED7
RED6
RED5
RED4
RED3
RED2
RED1
RED0
3V3_LCD
C5 100n
C6 10u
R1 0R
R2 0R
R3 0R
R4 0R
AD2_YP
AD1_XM
AD3_YM
AD0_XP
C4 10n DNP
C1 10n DNP
C2 10n DNP
C3 10n DNP
R64 13K
R7 27R
LCDDISP
BLUE[0..7]
GREEN[0..7]
RED[0..7]
LCDDAT4
LCDDAT7
LCDDAT3
LCDDAT6
LCDDAT2
LCDDAT5
LCDDAT1
LCDDAT4
LCDDAT0
LCDDAT3
LCDDAT2
LCDDAT1
LCDDAT0
LCDDAT10
LCDDAT15
LCDDAT9
LCDDAT14
LCDDAT8
LCDDAT13
LCDDAT7
LCDDAT12
LCDDAT6
LCDDAT11
LCDDAT5
LCDDAT10
LCDDAT9
LCDDAT8
LCDDAT15
LCDDAT23
LCDDAT14
LCDDAT22
LCDDAT13
LCDDAT21
LCDDAT12
LCDDAT20
LCDDAT11
LCDDAT18
LCDDAT17
LCDDAT16
3V3_LCD
3V3
R5 0R DNP
R6 0R DNP
CHANGE#
ZB_IRQ0
TWCK0
TWD0
J2
TSM-115-01-L-DV-A
5V_INTER
J3
TSM-120-01-L-DV-A
LCDDAT17
LCDDAT19
LCDDAT21
LCDDAT23
LCDPWM
LCDHSYNC
LCDPCK
AD1_XM
AD3_YM
R19 0R
ONE_WIRE
SELCONFIG R22 0R
LCD_DETECT R23 0R
5V_INTER
L1 22uH 880mA
5V/217mA
D1 RB160M-60 60V/1A
24.5V/40mA
VLED+
C7 10u 10V
C9 2.2u 50V
MN1
CP2123ST
VLED+ R69 200k
LCDPWM
R40 10k
CP2122 or CP2123ST
300mV
VLED-
R41 7R5
2 x 7 LEDs Back Light
2*20mA, 24.5V
MN3
SPX3819
500mA capability
SELCONFIG
C12 10u
C13 100n
C15 2.2u
C10 10u
C11 100n
MN2
DS2433S
R45 4.7k
ONE_WIRE
MN4
QT1070
DNP
R63 R56 R57 R58 DNP DNP
10k 4.7k 4.7k 4.7k
C14 100n
KEY0
KEY1
KEY2
KEY3
KEY4
KEY5
KEY6
R59 4.7k DNP
R60 4.7k DNP
R61 4.7k DNP
R62 4.7k DNP
KEY K4
KEY K3
KEY K2
KEY K1
MN5
QT1070_SOIC
C16 100n
R66 4.7k
R65 4.7k
R67 4.7k
R68 4.7k
Atmel
5.0_WVGA_R_AEA_DM
5.0_WVGA_R_AEA_DM
B Derek 26-Sep-12 X.X XX-XXX-XX
A Derek 30-Mar-12 X.X XX-XXX-XX
REV MODIF. DES. DATE VER. DATE
SCALE 1/1
REV. B
SHEET 1/1
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Section 8

Troubleshooting and Recommendations

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Section 9

Revision History

9.1 Revision History

Table 9-1.

Document	Comments	Change Request Ref.
11180A	First issue.	

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